Addressing Multi-Site Validation via a Modular Hardware Platform

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Mesa, Arizona • March 2–5, 2025

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- Multi-Site Validation Solution
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  - Device Cards
- Current State and Conclusion

Introduction

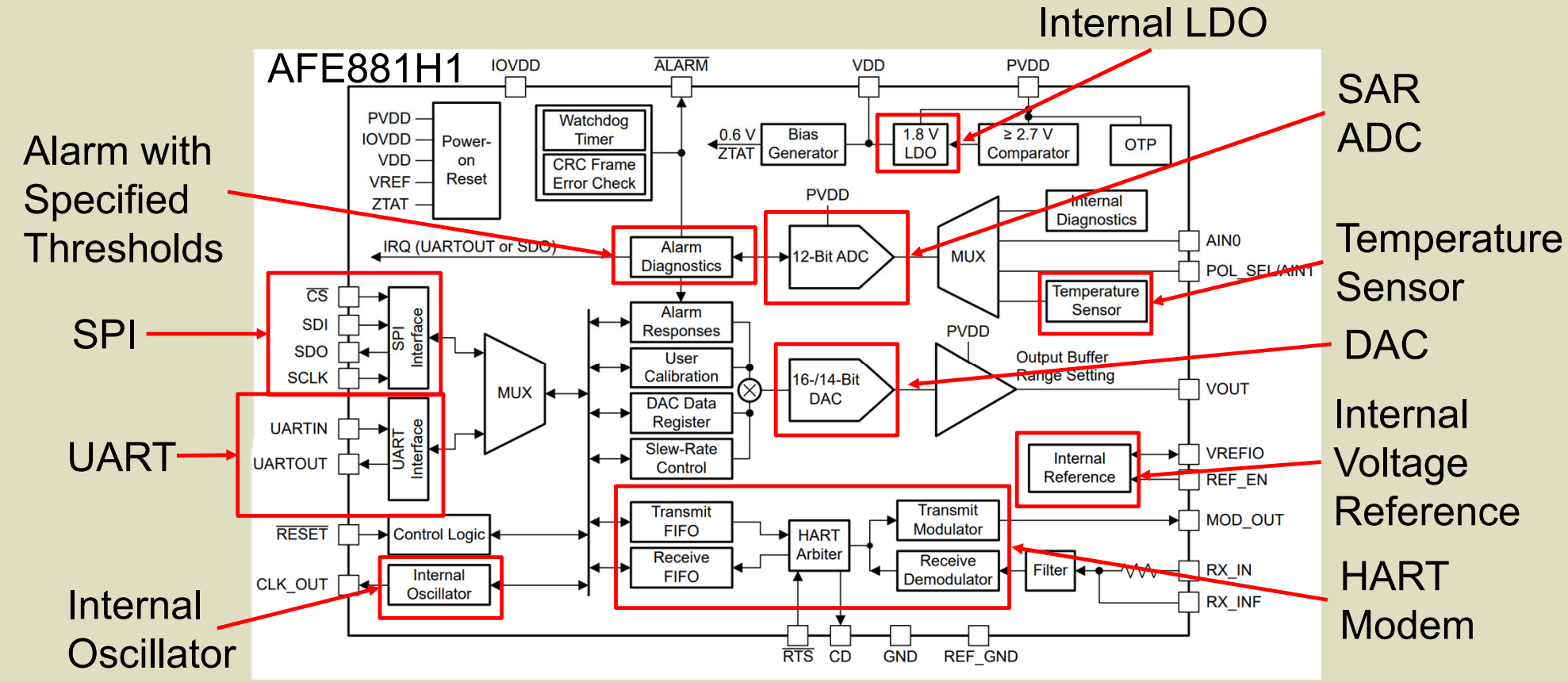
- Highly-integrated and complex integrated circuits (ICs) increase validation time
- ICs within a product family share basic functionality but may require different test hardware
- Single products exist in multiple packages, requiring more hardware
- ICs require validation at wider temperature range
- Individual validation systems for each product reduce software reuse
- Single site validation systems limit throughput
- A flexible, multi-site system is needed to maintain low product development time

Overview of TI's DAC Portfolio

- TI's DAC portfolio features wide variety of products with device specific features and functions

AFE881H1	• 16-bit low-power voltage output DAC • 12-bit ADC, integrated voltage reference and oscillator • 24 pin QFN package
DAC11001B	• 20-bit unbuffered voltage output DAC • External buffered voltage reference required • 48 pin QFP package
DAC530A2W	• 10-bit current and voltage output DACs • Integrated voltage reference, non-volatile memory • 16 pin WCSP BGA package

Overview of TI's DAC Portfolio



Validation of DACs

- DACs require extensive validation due to ATE limitations
- Detailed over-temperature characterization only done by validation engineers, not production ATE
- Some key performance metrics are unable to be fully characterized in production

DYNAMIC PERFORMANCE				
	Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling time to ±2 LSB, AV_{DD} = 5.5V, V_{REFIN} = 2.5V, gain = 2	6	µs
	Slew rate	AV_{DD} = 5.5V, V_{REFIN} = 2.5V	1.7	V/µs
	Power-on glitch magnitude	DAC code = zero scale	25	mV
	Output noise	0.1Hz to 10Hz, DAC code = midscale	12	µVpp
	Output noise density	1kHz, DAC code = midscale, AV_{DD} = 5.5V, V_{REFIN} = 2.5V	65	nV/Hz

Validation of DACs

- Validation occurs outside of a tester environment
  - Engineers aren't constrained by the tester resources
- Requires design of a validation solution capable of testing a given product
  - Includes test resource selection, schematic capture, PCB design, software design
- A full validation solution is required to meet all parameters in an acceptable timeframe

Validation of DACs

- All DACs share validation test types
  - DAC Linearity: INL, DNL, TUE, Gain Error, Full Scale Error, Offset Error, Zero Scale Error
  - Loading Characteristics: Load Regulation, Output Amplifier Headroom, Short Circuit Current, Output Impedance
  - Dynamic Performance: Output Settling Time, Output Slew Rate, Code Change Glitch Energy, Output Noise, PSRR
- Highly integrated products also share test types
  - Internal reference temperature drift
  - ADC linearity
  - Thermal hysteresis and package stress effects

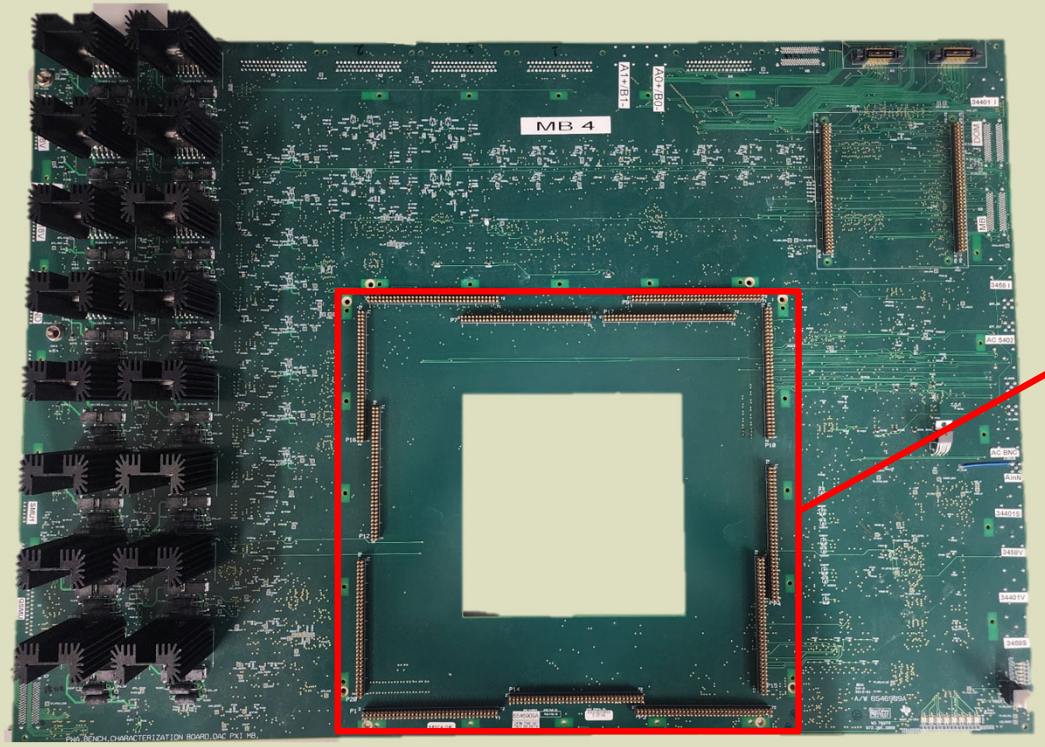
Validation of DACs

- Specific parameters must be characterized over temperature
- Push for wider -55°C-150°C temperature range in recent years
- Characterization at low temperatures causes icing and condensation, increasing risk of board failure
- Products available in multiple packages require validation of each package type
- Due to shared tests between products there is an opportunity for a generic platform that is adapted to each specific device

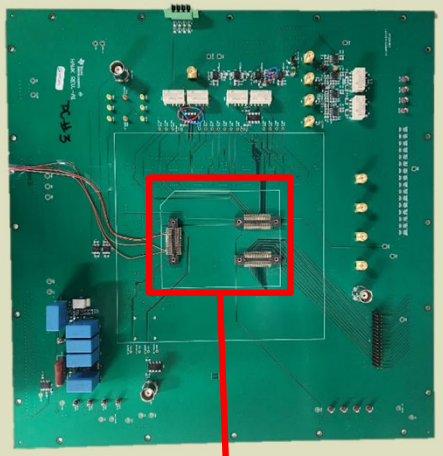
Single-Site Validation Solution

- Previous validation solution for DAC team was a single-site platform
- Basic external resources were used to make generic test resources
  - Power supplies
  - Source/Measure Units
  - Analog Inputs/Outputs
  - Digital Inputs/Outputs
- Device specific and package specific daughter cards interfaced with motherboard

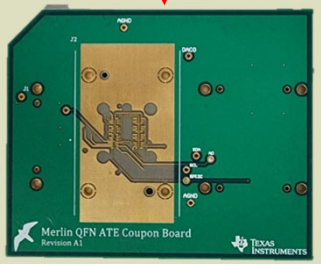
Single-Site Validation Solution



Generic Motherboard



Device Specific Coupon



Package Specific Coupon

TestConX™

Single-Site Validation Solution

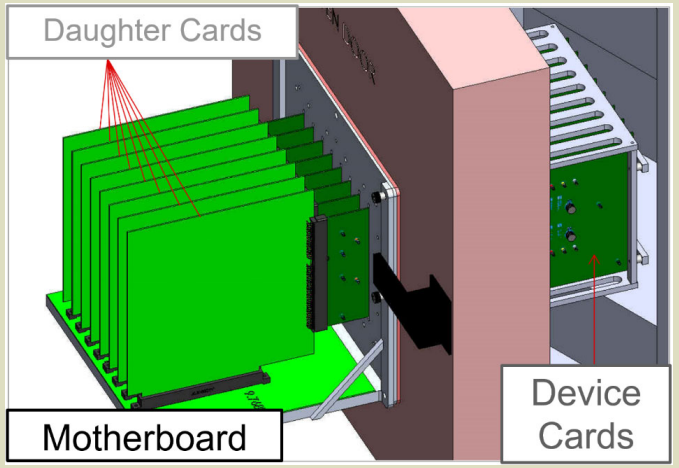
- Platform was capable, but had severe limitations
  - Excessively complex hardware → Steep learning curve for new engineers
  - Static test resources → Unable to adapt to higher voltage/power parts
  - Defined for current, not future roadmap devices
  - Physically large board → Difficult to fully bring to extreme temperatures
  - Many points of failure → Excessive debug time
  - Forced-air for temperature characterization → Icing and condensation
  - In practice resources only for single site → Limited throughput
- In short: too much, too rigid, too slow

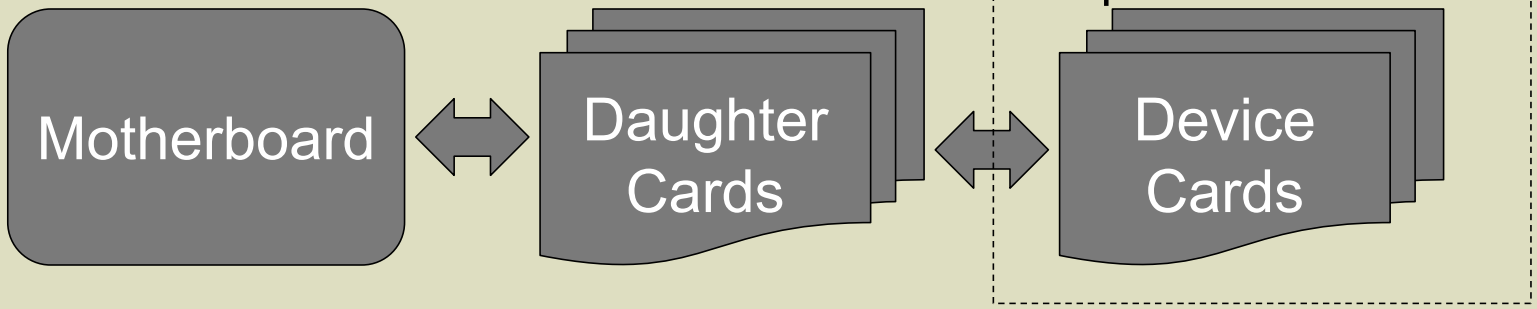
Multi-Site Validation Solution

- Learning from the single site system, a new system required:
  - Modular, flexible hardware
  - Generic test resources from external equipment
  - Temperature testing done within an temperature chamber (TC)
  - Support true multi-site testing for majority of TI DAC devices
  - Maintain similar abstraction and separation of responsibilities to deal with different test types and products

Multi-Site Validation Solution Architecture

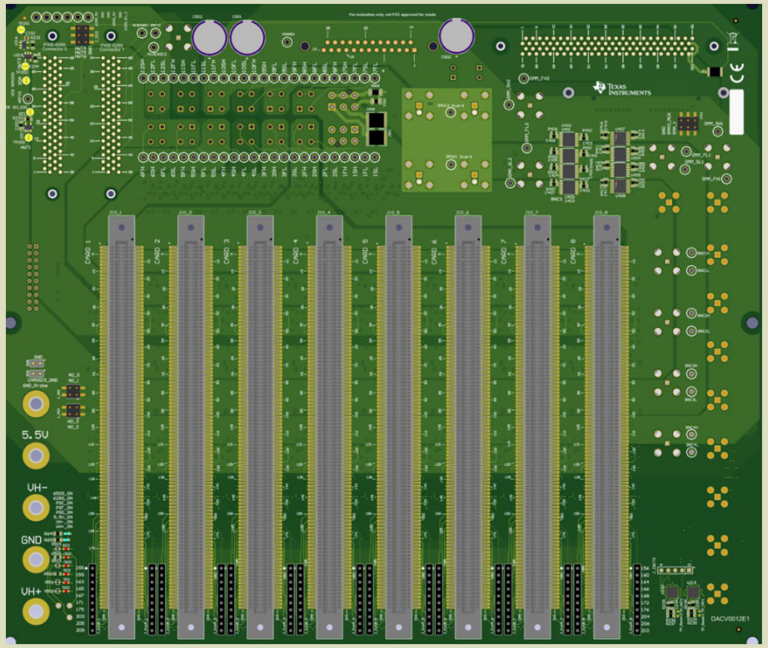
- 3-Layer hardware stack
  - Resource distribution motherboard
  - Multiple test specific daughter-cards
  - Multiple device specific grand-daughter cards
- Motherboard and daughter-cards externally dock to oven
- Device specific cards contained fully within TC





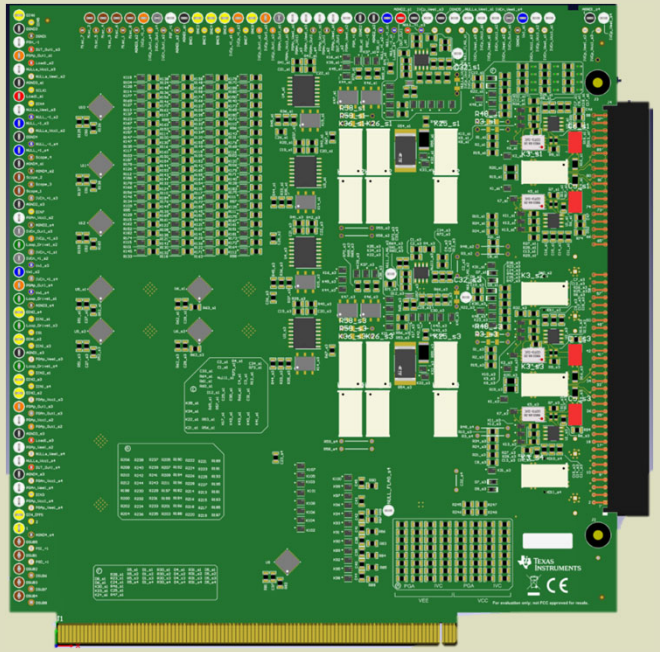
Multi-Site Validation Solution Motherboard

- Single point of interface for all test equipment
- Test resources are distributed to multiple daughter cards in 3 ways
  - Broadcast: Accessible by all daughter cards at all times
  - Multiplexed: Accessible by all daughter cards one at a time
  - Dedicated: Accessible by a single daughter card at all times
- All test resources come from external equipment



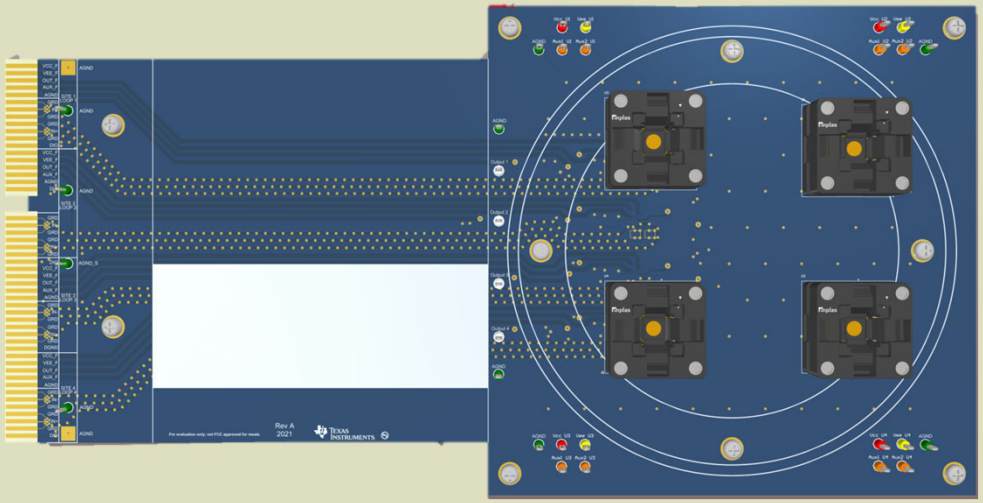
Multi-Site Validation Solution Daughter-Cards

- Daughter-cards designed for specific test types
  - Voltage output DAC linearity
  - ADC linearity
  - Voltage reference temperature drift
  - Long term drift
- Common pinout/connector to device specific cards
- Highly integrated devices are tested with a combination of daughter-cards



Multi-Site Validation Solution Device-Cards

- Only part of the system stressed over temperature
- Only part of the system that is device specific
- Device-cards support multiple DUTs per card
- Different cards for different packages
- Different cards for pre/post solder stress analysis



Systems Compared

Parameter	Single Site Solution	Multi-Site Solution
Flexibility	Low	High
Debug Time	High	Low
New Product Development Cost	Low	Low
Cold Temperature Testing Capability	Low	High
Shared Software Across Products	High	High
Multiple Package Testing Capability	High	High
Throughput	Low	High

Current State and Conclusion

- First generation motherboard and daughter board in use on pilot project
- Additional daughter boards targeting different parameters in development
- TC based testing allowing -55°C characterization with no icing concerns
- Platform approach and architecture being considered by other TI teams

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