Enabling Near-DUT Voltage Sense and Control

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TestConX™

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Outline

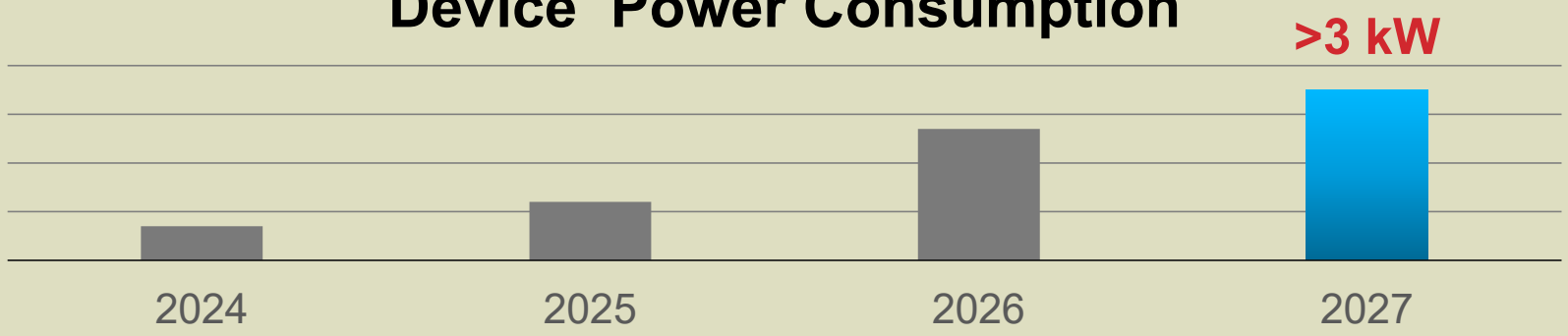
- Key challenges arising from HPC / AI trends and process shrinks
- Status quo, shortcomings of current interconnect solutions
- Interconnect design approach addressing these shortcomings

Effects of Power Trend

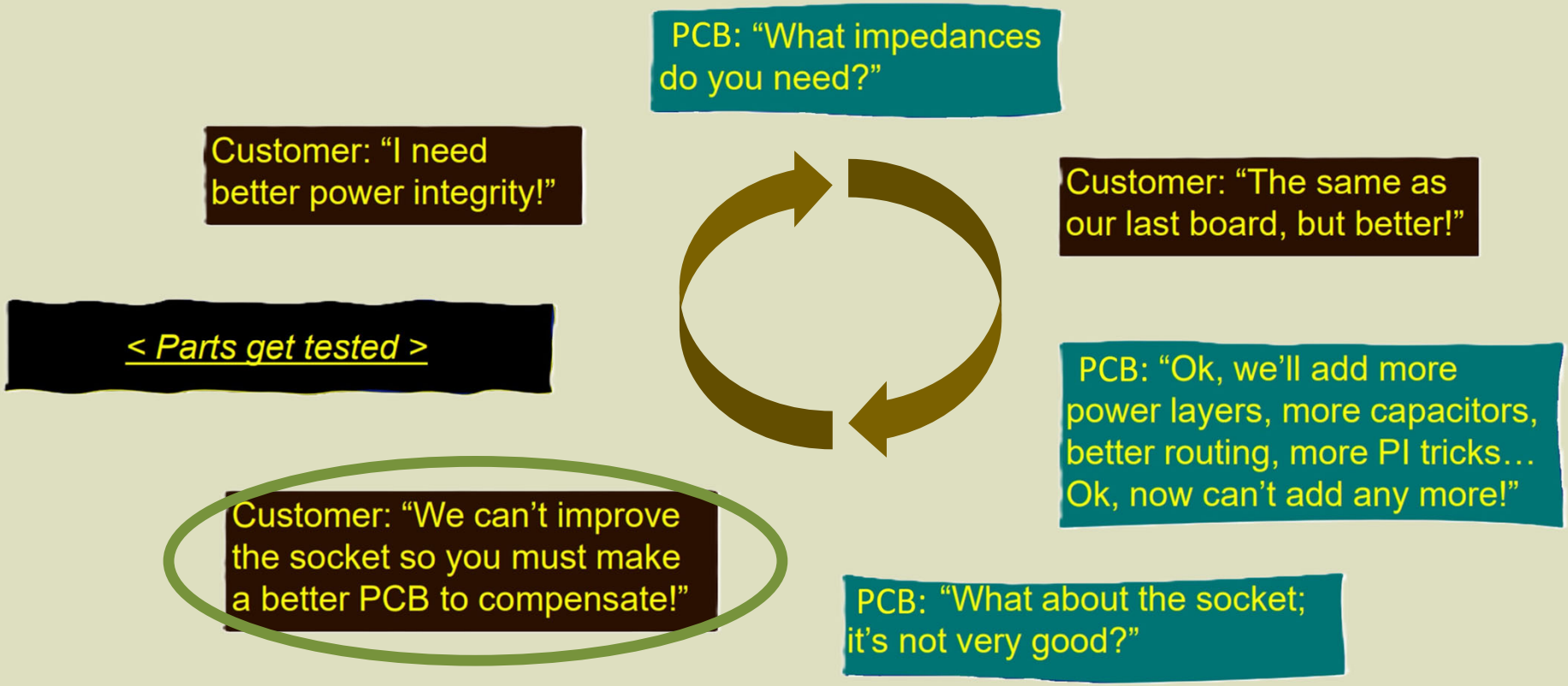
- The power / heat dissipation trend combined with fab process shrinks presents 3 key challenges
  - Locally concentrated current draw
  - Locally concentrated heat dissipation (hot spots)
  - Voltage stability / power integrity

Related

Device Power Consumption

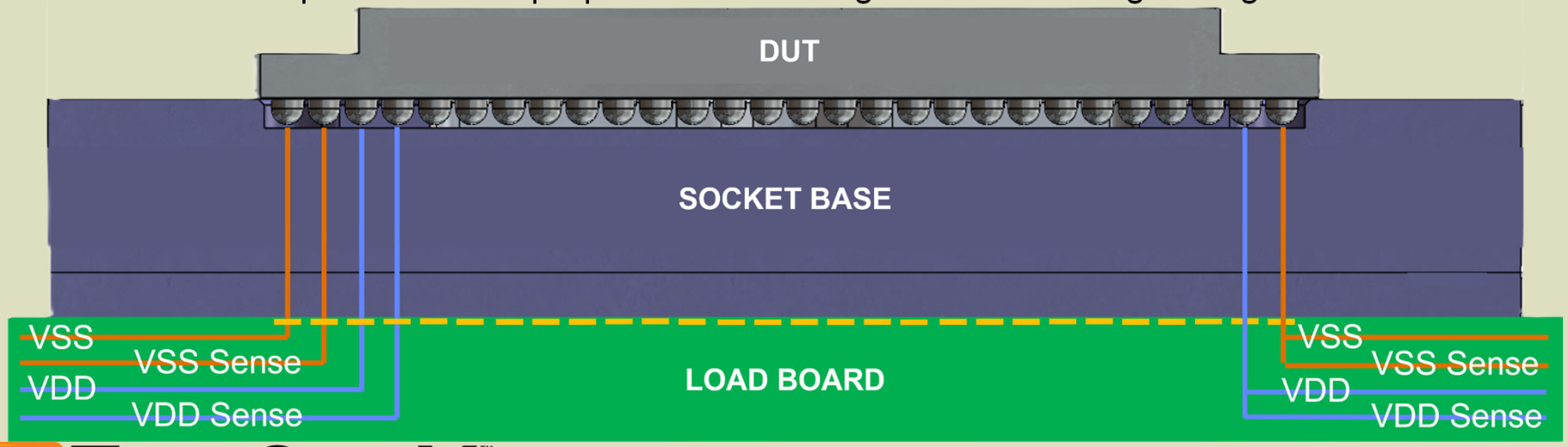


The Typical Model for Power Integrity



Limitations of Standard Interconnects

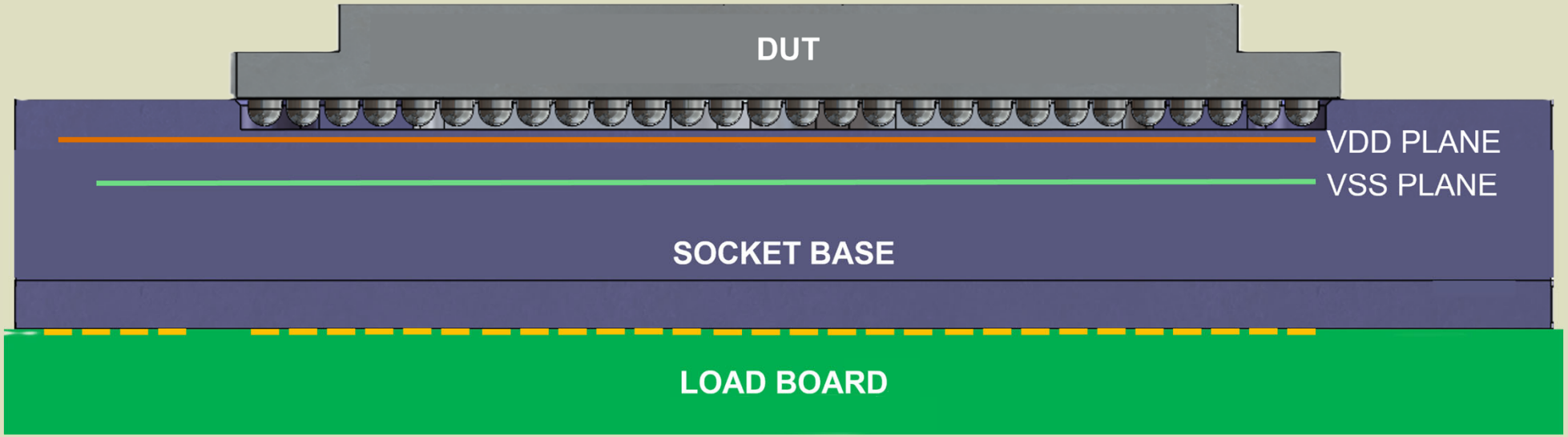
- Power integrity becomes more difficult as current and dI/dt increases
  - If tester voltage reference is on PCB side of the interconnects, parasitic losses decrease control
  - VDD/VSS pins can be repurposed for sensing if there is enough margin



ENHANCED INTERCONNECT DESIGN

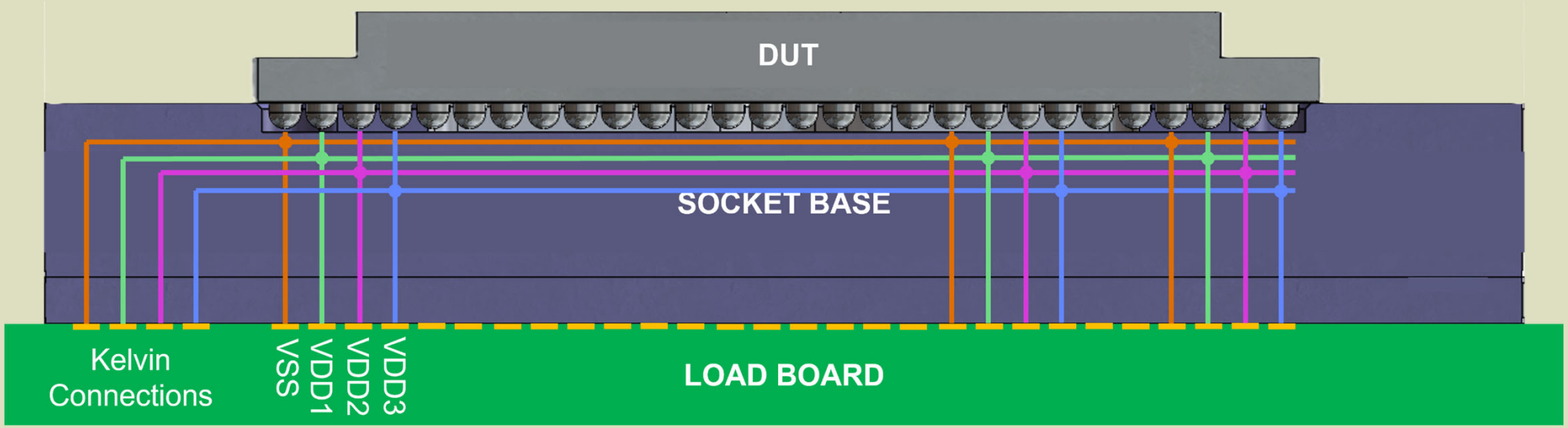
Integrated VDD / VSS Planes

- Integrate VDD and VSS planes into the test socket, near the DUT



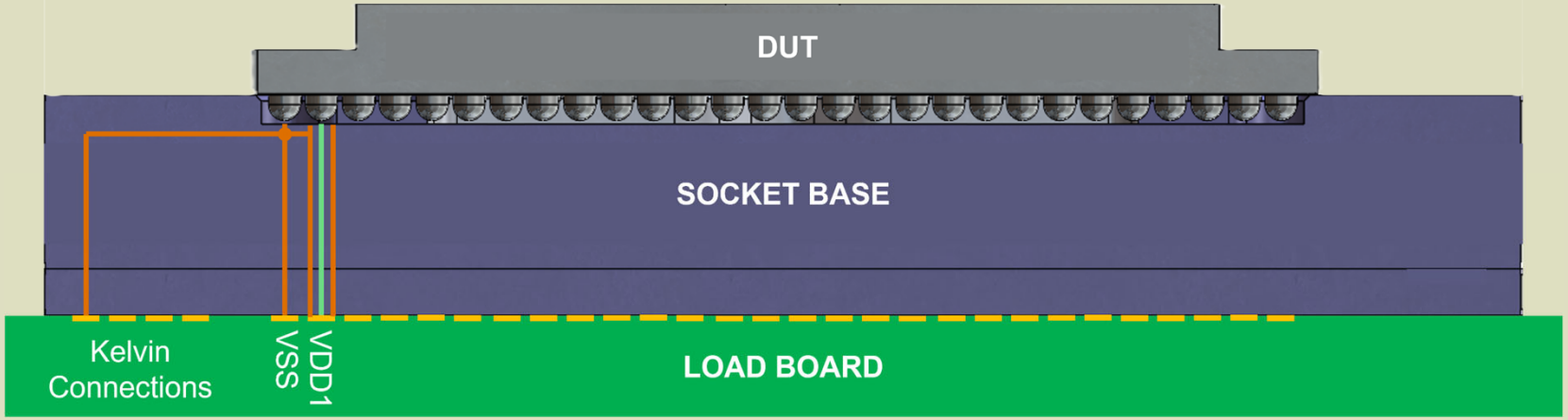
Near-DUT Voltage Sensing

- Planes / traces can connect additional VDD/VSS pins outside the DUT footprint for a Kelvin connection to the tester

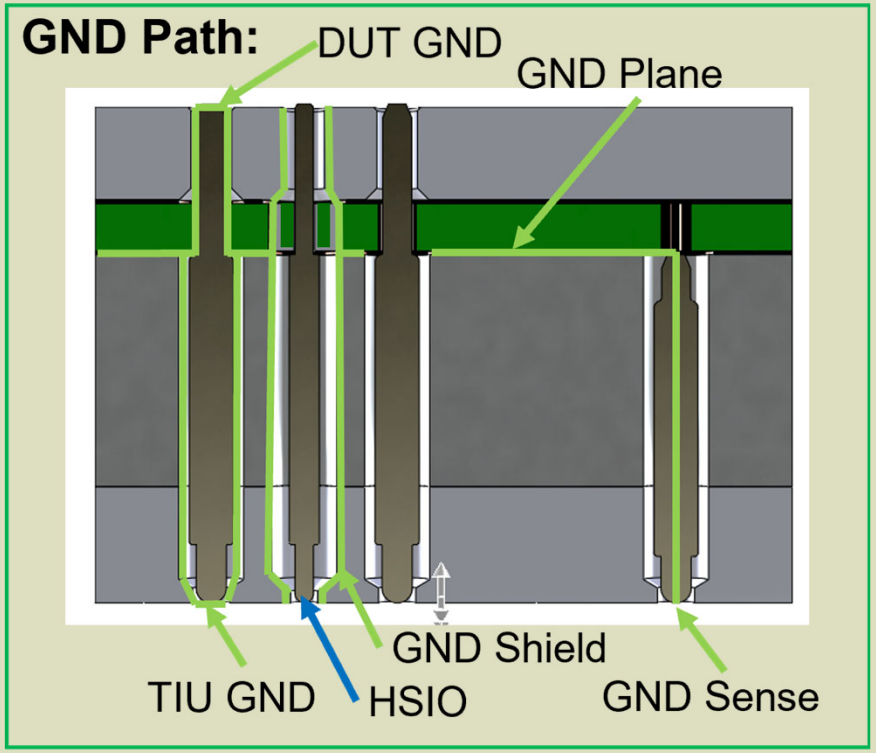


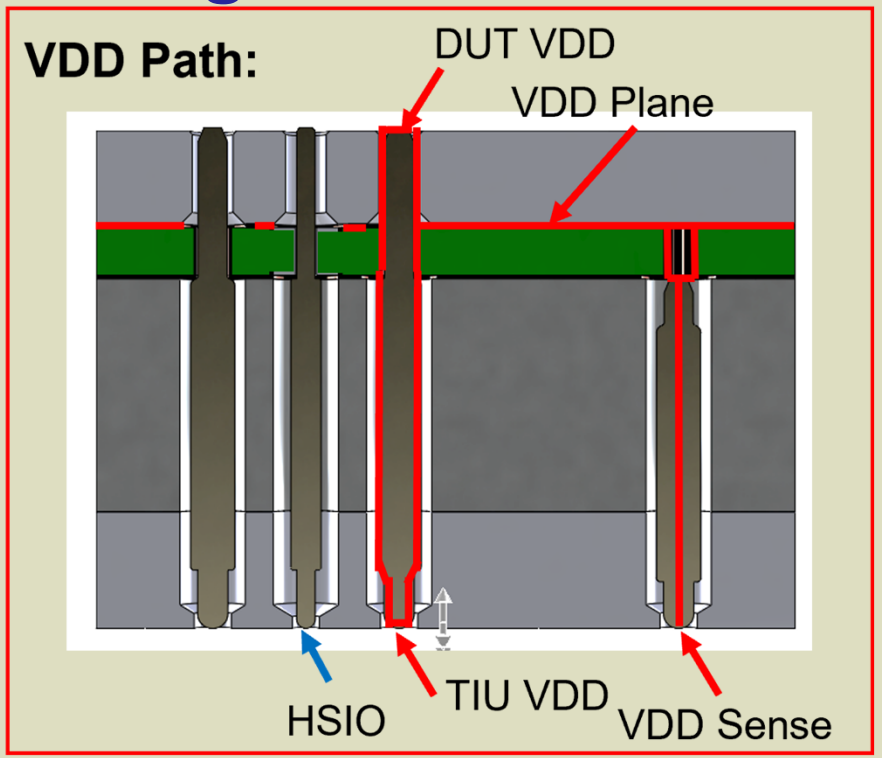
Coax Construction

- Increasing bandwidths / Nyquist requires coax construction to meet NEXT / FEXT requirements
- Impedance tolerance also tightens



Socket Design





TIU: Test Interface Unit, Load Board

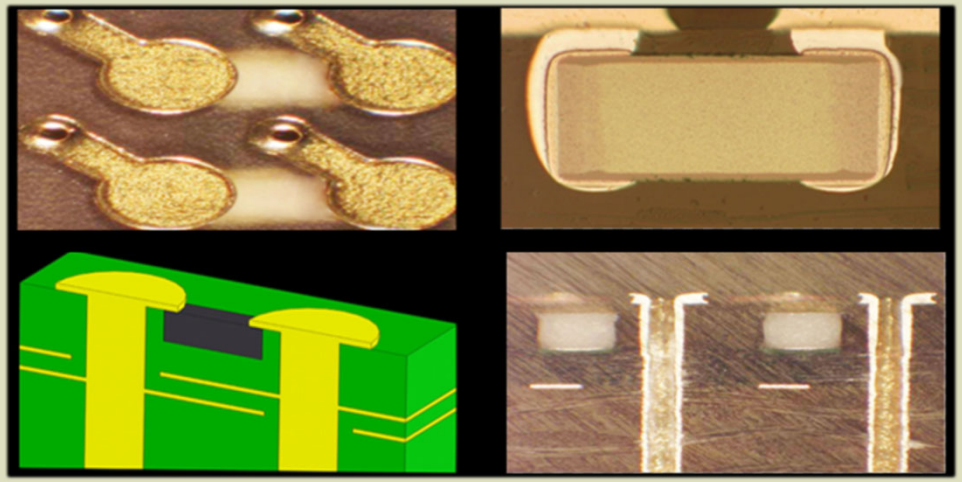
Patent Pending

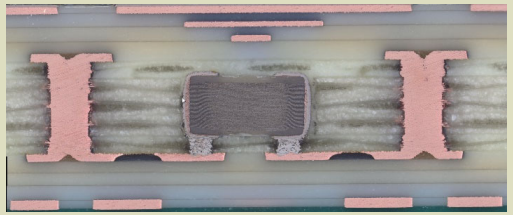
HSIO: High-speed I/O

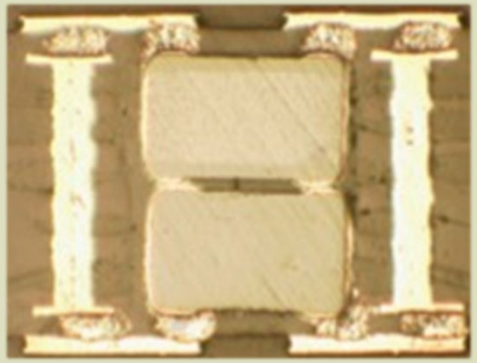
ADDITIONAL CONSIDERATIONS

Enhanced De-Coupling

- VDD / VSS planes add capacitance near DUT
- Add capacitors near DUT in some areas / some applications, interstitial may also be possible

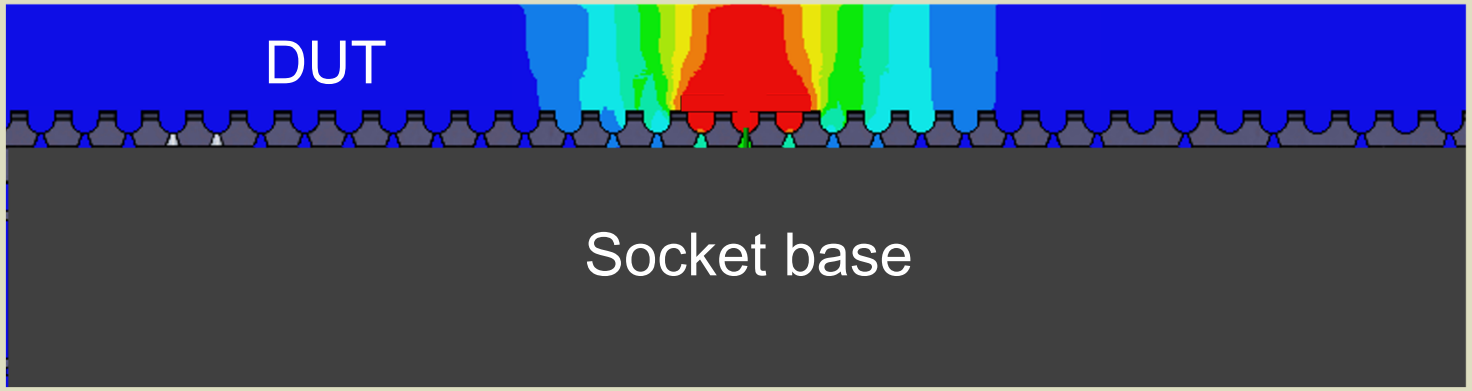






Limitations of Standard Interconnects - Thermal

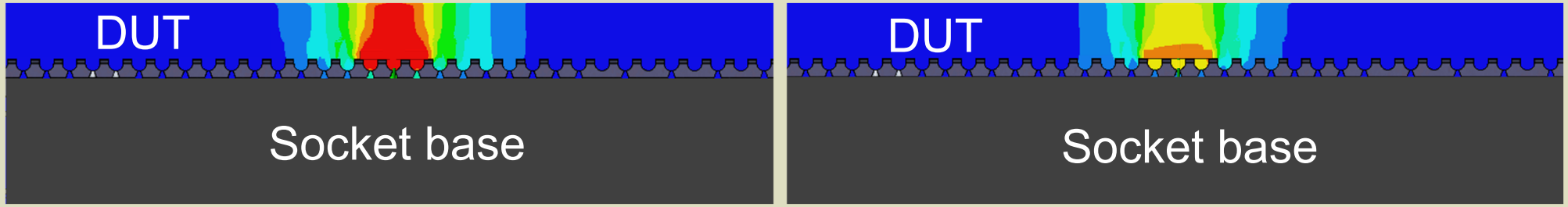
- Interconnect contact elements (spring probes, etc.) are typically isolated electrically and thermally
  - Poor thermal conduction to PCB
  - Unable to spread current and heat laterally to mitigate hot spots



Current and Heat Spreading

- Electrical current can be spread across the planes
- Socket can act as a heat sink, additional spreading and dissipation

Temperature contour plot comparison – Localized Hot Spot



No VDD/VSS Planes

VDD/VSS Plane

Elastomer Interconnects

- Why not just use elastomer interconnects?
  - Elastomers usually have low inductance and CRES, reducing the parasitic losses
  - Not good spreaders or conductors of heat, current can't spread laterally
  - Adding de-coupling capacitance difficult
  - Voltage measurements / control won't be as accurate
  - Without coax, crosstalk can limit bandwidth esp. large pitch devices

Summary

- Rapidly increasing power delivery challenges the conventional socket design
- Constructing a socket with integrated planes and circuitry can mitigate several of these challenges
  - Voltage sensing at the DUT without sacrificing pins
  - Maintain coax shielding along full length of interconnect
  - Spreading the current and heat away from localized hot spots
  - Embedded capacitance to further mitigate transients

Acknowledgements

- “Solving Socket Power Integrity; The Last Link in the Chain”, Don Thompson and David Unger, R&D Altanova, TestConX 2022
- “Enabling High-speed Loopback Tests for Serdes, PCIE Gen5/6 on Probe Using Embedded Capacitors on the MLO”, Quaid Joher Furniturewala, R&D Altanova, SWTest 2023

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