Challenges and Strategies for Testing 224 Gbps SerDes

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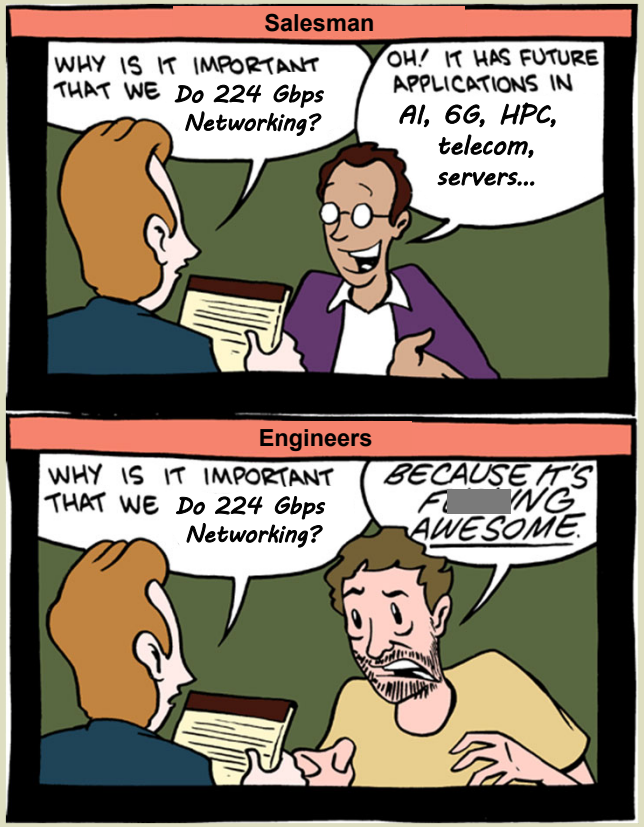
TestConX™

Mesa, Arizona • March 2–5, 2025

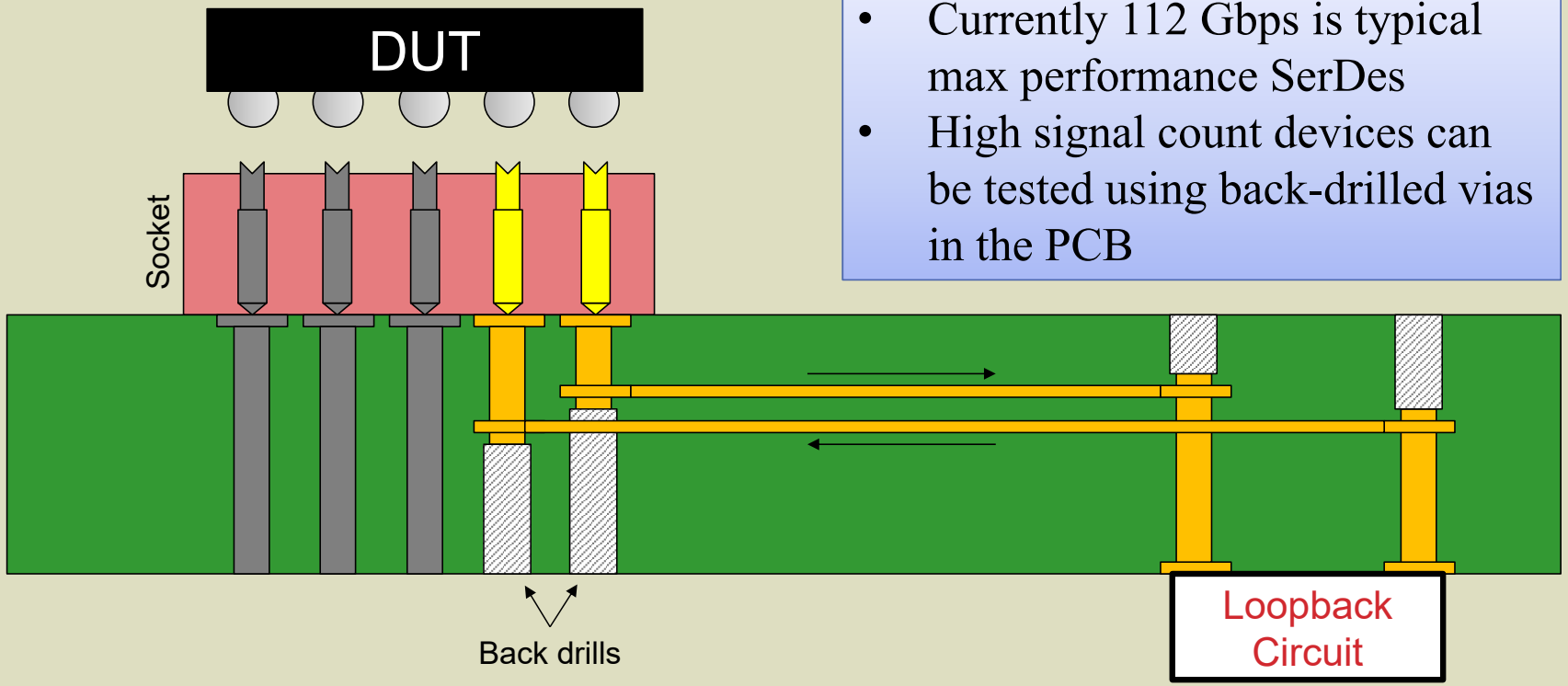
Why Do We Need 224 Gbps?

- **AI**: Faster data processing for complex model training
  - The speed of the link between nodes is the primary limiter of the AI network
- **Internet**: Smoother streaming, quicker downloads, lower latency
- **HPC**: Accelerated scientific research and simulations
- **Data Centers**: Improved performance and efficiency
- **Telecom (5G/6G)**: Supports next-gen mobile networks and applications
- **Autonomous Vehicles**: Real-time data processing for safe autonomous navigation
- **Industrial Automation**: Enhanced efficiency and control



Comic modified from smbc-comics.com

The Standard SerDes Test Structure



- Currently 112 Gbps is typical max performance SerDes
- High signal count devices can be tested using back-drilled vias in the PCB

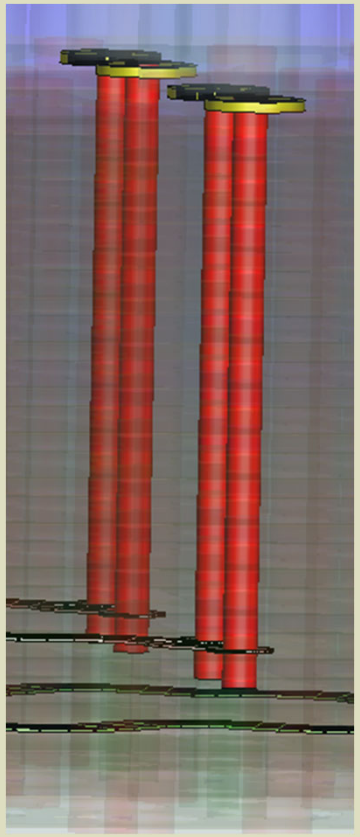
Migrating from 112 Gbps to 224 Gbps

Initially, these were our concerns, in order of perceived risk:

1. Through hole vias
2. Trace length
3. Sockets
4. Loopback components
5. Manufacturing tolerances

Through-Hole Vias

- Vias MUST be optimized using a 3D field solver (e.g. HFSS or CST)
- The via impedance must be matched with the target impedance (Note: SerDes is often 85 Ω or 92 Ω)
- Impedance is tuned by adjusting the drill diameter and copper plane keep-outs to adjust the capacitance and inductance
- Performance for a good tuned impedance via is historically around 45 to 50 GHz



Trace Loss: A Problem of Physics, Part 1

- As frequency increases, loss increases exponentially thus a mostly straight line on a dB plot
- Skin depth has a square root relationship with frequency

$$R_{skin}(f) \propto \sqrt{f}$$

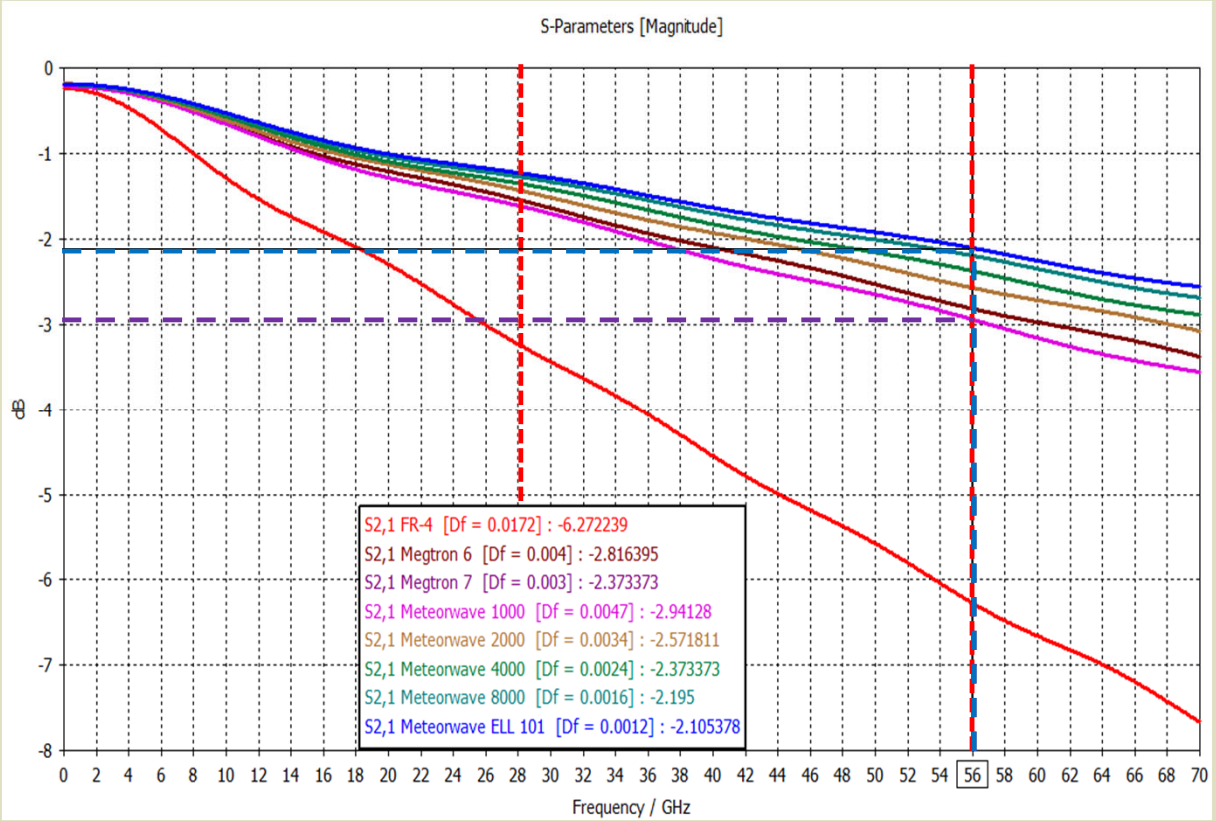
- Dielectric loss is linear with frequency

$$P_{loss}(f) \propto f$$

- In our area of interest (5GHz to 56 GHz) trace loss is mostly linear on a dB vs frequency plot

Trace Loss: A Problem of Physics, Part 2

- Trace loss is primarily a function of conductor loss and dielectric loss
- Conductor loss is dominated by “skin effect”
- Dielectric loss is defined by the material’s loss tangent
- Trace loss is additive per unit length (3dB + 3dB = 6dB)
- 224 Gbps PAM4 is 1.5x to 2x more lossy versus 112 Gbps PAM4
- <u>This means more loss for same trace length!</u>



The Conclusion Is….

Traces must get shorter

or

Traces must get wider

or

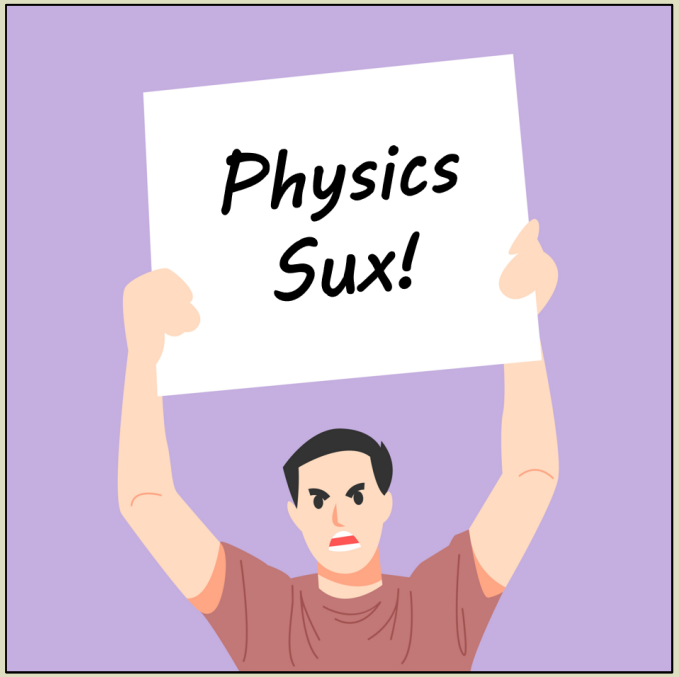
Dielectrics must get better

or

Copper must get smoother

or more likely

the silicon must accept more loss!



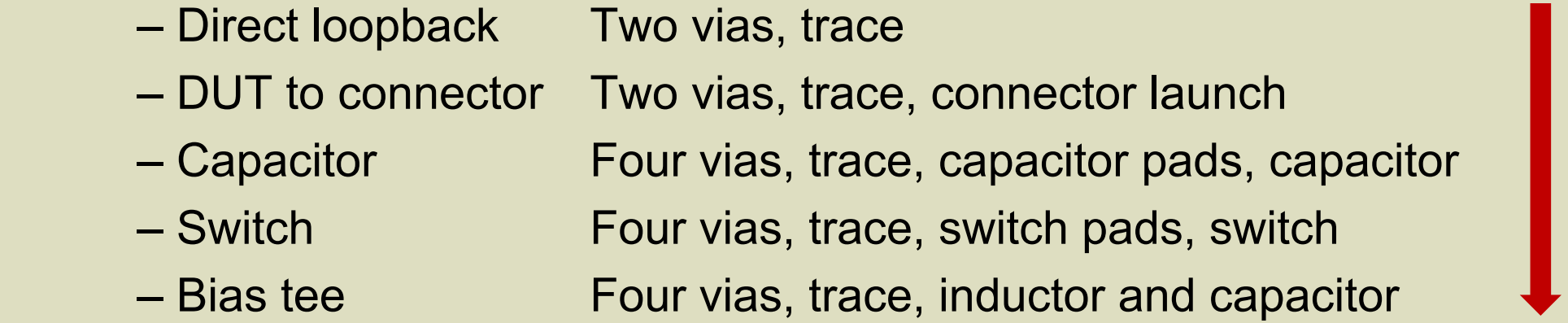
Picture by M. Irkham Saddad

Typical 224 Gbps Test Options

SerDes Test Options

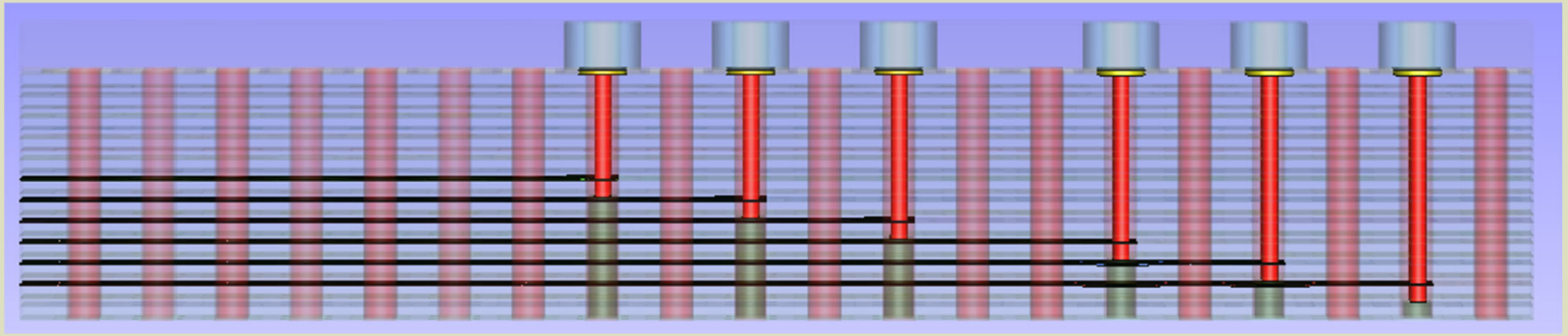
– Direct loopback	Two vias, trace
– DUT to connector	Two vias, trace, connector launch
– Capacitor	Four vias, trace, capacitor pads, capacitor
– Switch	Four vias, trace, switch pads, switch
– Bias tee	Four vias, trace, inductor and capacitor pads, capacitor, 2x inductors

Difficulty



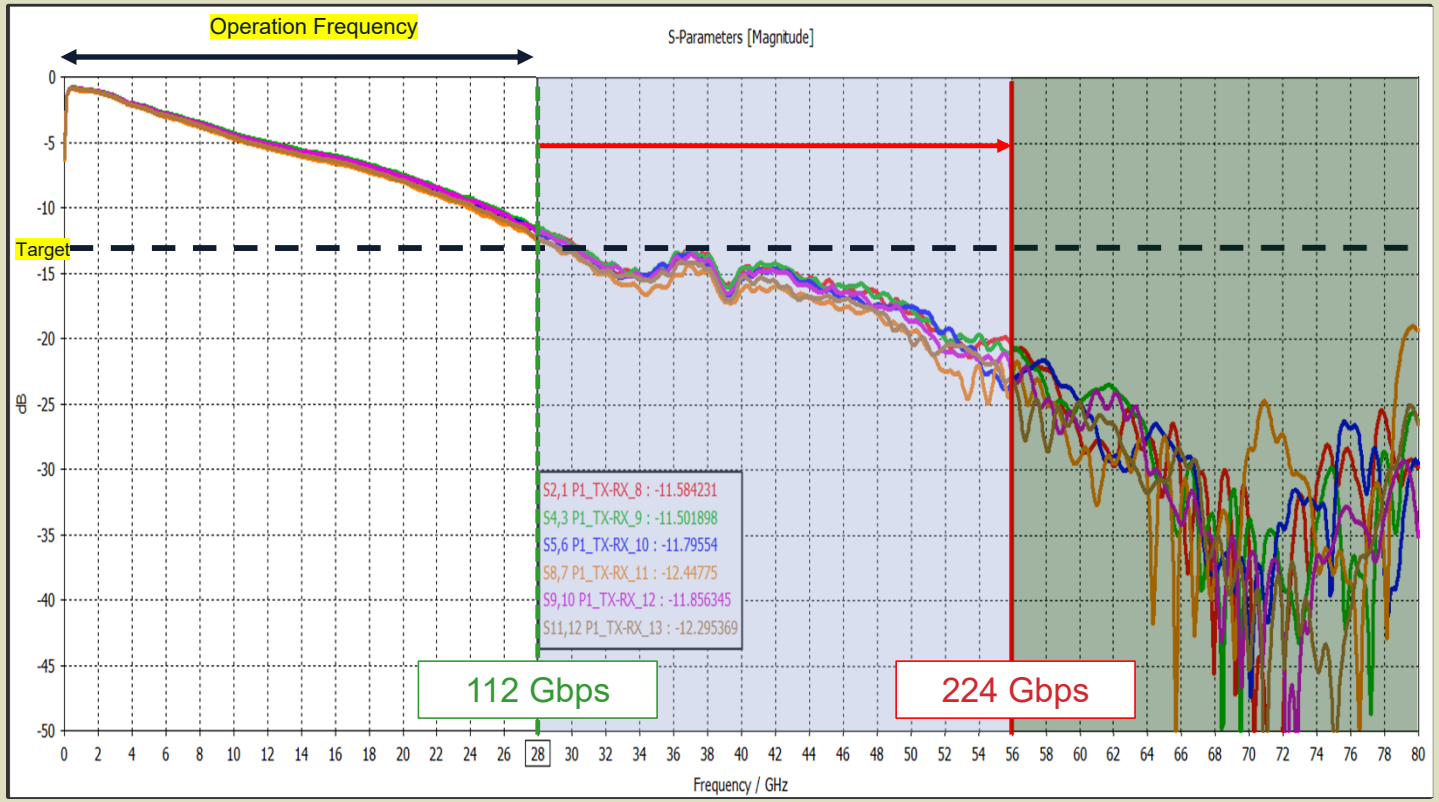
Let's start with a 112 Gbps Load Board

- Six routing layers in a single lamination design
- Uses impedance controlled vias with back-drilling
- Loopback through a bias tee
- 85 Ω differential signals

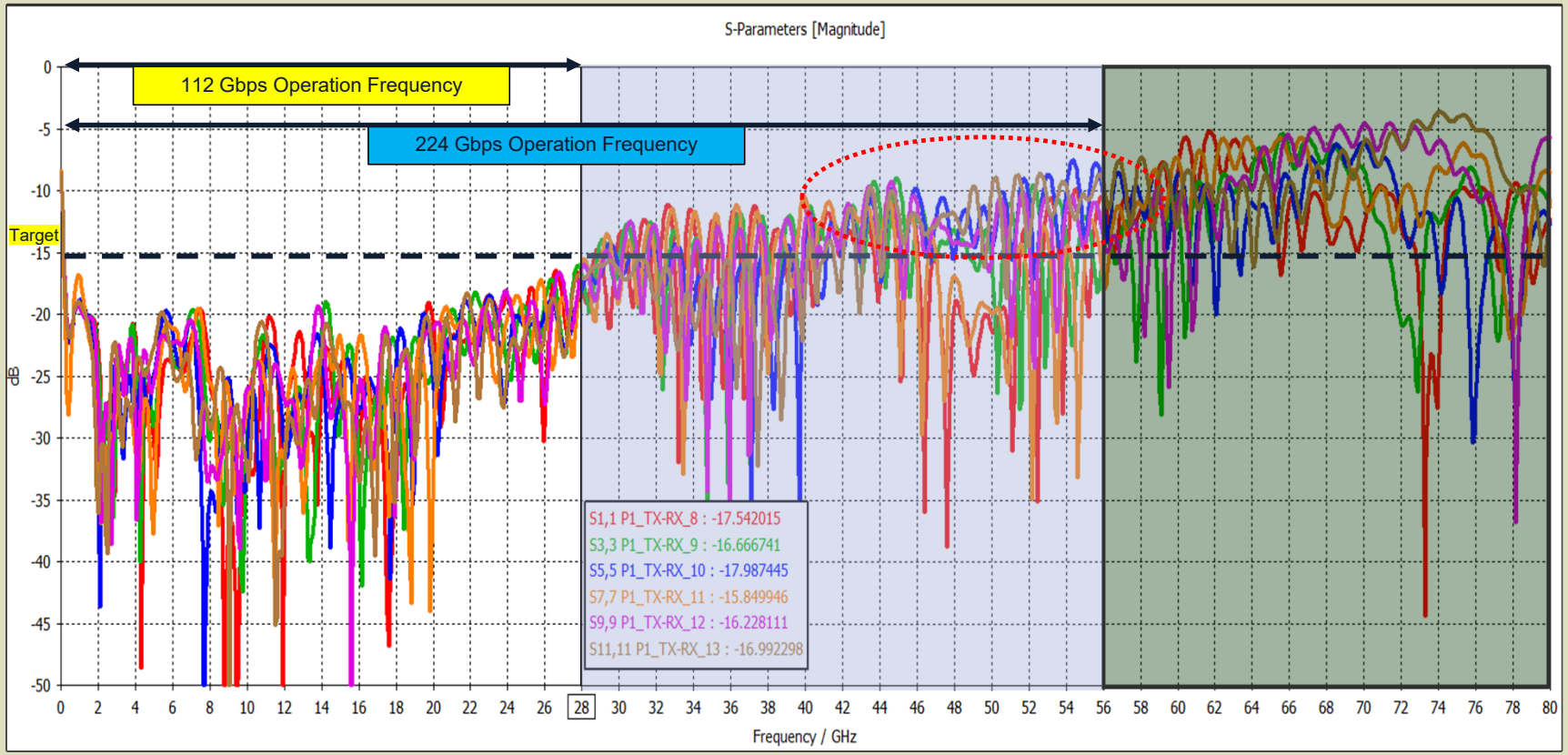


112 Gbps PCB Measured Insertion Loss

- Insertion loss target was -12 dB at 28 GHz
- Good grouping of signals
- Consistent performance up to 32 GHz
- Performance drops off after ~35 GHz
- This is due to the PCB vias and the test system

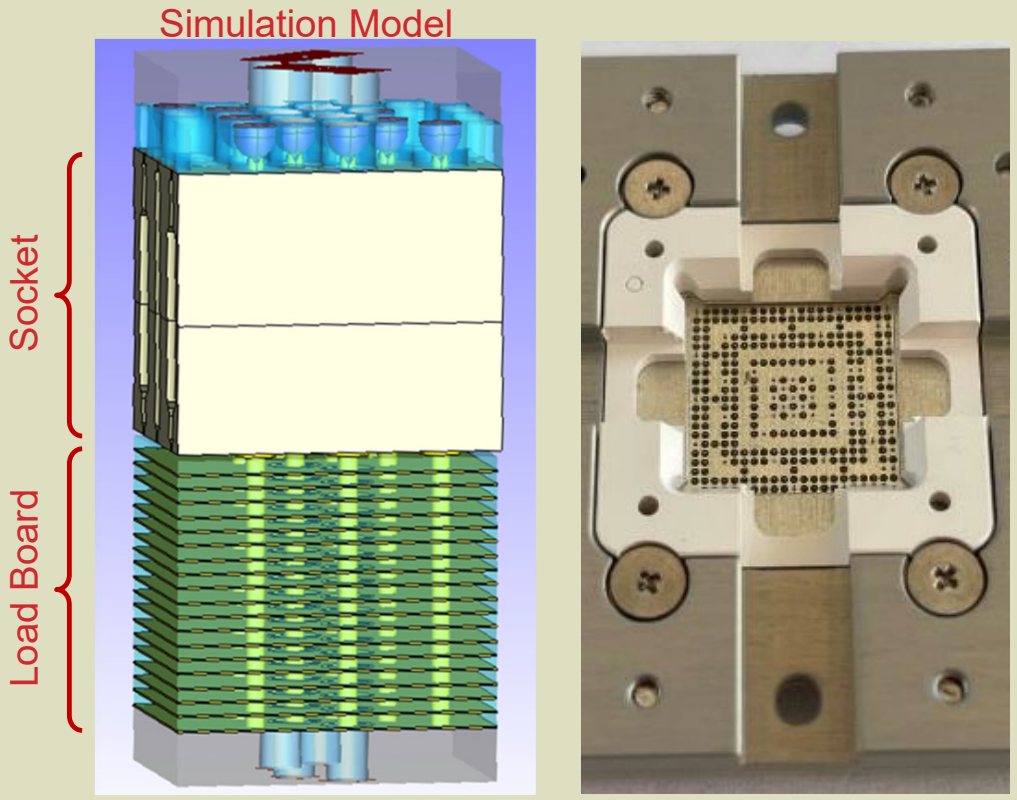


112 Gbps PCB Measured Return Loss



224 Gbps Socket

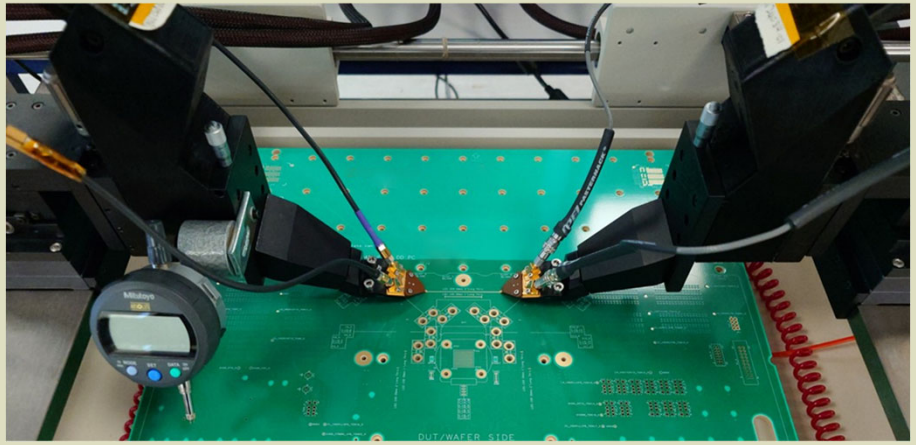
- Strongly recommend coax or elastomer sockets. This gives us:
  - Consistent bandwidth
  - Multiple impedance options (*e.g. 100 Ω and 85 Ω in one design*)
  - Reduced crosstalk
- Socket simulation needs to be integrated with the load board
- Strongly recommend that a single party is responsible for both the socket and the load board

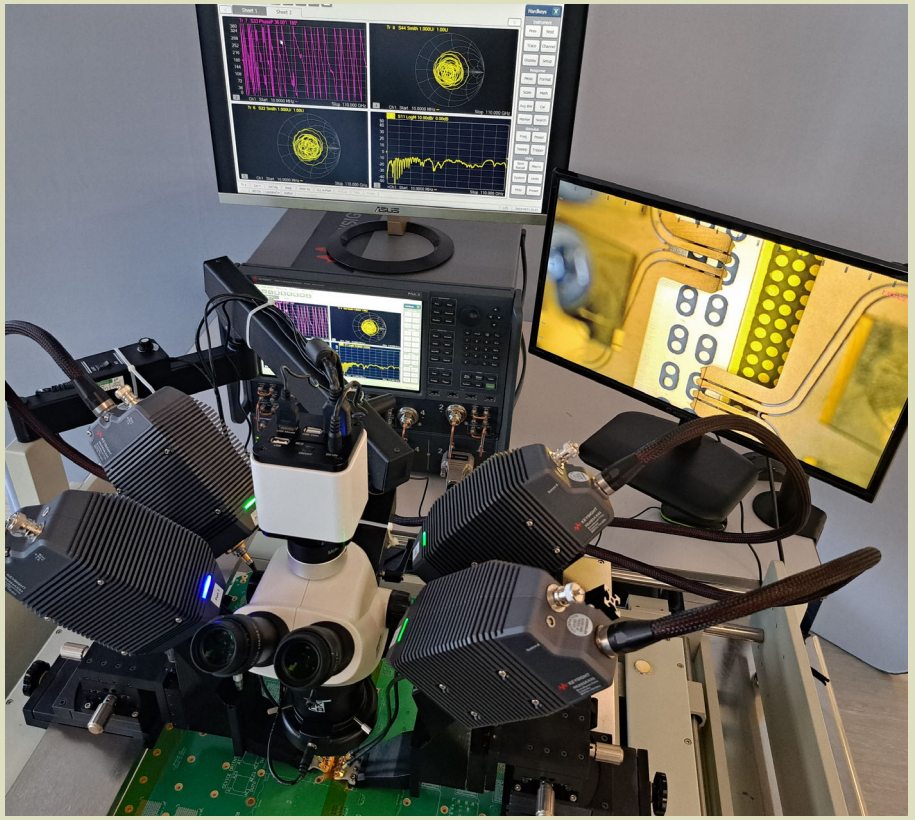


224 Gbps Evaluation PCB: Test Setup

Test Configuration

- 4 Port VNA
- IFBW = 3kHz
- 1mm cable to NuvoRF probe
- 4 Port @ 70 GHz
- Calibration to the end of the 1.0 mm cable

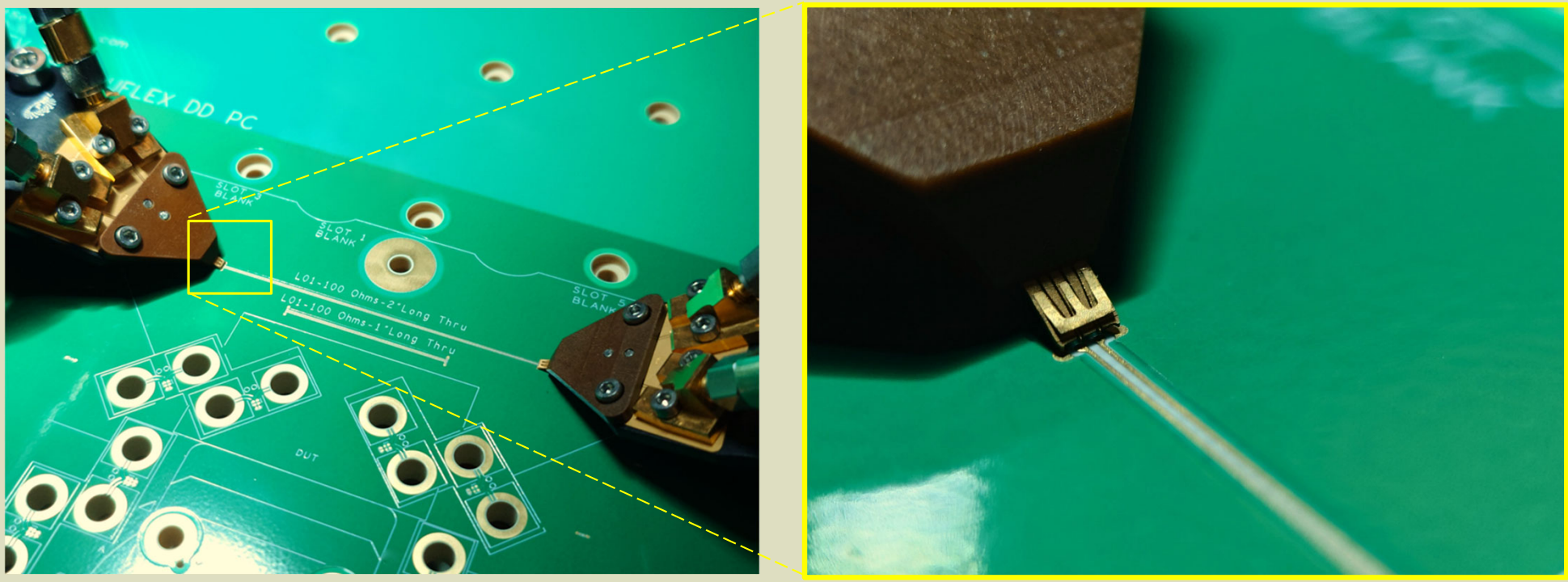




224 Gbps Measurement Challenges

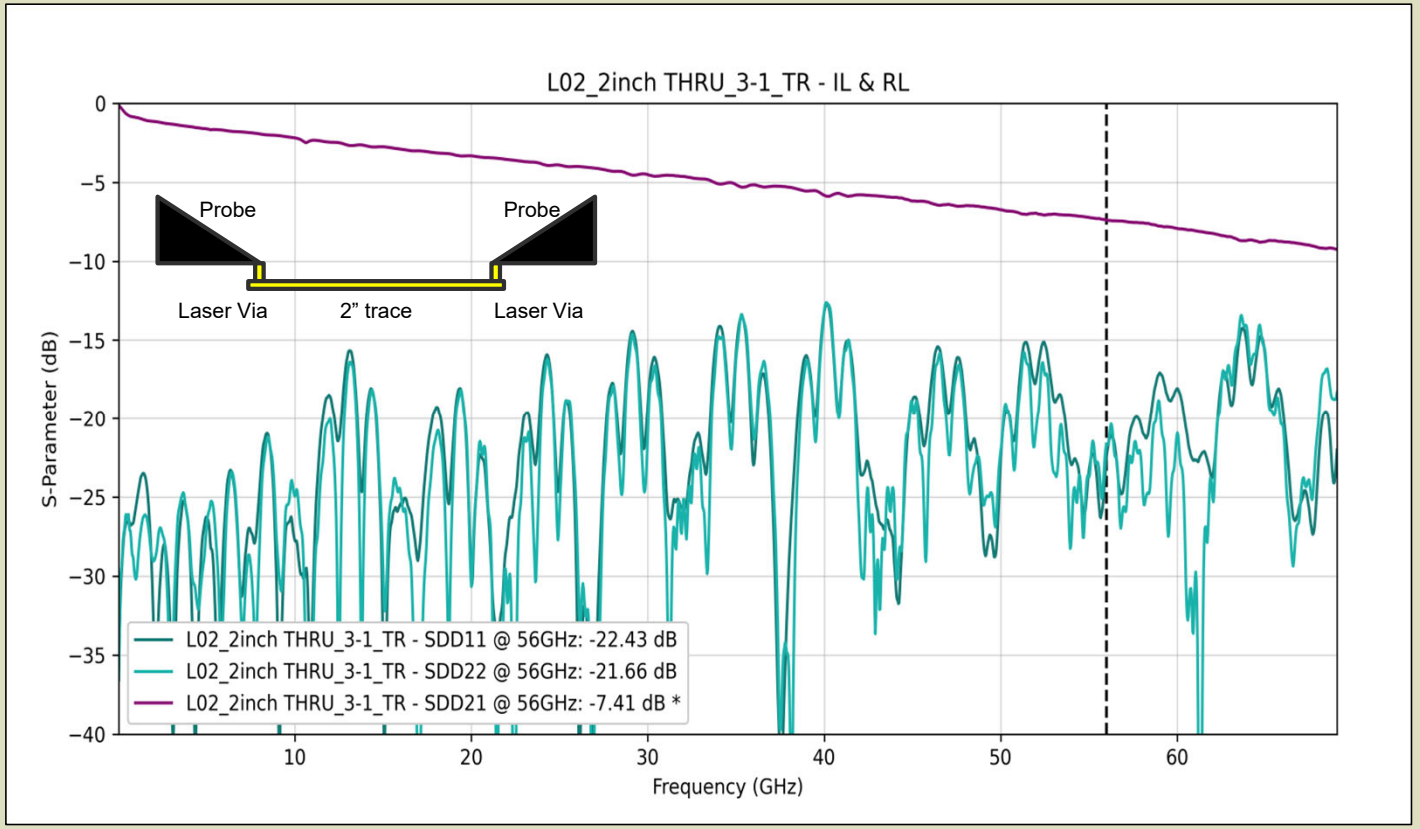
- We didn't find a 70 GHz differential probe available in the market – so we made our own
- Hard to get accurate measurements when measuring 85 Ω or 92 Ω differential with a 100 Ω measurement system
  - Gating, calibration, or de-embedding pose problems for 100 Ω to 85 Ω measurement environments
  - Need a custom probe to solve this challenge
  - Need 85 Ω or 92 Ω calibration substrates to match the circuit impedance

224 Gbps Evaluation PCB:
PTSL NuvoRF 224 Gbps GSSG 500 Probe



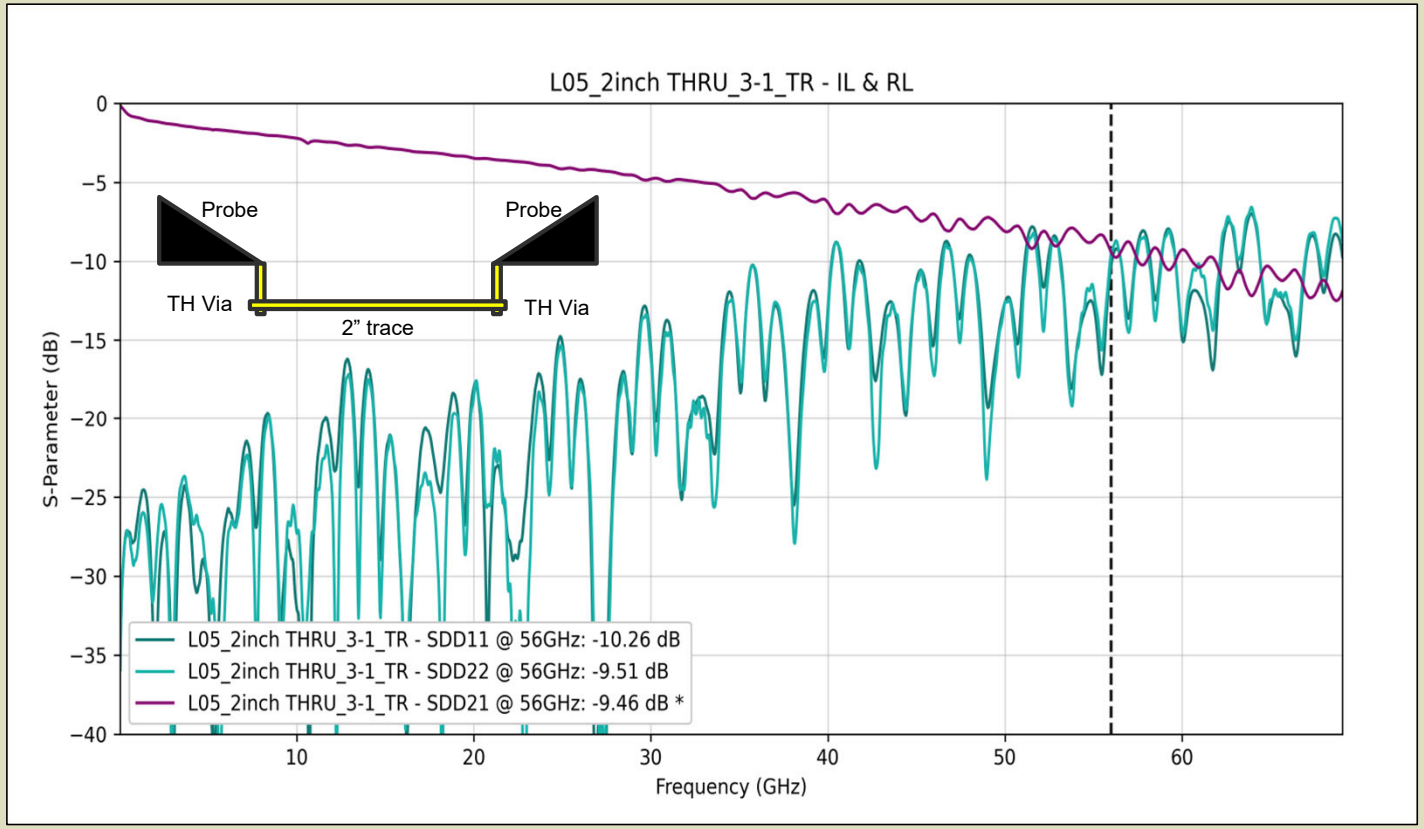
224 Gbps Evaluation PCB: Laser Vias

- Probe performance is excellent
- 100 Ω environment
  - Need measurement solution for 92 Ω (In progress)
- This is good for 224 Gbps (>56 GHz)
- Note: No loopback circuit



224 Gbps Evaluation PCB: Through Hole Vias

- Through hole via shows problems around 40-50 GHz
- This is not good enough for 224 Gbps
- Special focus is required for through hole vias



Conclusions

- Standard via tuning is not good enough. A special via structure is needed to get to 56 GHz / 224 Gbps PAM4
- The best loopback strategy has yet to be identified
- Measuring this is difficult
  - 85 Ω or 92 Ω requires special tools and techniques
  - 56 GHz large pitch differential is especially challenging

Special Thanks

- Robin Cedeno
- Ross McMillan
- Tim Rey

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