Signal Integrity and Power Integrity Test Hardware Design Requirements, Challenges for low voltages high performance SOC

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Contents

- Power Integrity Challenges of low voltage devices for multi-site Test load boards.
- Signal Integrity Impact of small pitch packages high performance SOC.
- Multi-IP provider on a single SOC.
- Noise floor management and sensitivity for Digital and Mixed-Signal devices.
- Recommendation, Conclusion.

Critical details for low voltage SOC

- Supply voltage levels trending down to 0.76V, 0.60V….
- The 5.00 % of 0.76 V is 38.00 mV.
- The 5.00 % drop of 15.00 A supply is 2.50 mΩ. Single digit impedance for major IPs such as VDD-Core, DDR, Analog Block.

Power delivery for low voltage SOC

- Power plane design, layout and geometries.
- Power plane design for multi-site load board.
- Power filter design, components, and placements.
- Power Connector specifications and precisions in time domain and frequency domain.

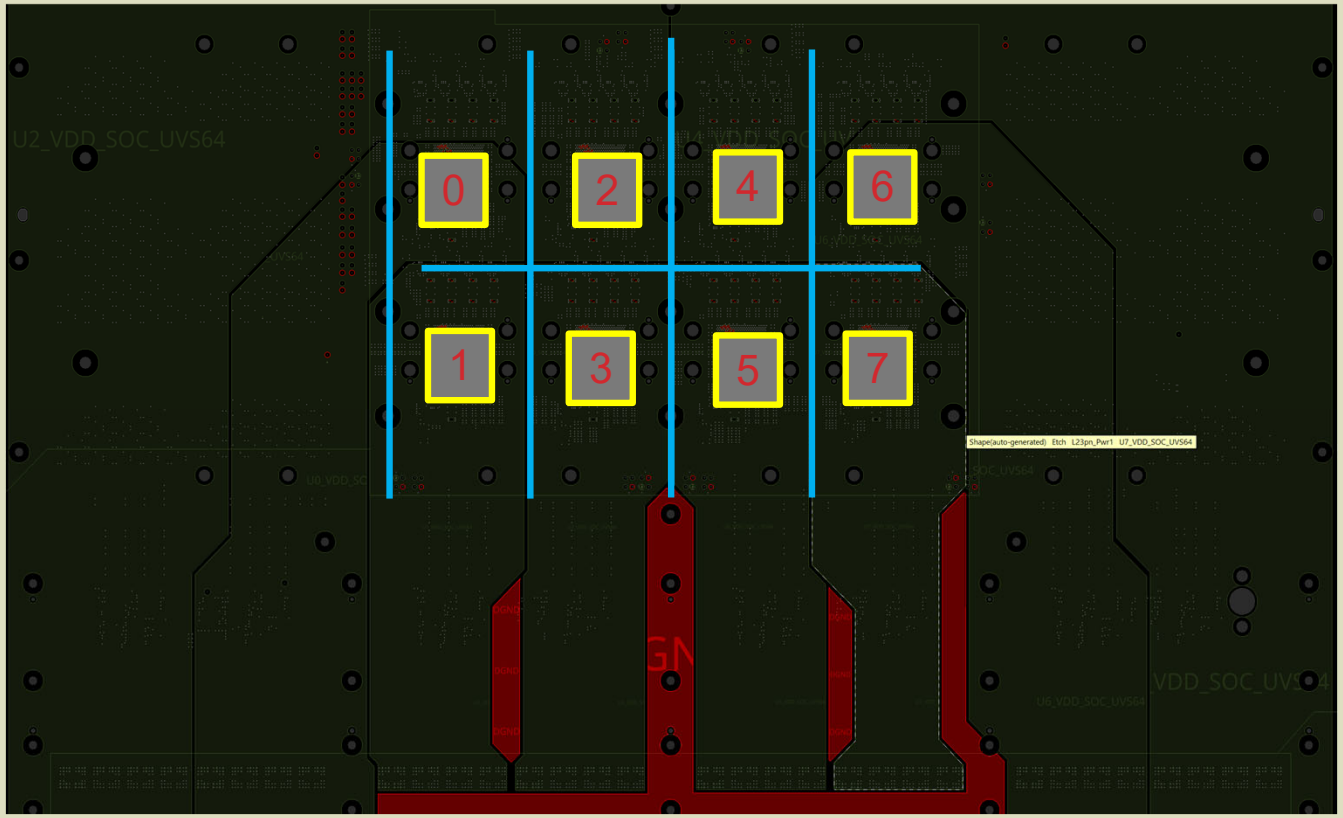
Power Integrity challenges for low voltage SOC

Test Issues related to power distribution

- Site to site correlation on high current, high performance IPs (e.g., di/dt for Core, DDR, Analog Block).
- IP signal a noise to another IP.
- Cross-talk: Site signal a noise to another site.

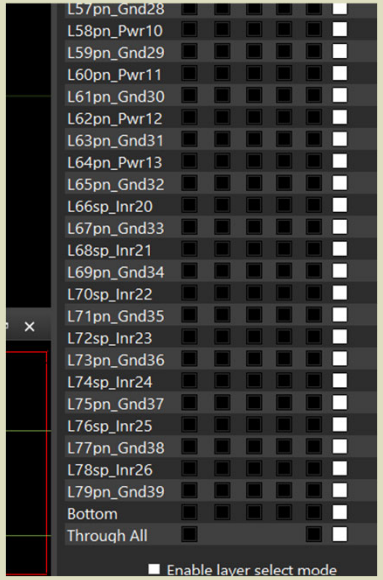
PCB Design Solutions for low voltage SOC

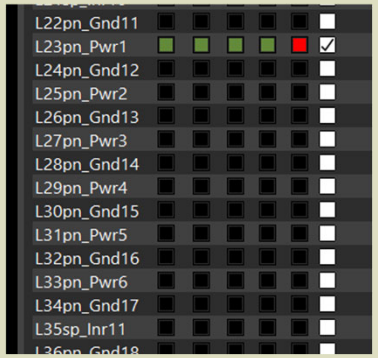
Power Plane for low voltage SOC

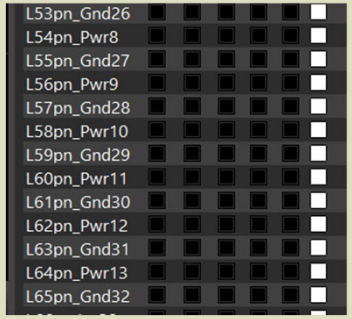


- Critical Geometries to ensure correlation between sites.
- ATE Symmetric instruments layout per associated sites.
- The entire power plane is used for a single DUT power, VDD.
- Additional layers for power distribution.

Additional power layers for low voltage SOC





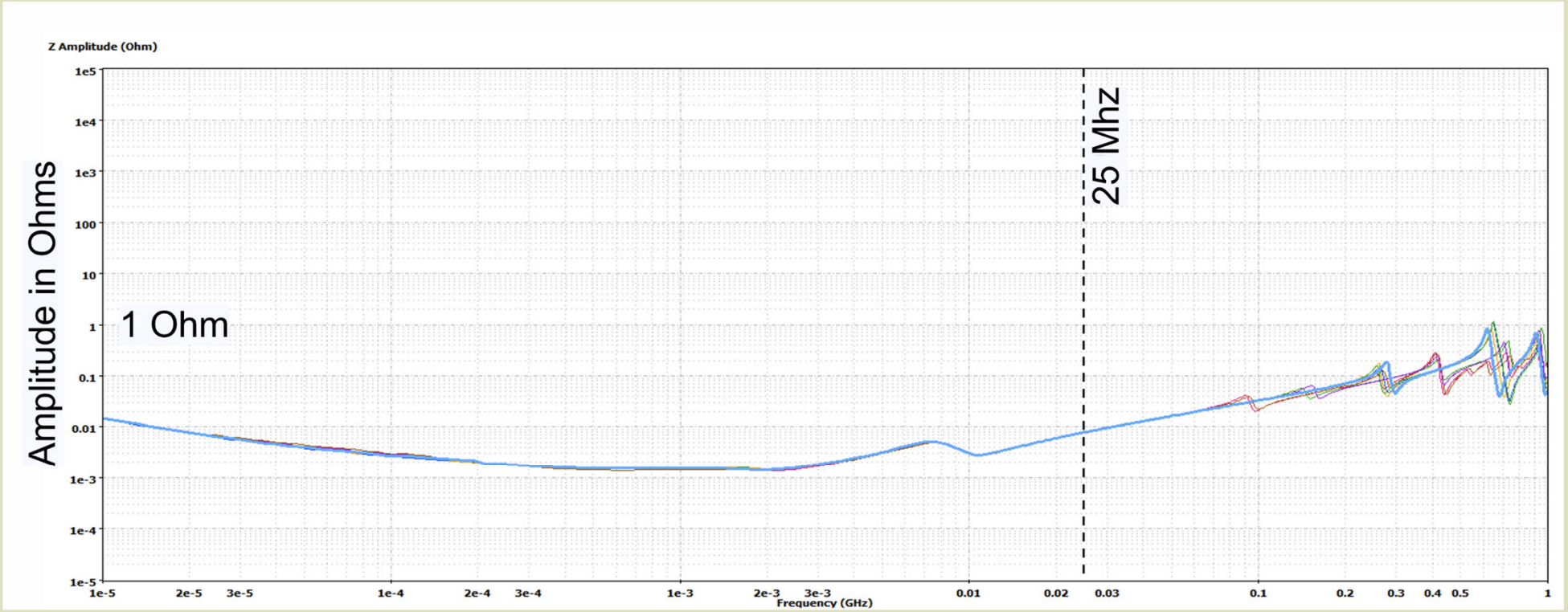


The need for more power plane layers

- Power delivery requires precise power plane design.
- Additional layer count is inevitable.
- Electrical, mechanical complexities associated with thick boards.

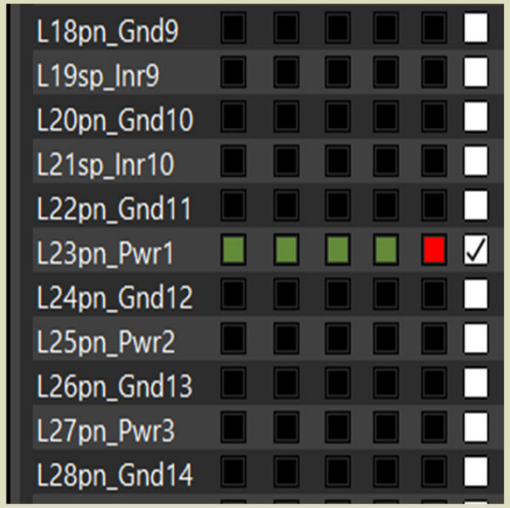
80+ layer PCB

Eight(8) sites SOC VDD PDN



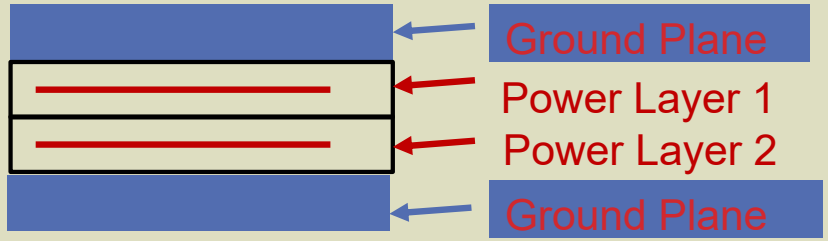
Frequency GHz

Sound Engineering on PCB Stack Up

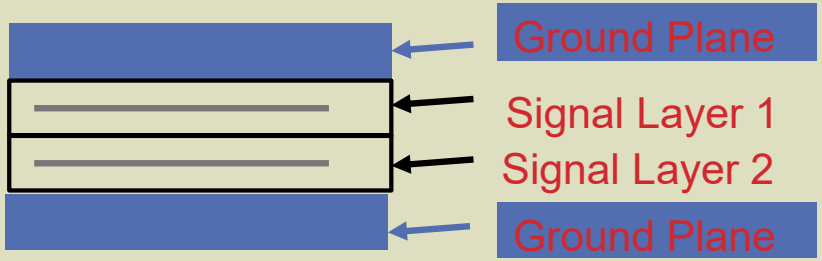


- **Eliminate all sources of cross talk or undesired coupling.**
- **IP to IP crosstalk**
- **IP-Power to IP-power crosstalk**

No Double Stacking of Power Layer



No Double Stacking of Signal Layer



Signal Planes In between Ground plane

Power Planes In between Ground plane

Signal Integrity Sensitivity on small pitch and low voltage SOC

Intricacies of Small Pitch Packages , Multi-Ip low voltage high performance SOC

- Inductive physical circuits on transmission line segment interface is common. Focus on hardware integration is a must to avoid SI issue as a function of frequency.
  - Small board pads.
  - Small diameter socket pins.
- Physical 3D modeling of hardware integration is very critical.
- Board Geometries, Structures, over all thickness is predicated by package pitch.

Intricacies of Small Pitch Packages , Multi-Ip low voltage high performance SOC

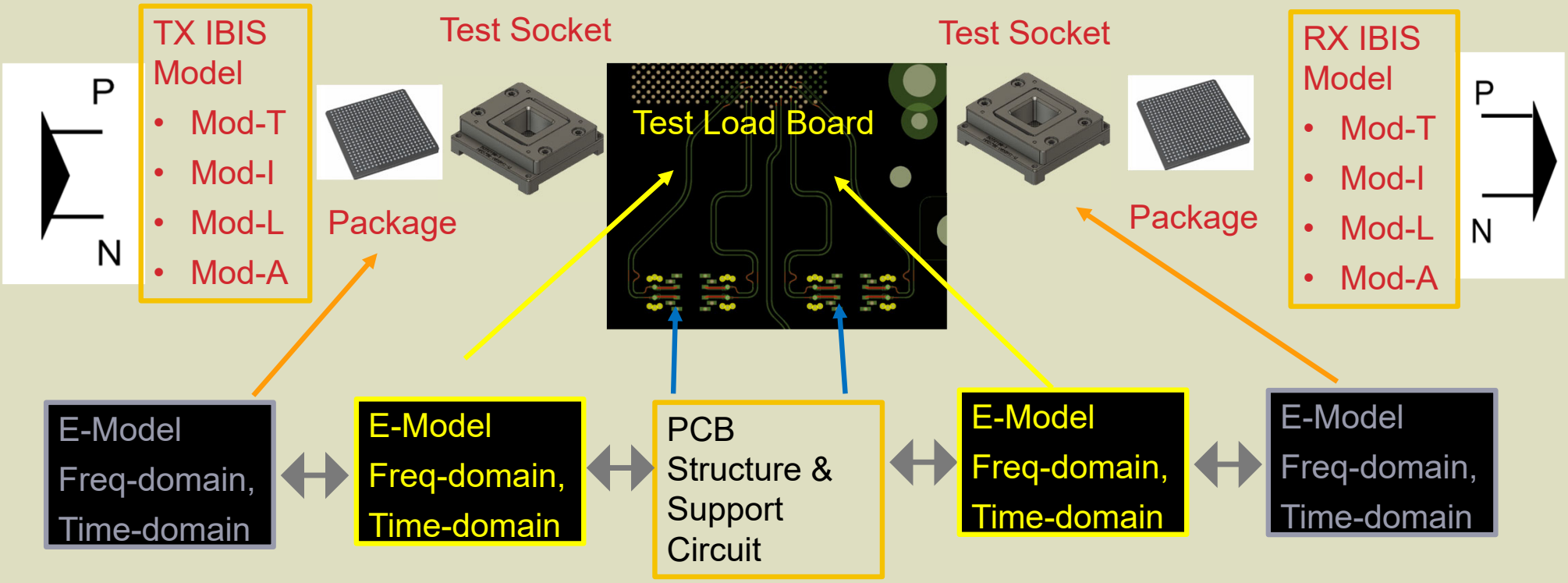
- IP specific Impedance (e.g. Differential Impedance-> PCIE=85 Ω, DDR=80 Ω, USB=90 Ω, STD I/O 100 Ω).
  - Standard Single Impedance Socket.
  - Coaxial Single Impedance Socket.
  - Coaxial Multi-Impedance Socket.
- Type of Pin, & Pin-Tip Design.
- DUT Grid surface design, structure becomes complicated as a function of socket technology.

Multi-IP
on small pitch and low voltage SOC

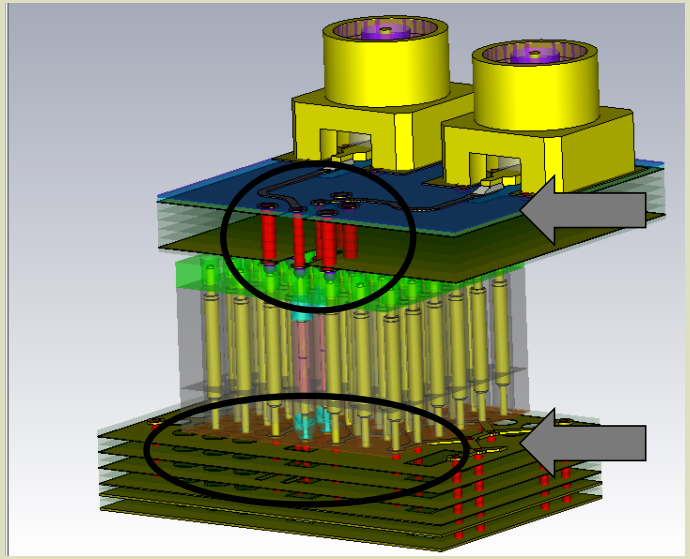
IP specific Impedance

IP Type	Model	Impedance (Diff) (Specifications)	Data Rate	Modeled, Simulated best results Impedance range
PCIE	T	85 Ω	16 Gbps	85 Ω to 90 Ω
DDR	T	80 Ω(40 Ω SE)	8 Gbps	90 Ω to 100 Ω
Ethernet	I/A	85 Ω 100 Ω	16 Gbps	85 Ω to 90 Ω
PCIE	I/A	85 Ω	10,16, 2.5 Gbps	85 Ω to 90 Ω
USB3	I	90 Ω	10 Gbps	90 Ω
DDR	I/T/A	80 Ω (40 Ω SE)	4 Gbps	90 Ω to 100 Ω
PCIE	L/A	100 Ω 85 Ω	28,32,45 Gbps	85 Ω to 100 Ω

Multi-IP SOC for function and data rate

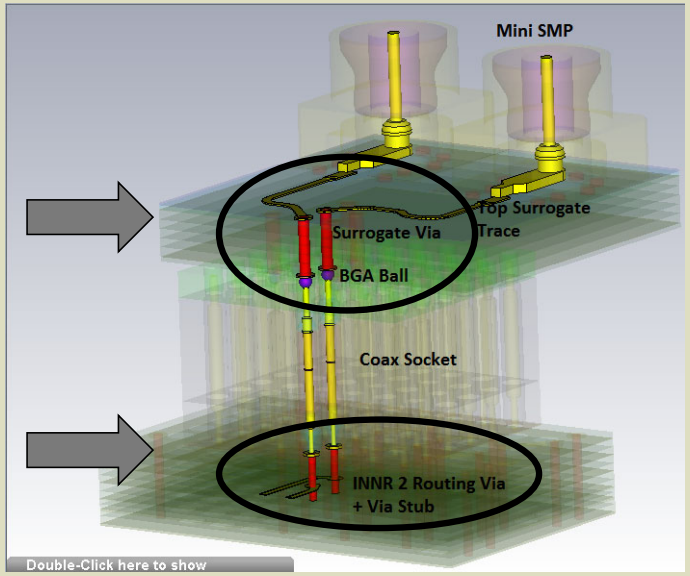


Hardware Integration,3D Physical Modeling



DUT to Socket transition

Socket to PCB transition

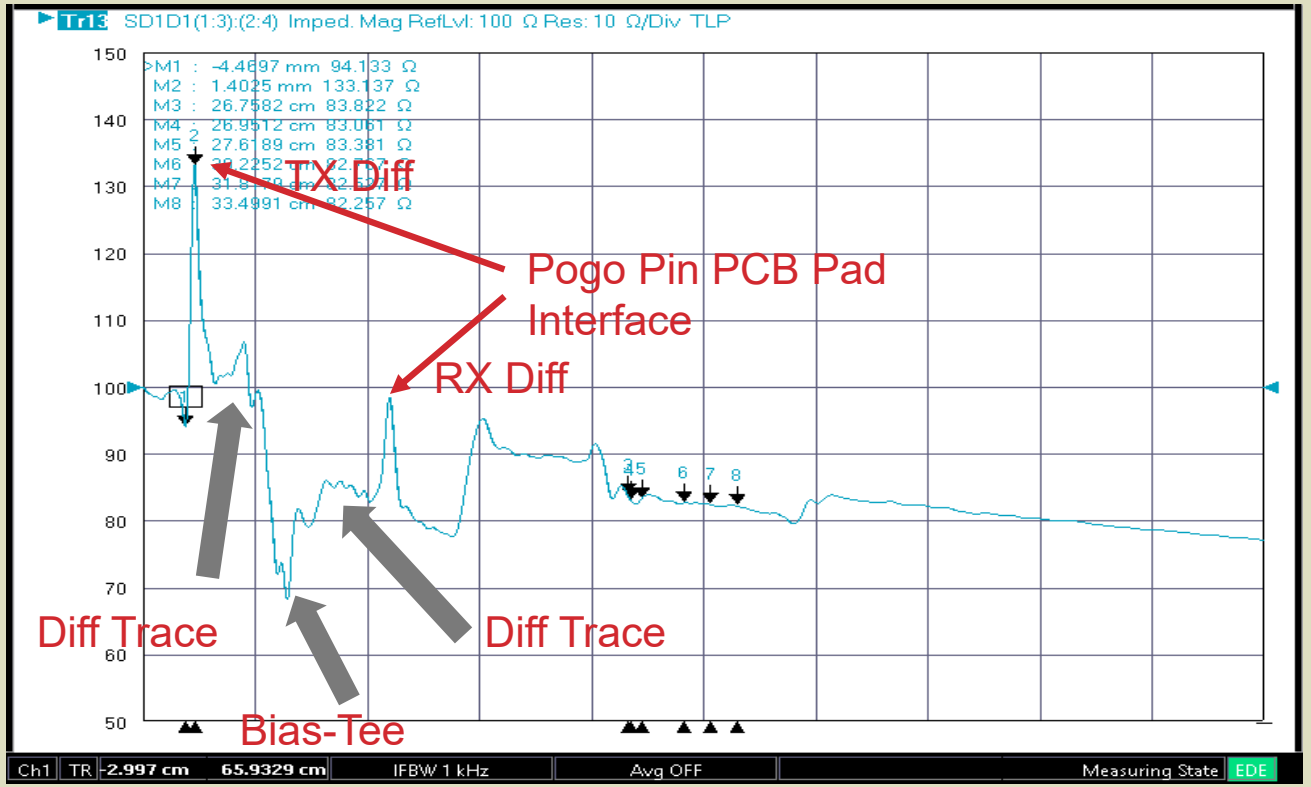


Small geometries of board pads, socket pin make an inductive interface.

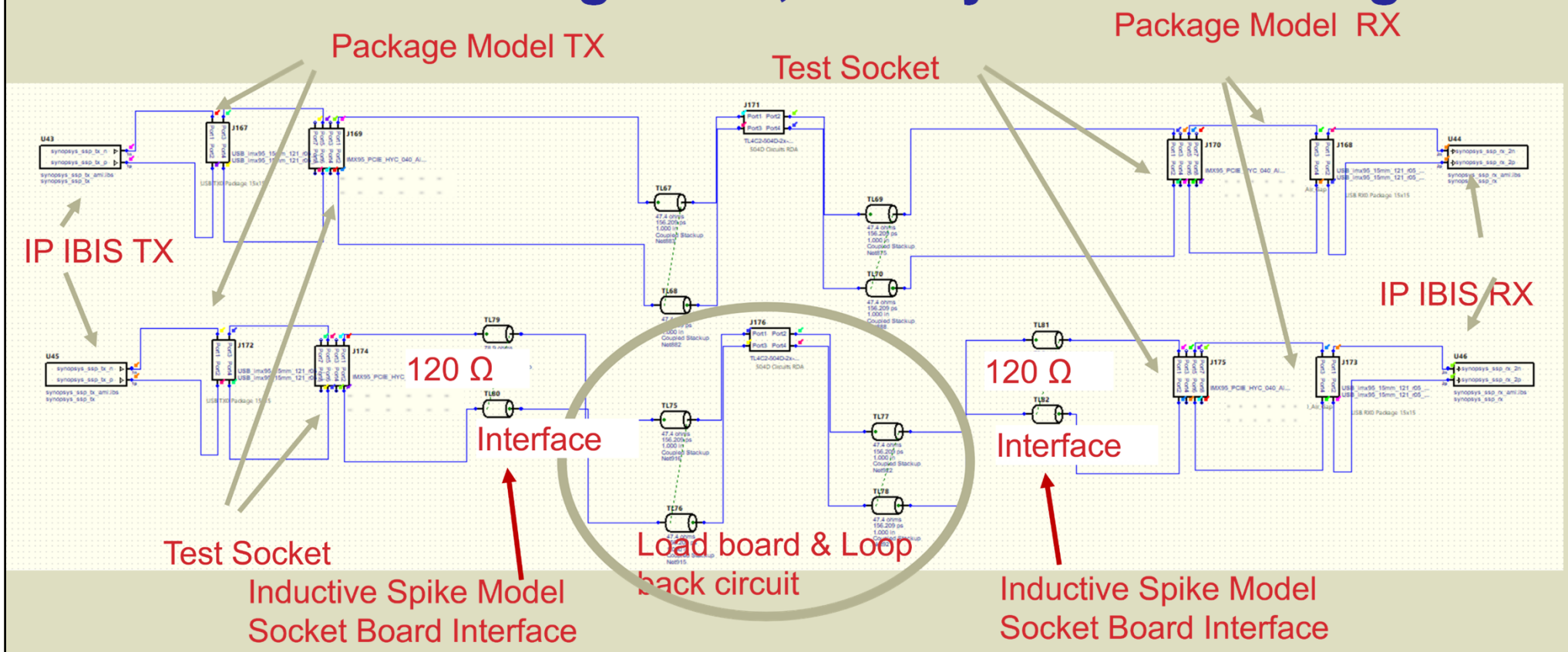
Hardware Integration,3D Physical Modeling

Observations.

1. Impedance spike ~ 33 Ω at pogo-pcb pad interface on both TX & RX
2. Return Loss above -10 dB is due to the inductive spikes.
3. High Isolation on differential P&N Leg of coax socket (little to no coupling)



Hardware Integration,3D Physical Modeling



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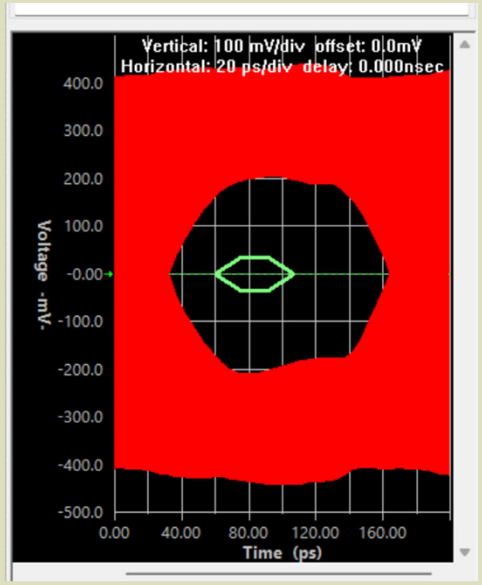
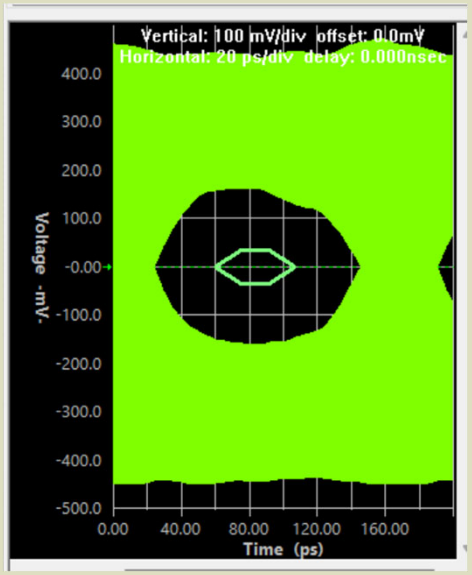
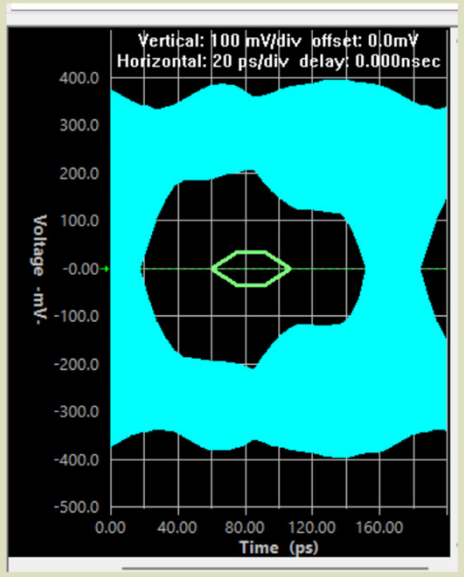
Hardware Integration,3D Physical Modeling



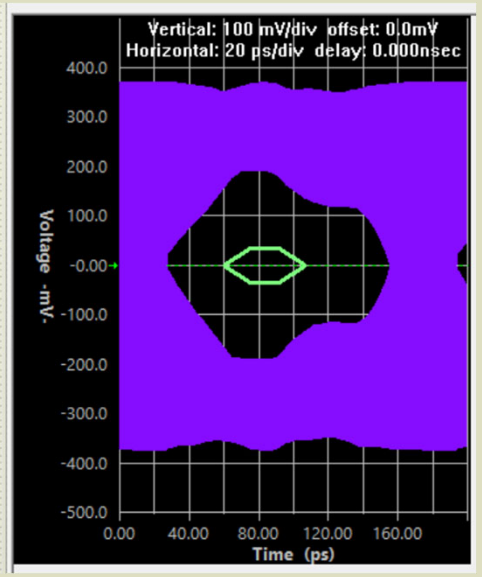
90 Ω Socket



90 Ω Socket
with 120 Ω Spike



95 Ω Socket



95 Ω Socket
with 120 Ω Spike

Data Eye deformation, degradation

1. From 90 Ω differential impedance to 95 Ω
2. From 120+ Ω inductive spike at pogo-pin board pad interface

Noise Floor Sensitivity of Multi-Ip and low voltage SOC

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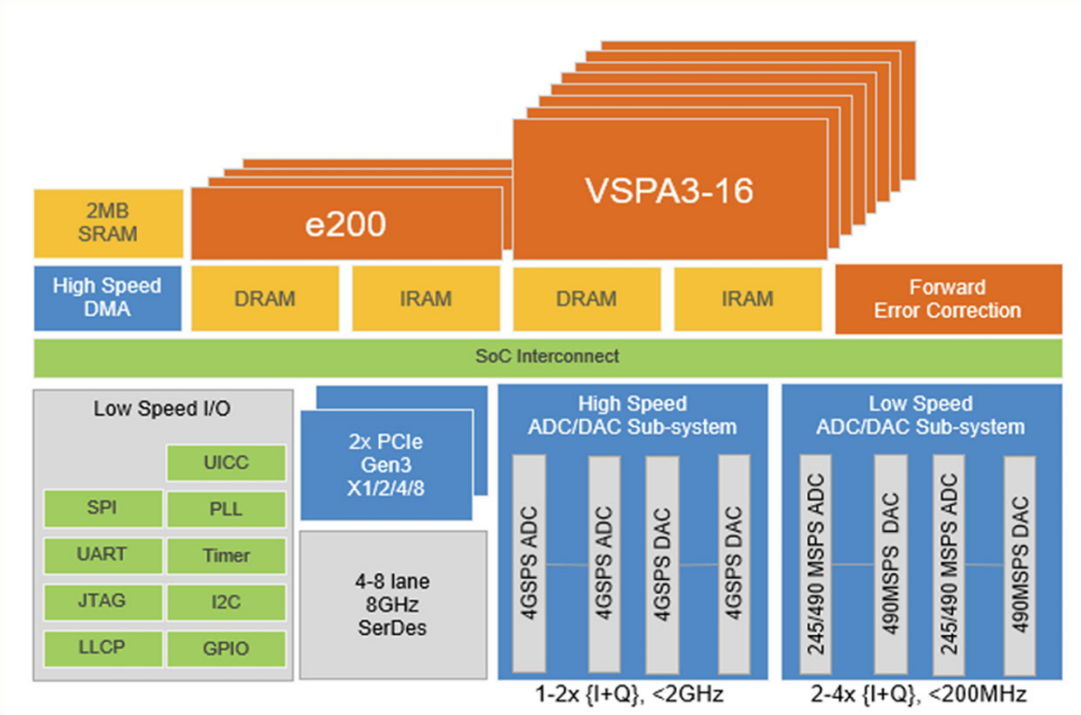
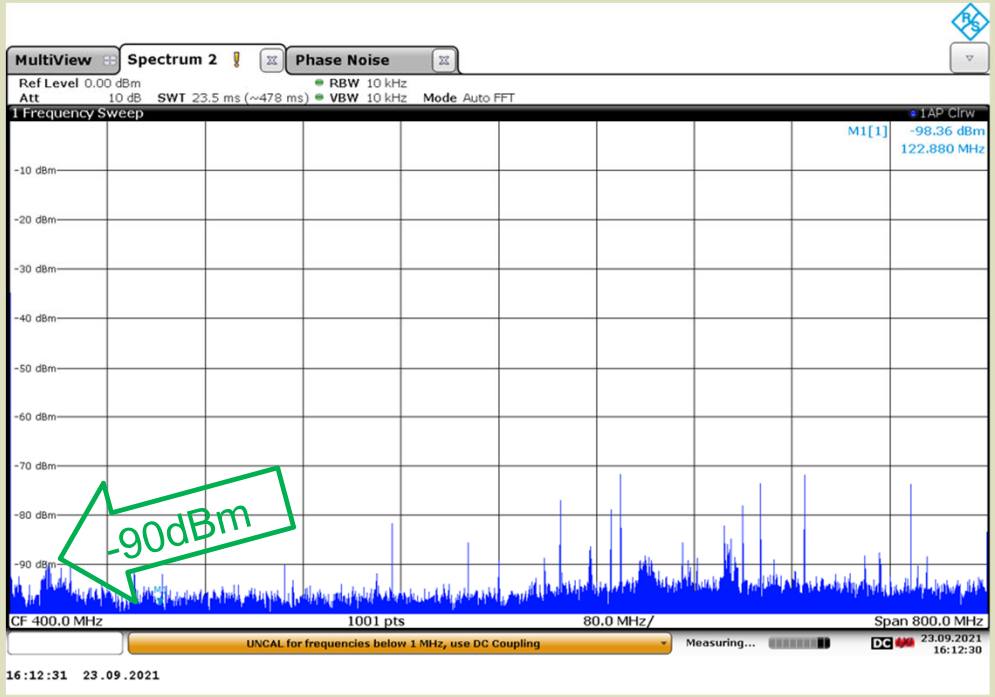
Multi IP SOC with different noise floor sensitivity



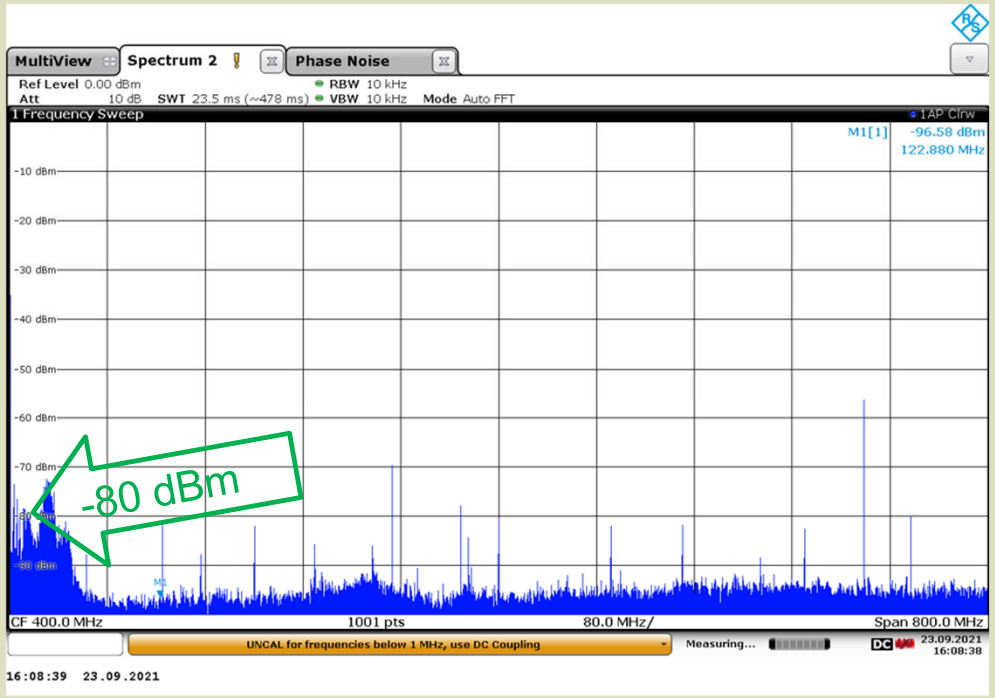
Noise floor sensitivity as a function of IP

- DGND-Digital ~ (-20dBm)
- SDGND –Serdes (-30dBm)
- DCS-GND –(-90dBm)
- Low Jitter Ref Clock – (-140dbm)

Noise Floor Sensitivity specific to each IP

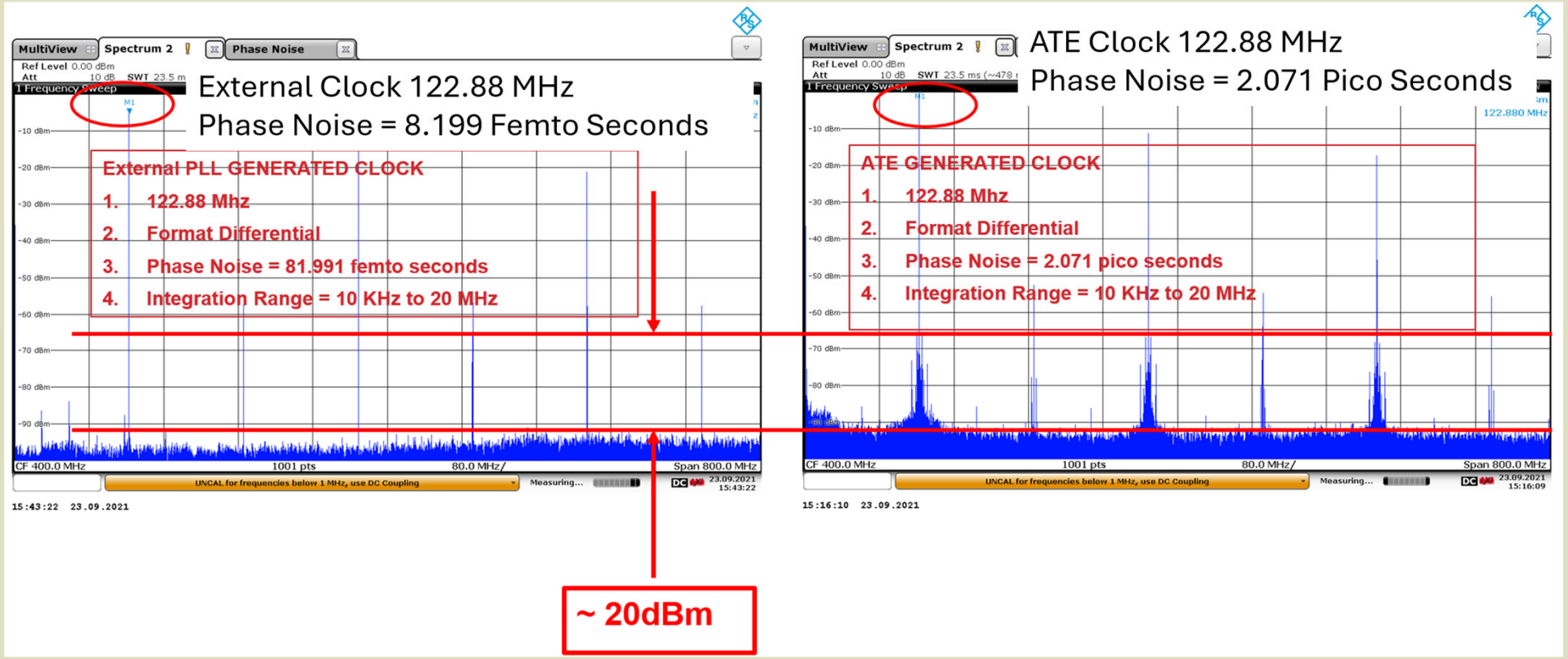


LS AGND

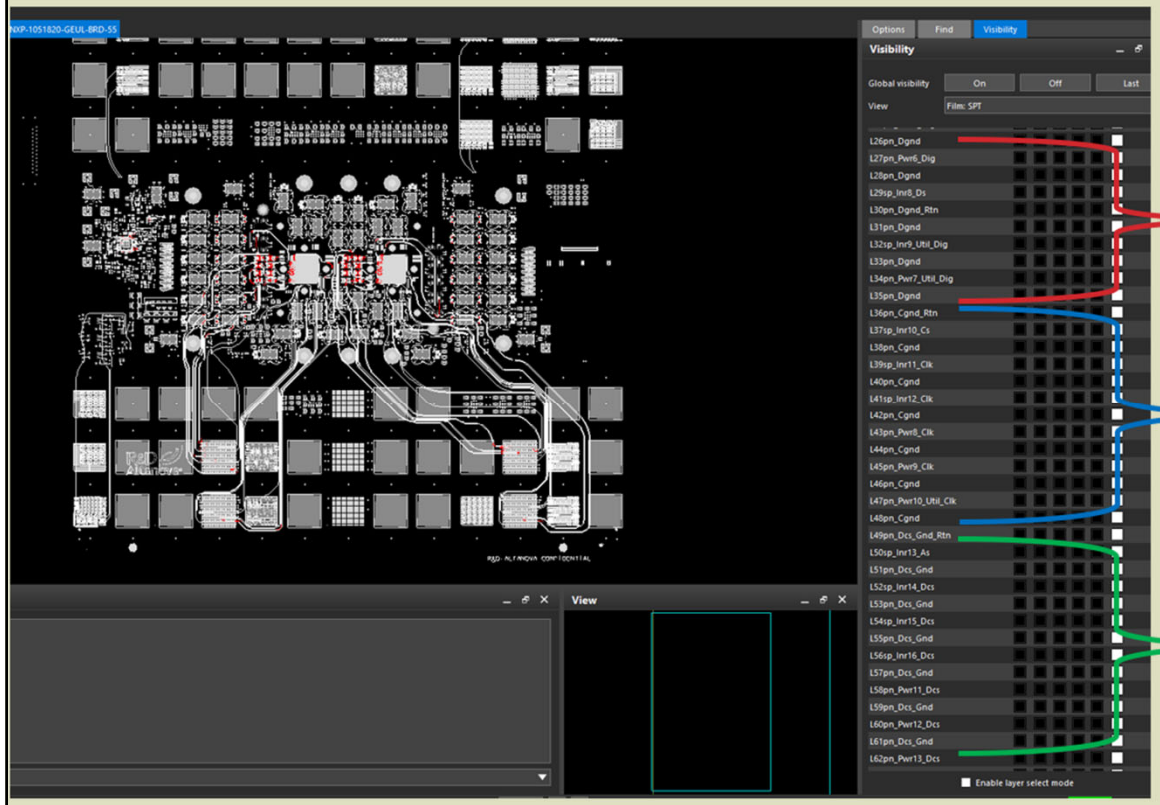


HS AGND

Noise Floor Sensitivity specific to each IP & Associated ATE Instruments



Power, Ground Management for Noise Floor Sensitive SOC



- Different power, ground domain as a function of IP.
- Consistency in ground, domain implementation.
- No Mixed-ground.
- Dedicated Power planes as a function of IP.

Solutions, Mitigation, future questions

Low Voltage High Performance SOC test hardware implementation

- High Layer count 80 Layers +, Thick PCB 300 mils +.
- Connector, socket impedance-resistance specifications will be challenged to meet single digit parameters.
- Design NRE is considerable addition to cost.
- Hardware 3D, Physical Modeling is more critical than ever. Transmission Line-segment integration is a must.
- Dedicated Power, Ground, Domain management is key to meet SI, and Noise floor requirements (Analog).
- Mechanical (50%) and Electrical (50%) aspect of the Design.

Credits and Recognition

- NXP Test Socket team (Riley Horner, Sean Young, Matthew Lauderdale)
- Hardware Development Partners
- Henry Lai, Jacob Neely

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