Vector Network Analyzer (VNA) for Hardware Transmission Line Validation

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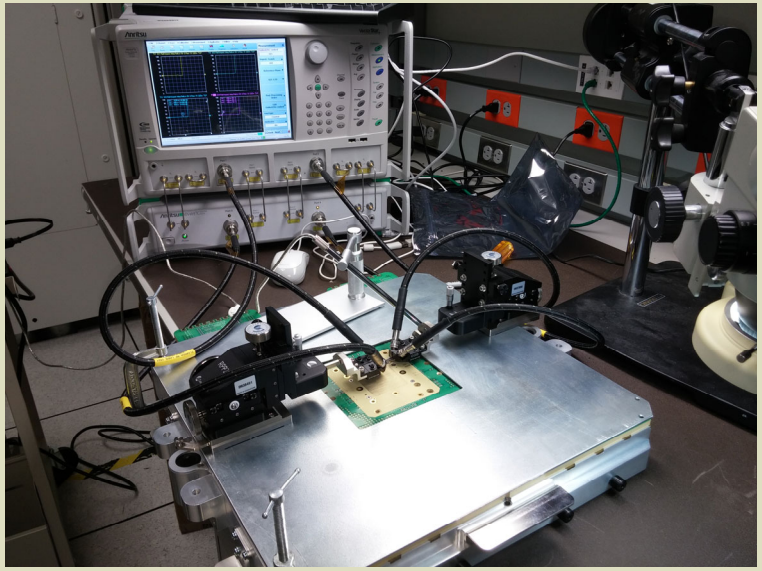
Vector Network Analyzer (VNA) for hardware transmission line validation

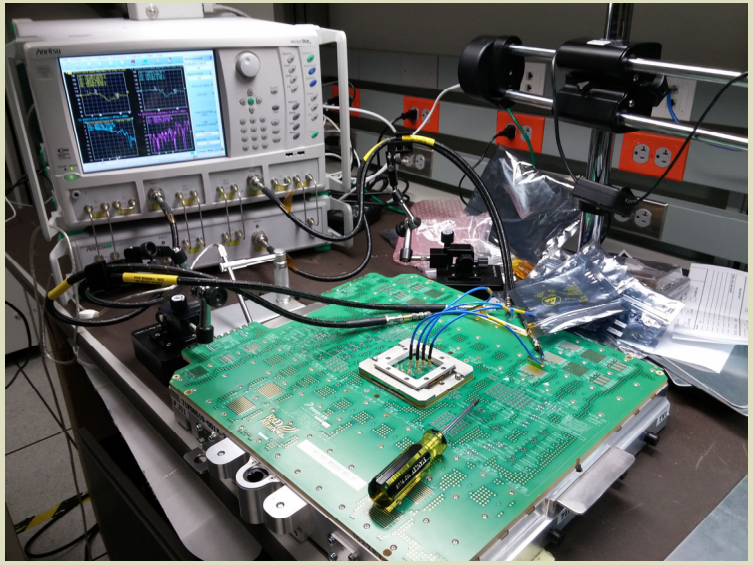
Agenda

- VNA Overview
- Time domain, Frequency domain and VNA
  - S-parameters, Time Domina Reflectometry
- De-embedding methods and techniques
- SOC with IP specific impedance requirements
- Conclusion

Vector Network Analyzer (VNA) for hardware transmission line validation



Vector Network Analyzer
Board Probe



Vector Network Analyzer
Cabled

VNA, S-parameter overview

S2D1- Differential

S21- Single Ended

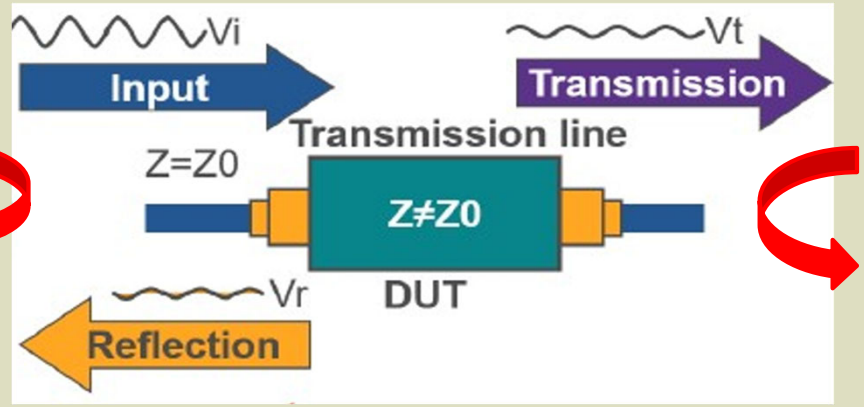
Transmission Coefficient from port 1 to 2

S2D1, S21

D2D2- Differential

S22- Single Ended

Reflection Coefficient on Port 2



D1D1, S11

D1D1- Differential

S11- Single Ended

Reflection Coefficient on Port 1

S1D2, S12

S1D2- Differential

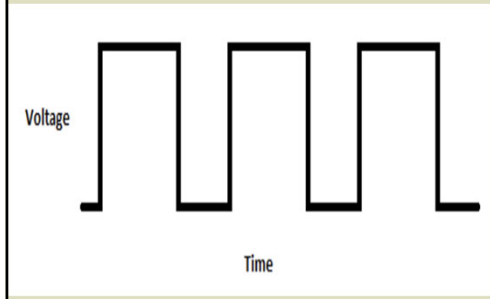
S12- Single Ended

Transmission Coefficient from port 2 to 1

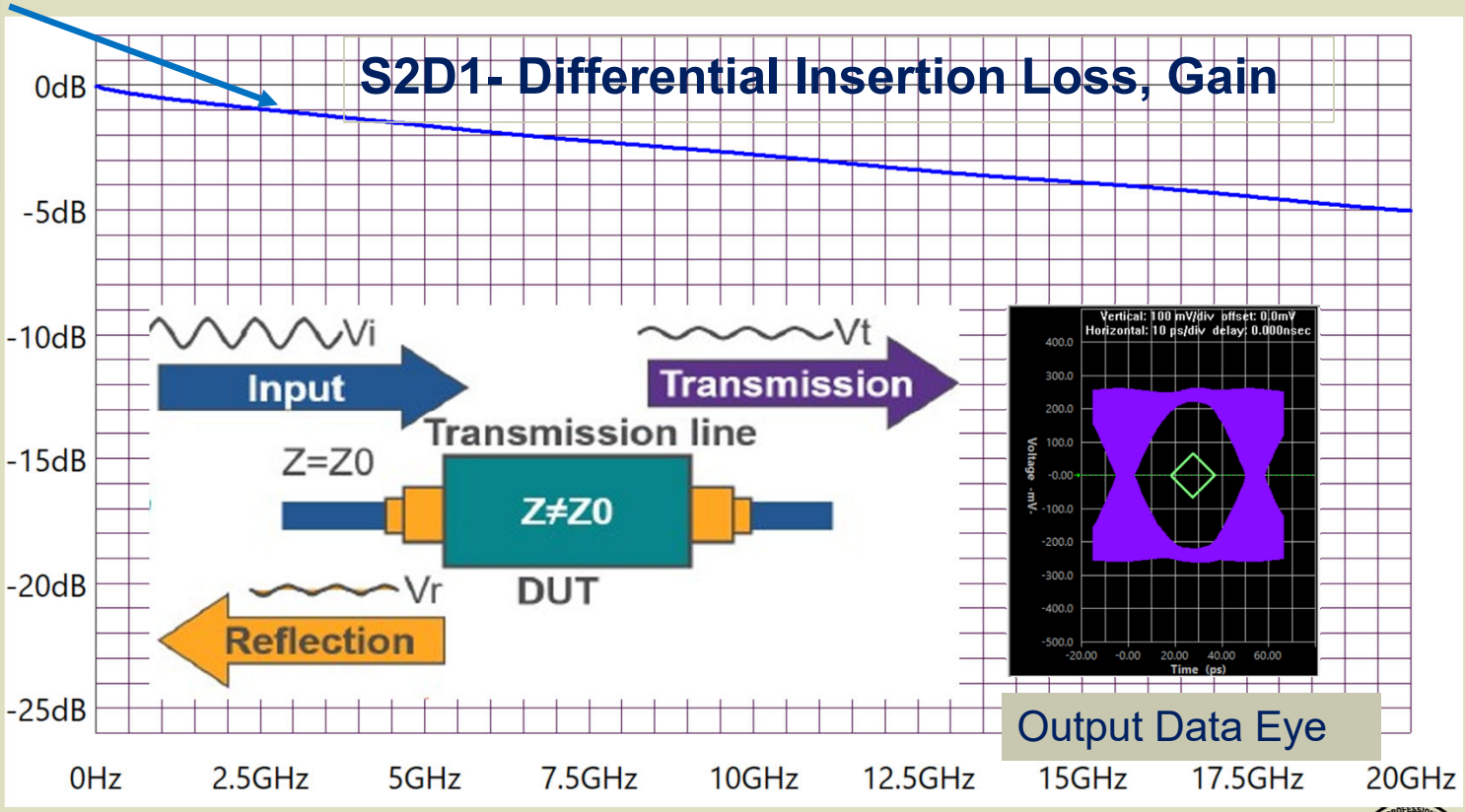
VNA, S-parameter overview

Efficient Energy transfer from input port to output port.

Linear observable curve



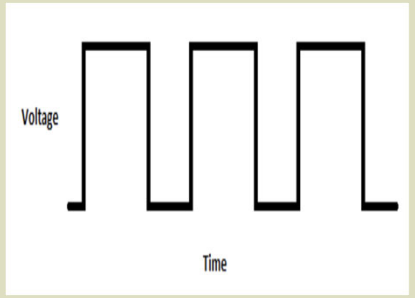
Input Signal



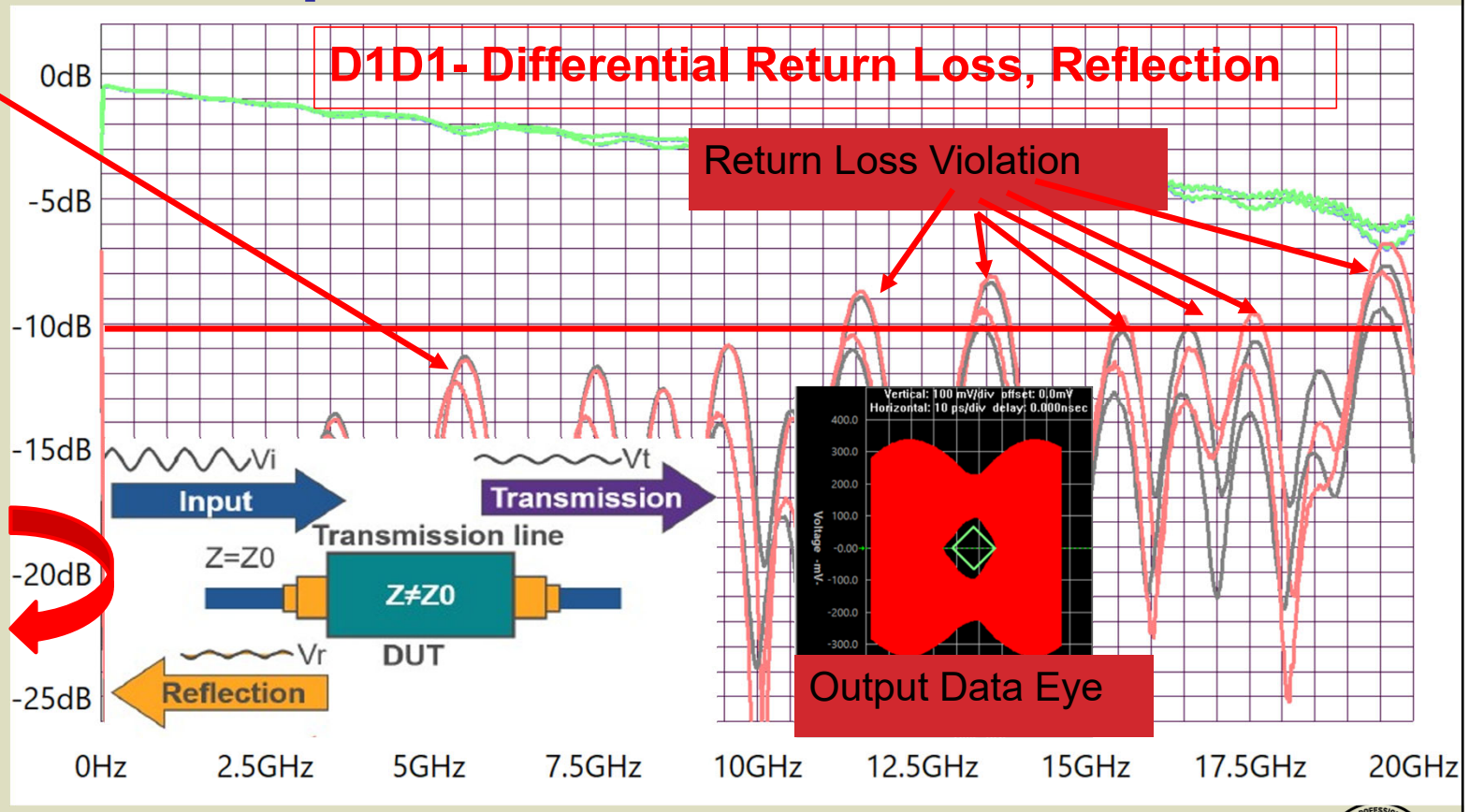
Output Data Eye

VNA, S-parameter overview

High Reflection rate
Poor Energy transfer from input port to output port.

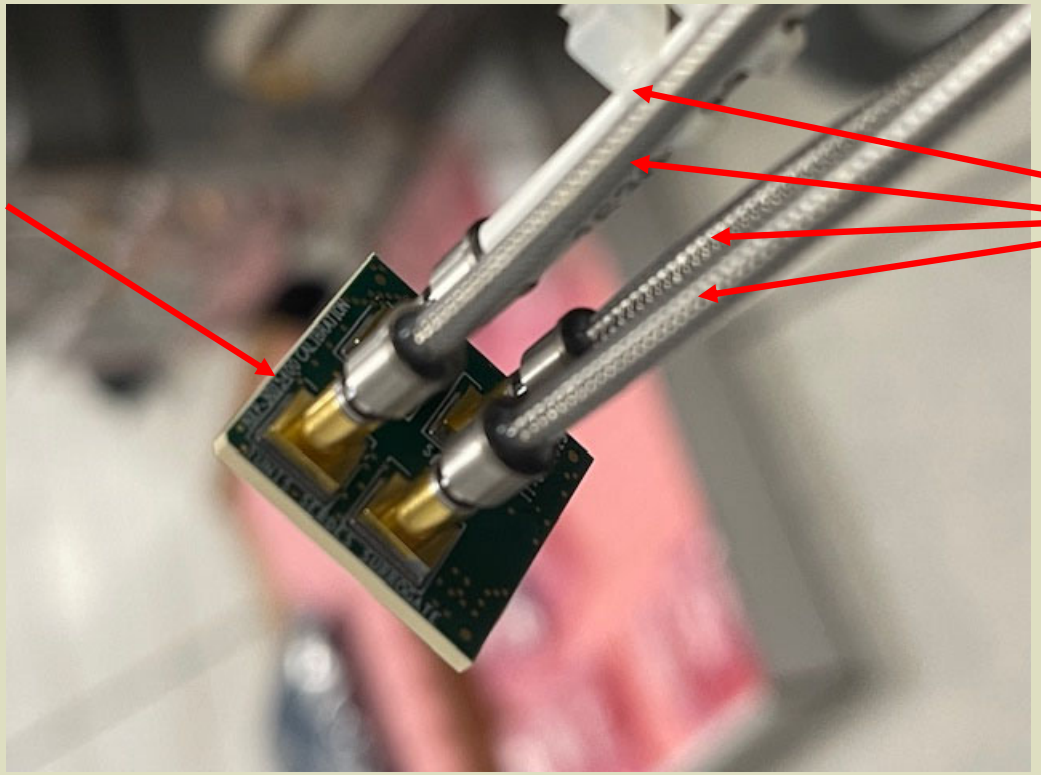


Input Signal



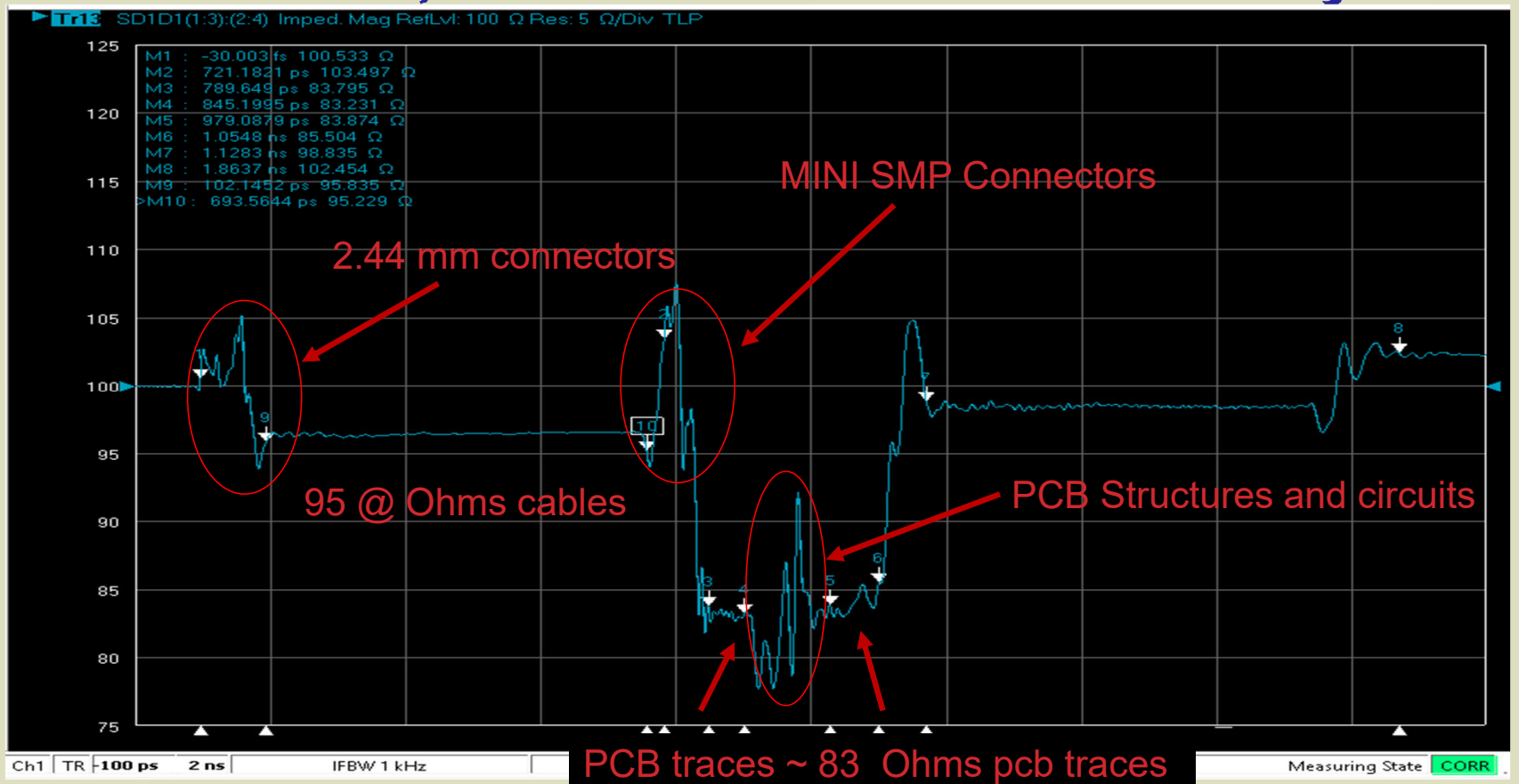
VNA De-embedding methods

Measuring fixture
(e.g. probe-package-pcb)
Differential 4-port

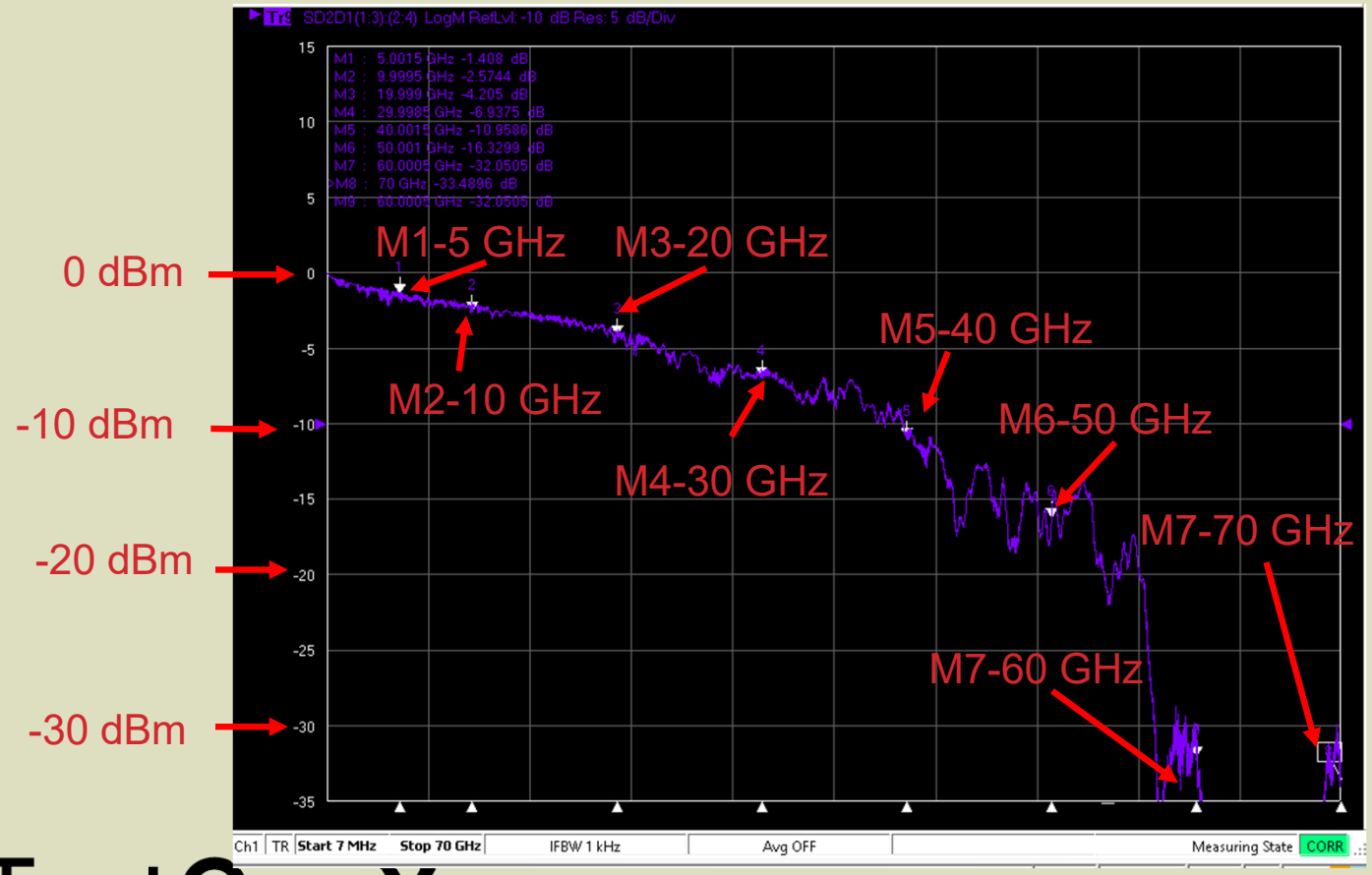


4-Port Cable
2.4mm to Mini SMP
6 Inch Cable

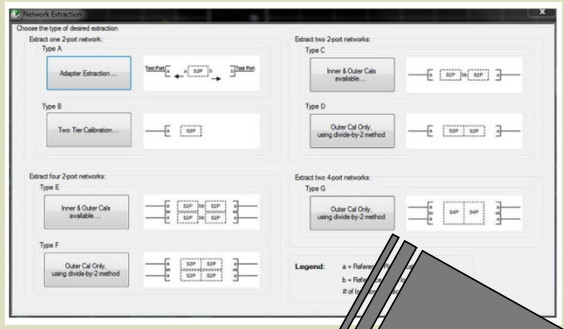
VNA, Time Domain Reflectometry



VNA De-embedding Options (Insertion Loss)



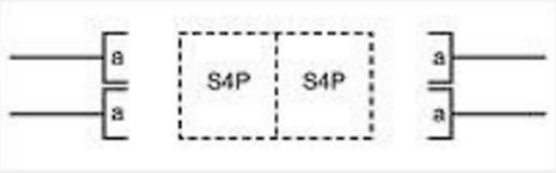
VNA De-embedding Options



Extract two 4-port networks:

Type G

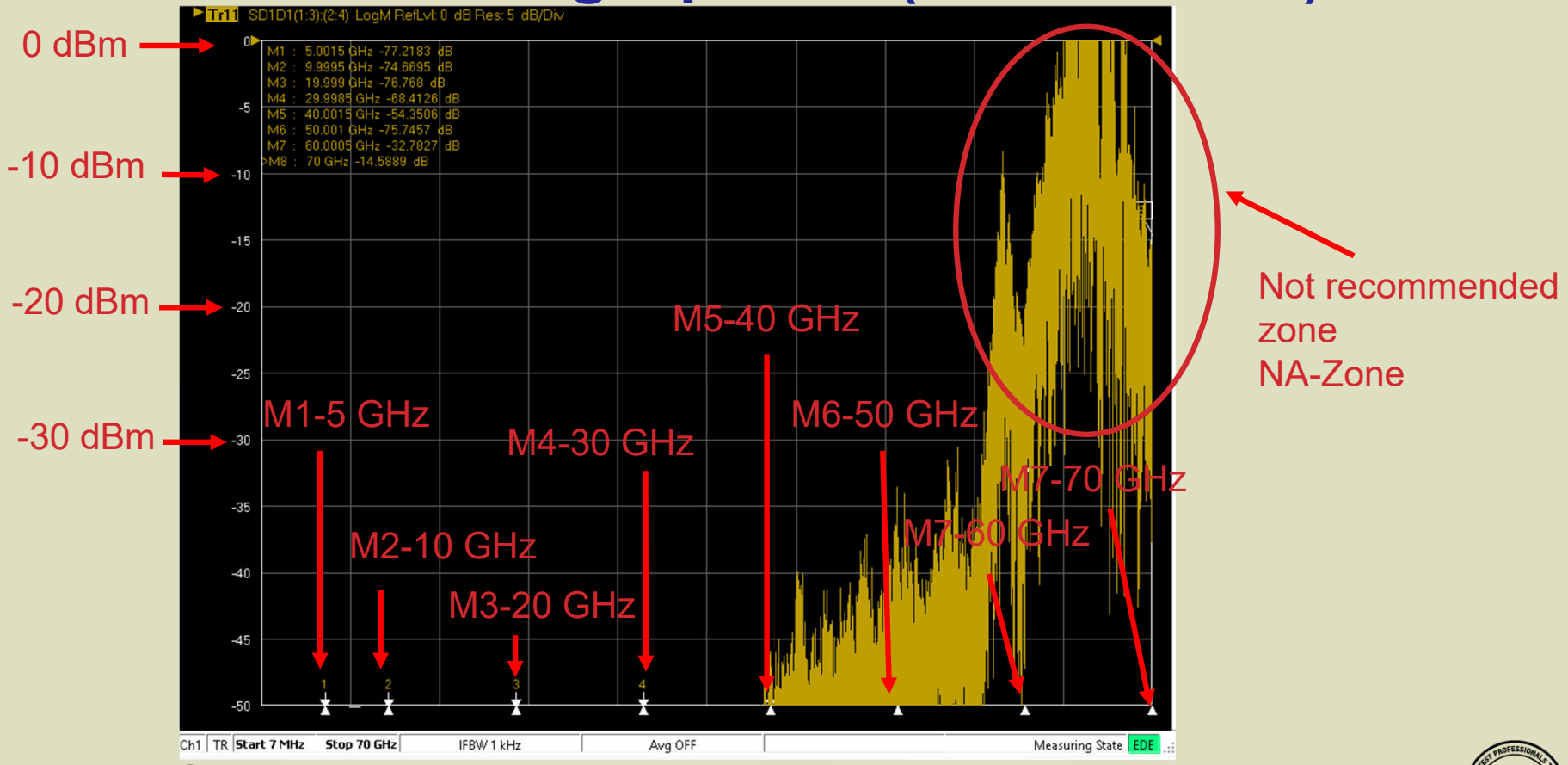
Outer Cal Only,
using divide-by-2 method



Legend: a = Reference Plane location/s of cal a

VNA De-embedding Options (Insertion Loss)

VNA De-embedding Options (Return Loss)

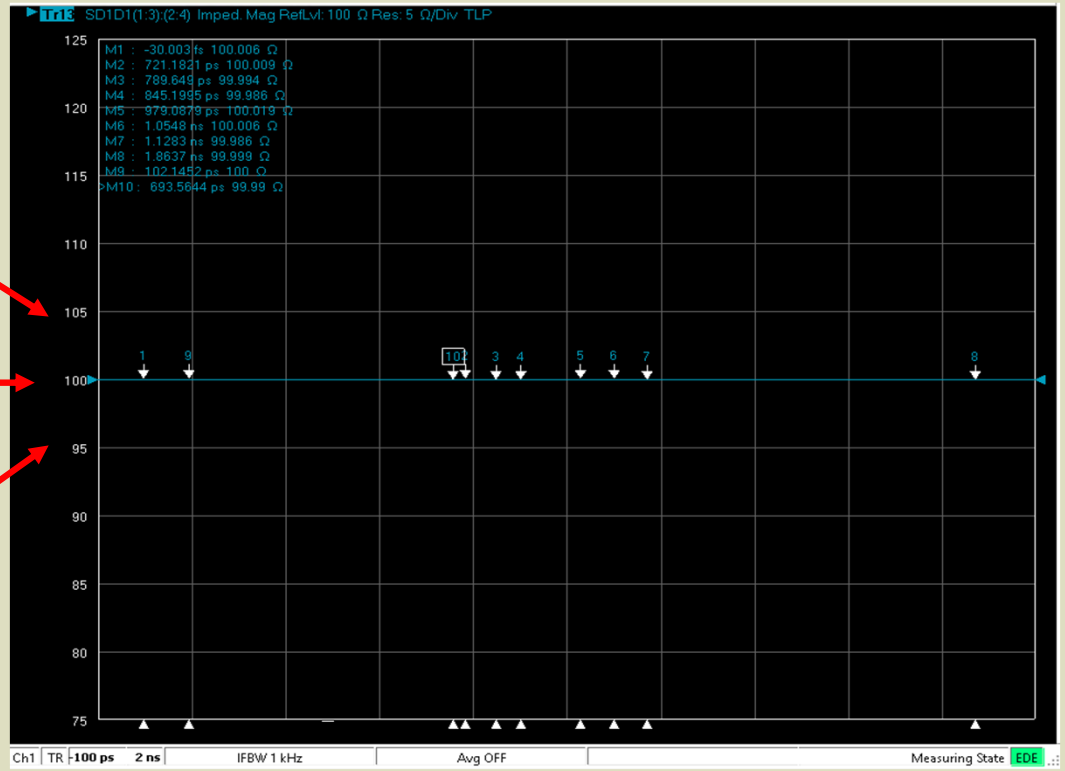


VNA De-embedding Options (TDR after de-embedding)

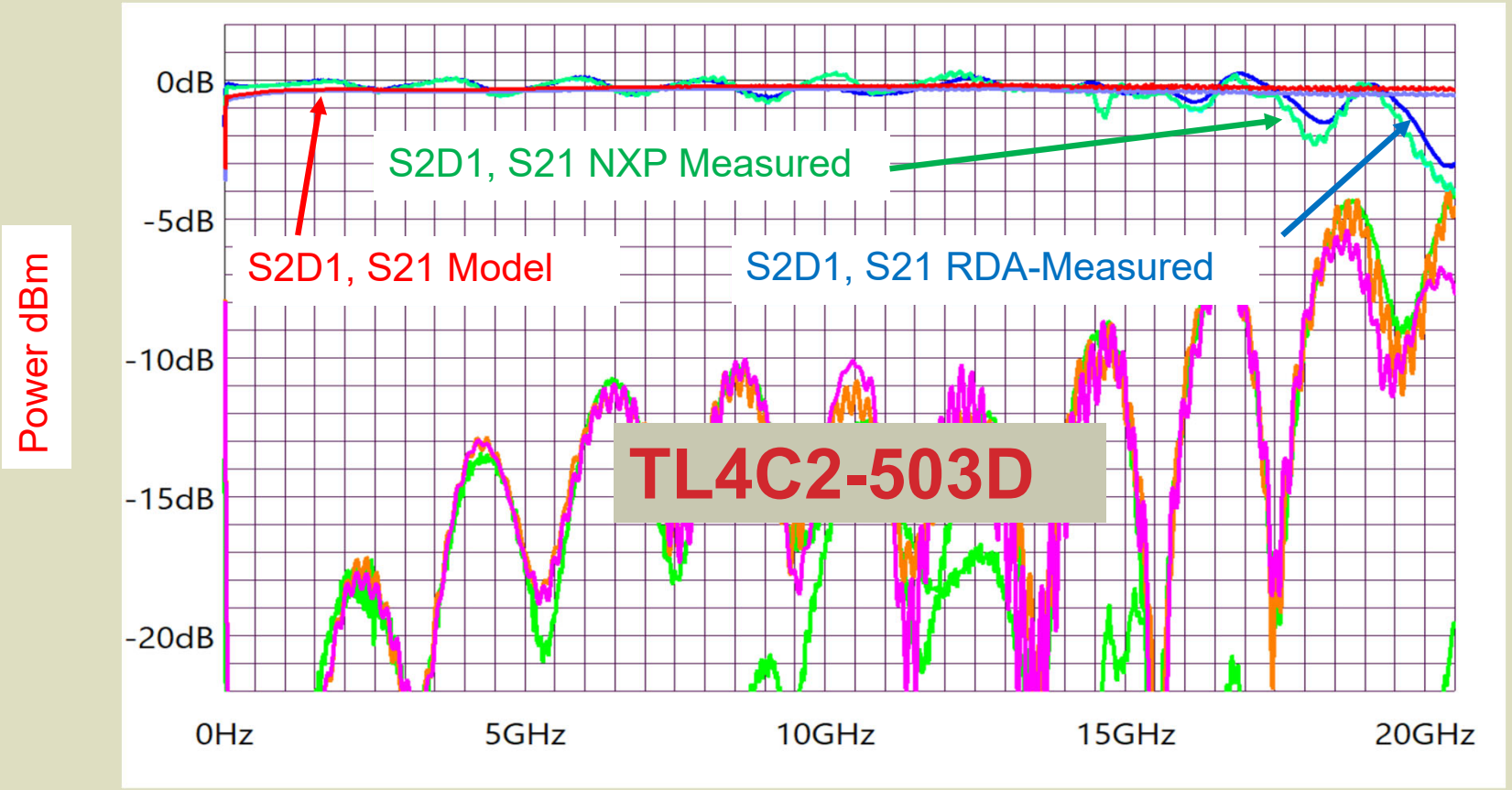
105 Ohms Differential

100 Ohms Differential

95 Ohms Differential



VNA, 85 Ohms Bias-Tee Model vs Measured NXP & RDA

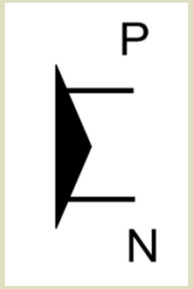


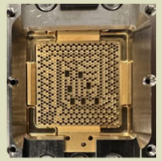
Measurement Strategy & Planning NXP & RDA

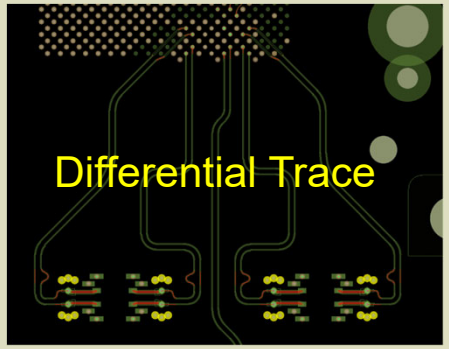
- Correlation of measurement methodology and techniques is key
  - Resolution Steps
  - Range as function of real-world application of the hardware to be measured (e.g. 3rd , 5th harmonic, standards compliance)
  - Fixturing such as connectors, cables, probes, prototype boards
- Hardware Design for Testability
  - How to facilitate Signal Integrity Validation on the hardware
  - Design fixtures, probe for SI measurement of the transmission line
  - Transmission line segment design, analysis, and integration

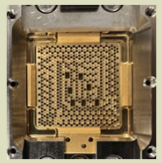
SOC IP's with Specific Differential Impedance

TX IBIS Model
- Mod-T
- Mod-I
- Mod-L









RX IBIS Model
- Mod-T
- Mod-I
- Mod-L

TX, RX Impedance IP Specific (Package Electrical Rules for IMX95 and Tunis)
- Standard I/Os 100 Ohms, Diff 50 Ohms SE,
- USB 90 Ohms, (5G+, 10G+ Data Rate)
- PCIE/Ethernet 85 Ohms, (16G,28G, 32G Data Rate+)
- DDR 80 Ohms Diff, 40 Ohms SE, (4G, 8G+ Data Rate+); Not on Bias-Tee Loop back

TX Impedance Thevenin Equivalent circuit Math=VNA TDR Profile **RX Impedance**

S-Parameters

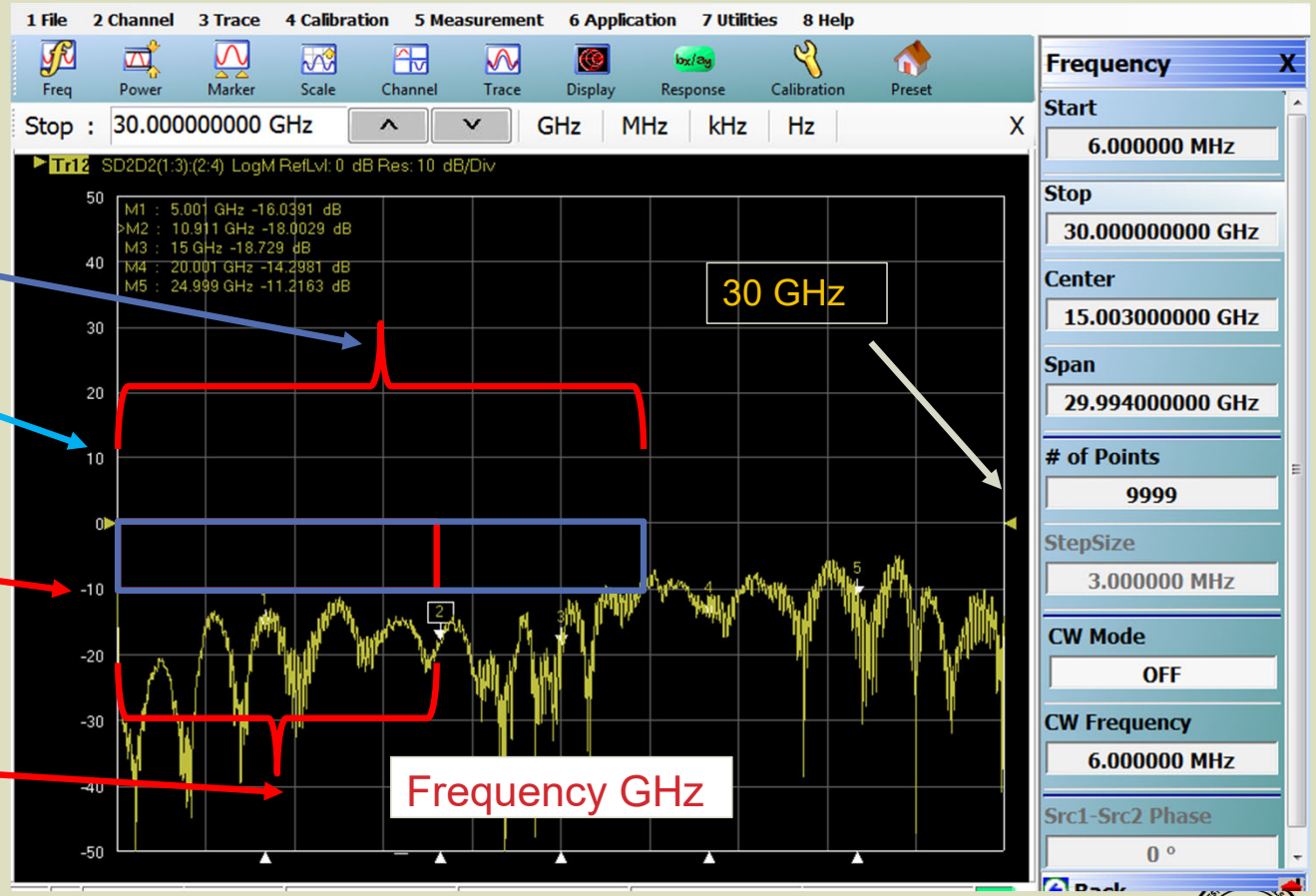
VNA, Return Loss Measurements

28 G HW Pass Region

Power dBm

-10dB HW Budget

16 G HW Pass Region

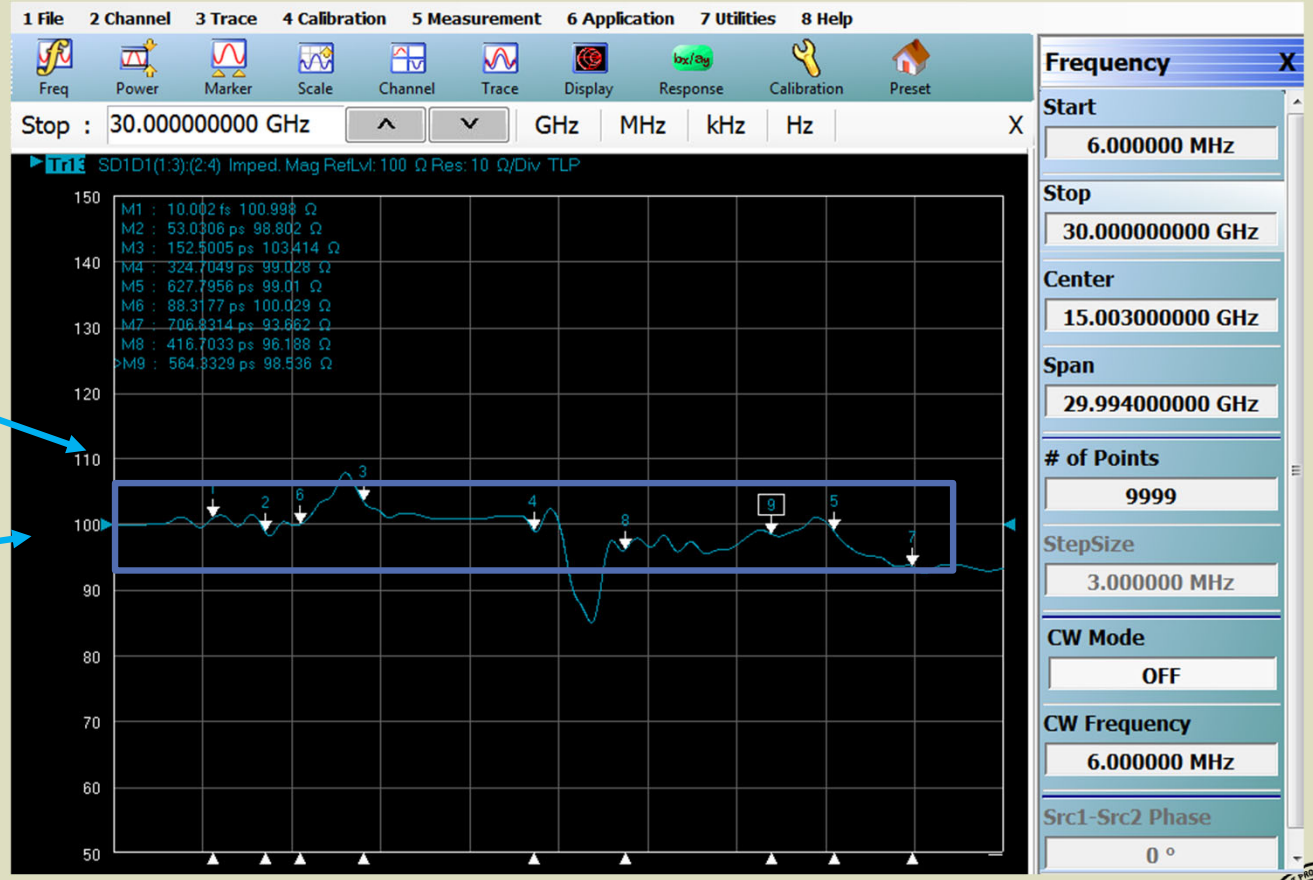


VNA, TDR Profile ; 100 Ohms Differential

Good impedance profile from TX to RX

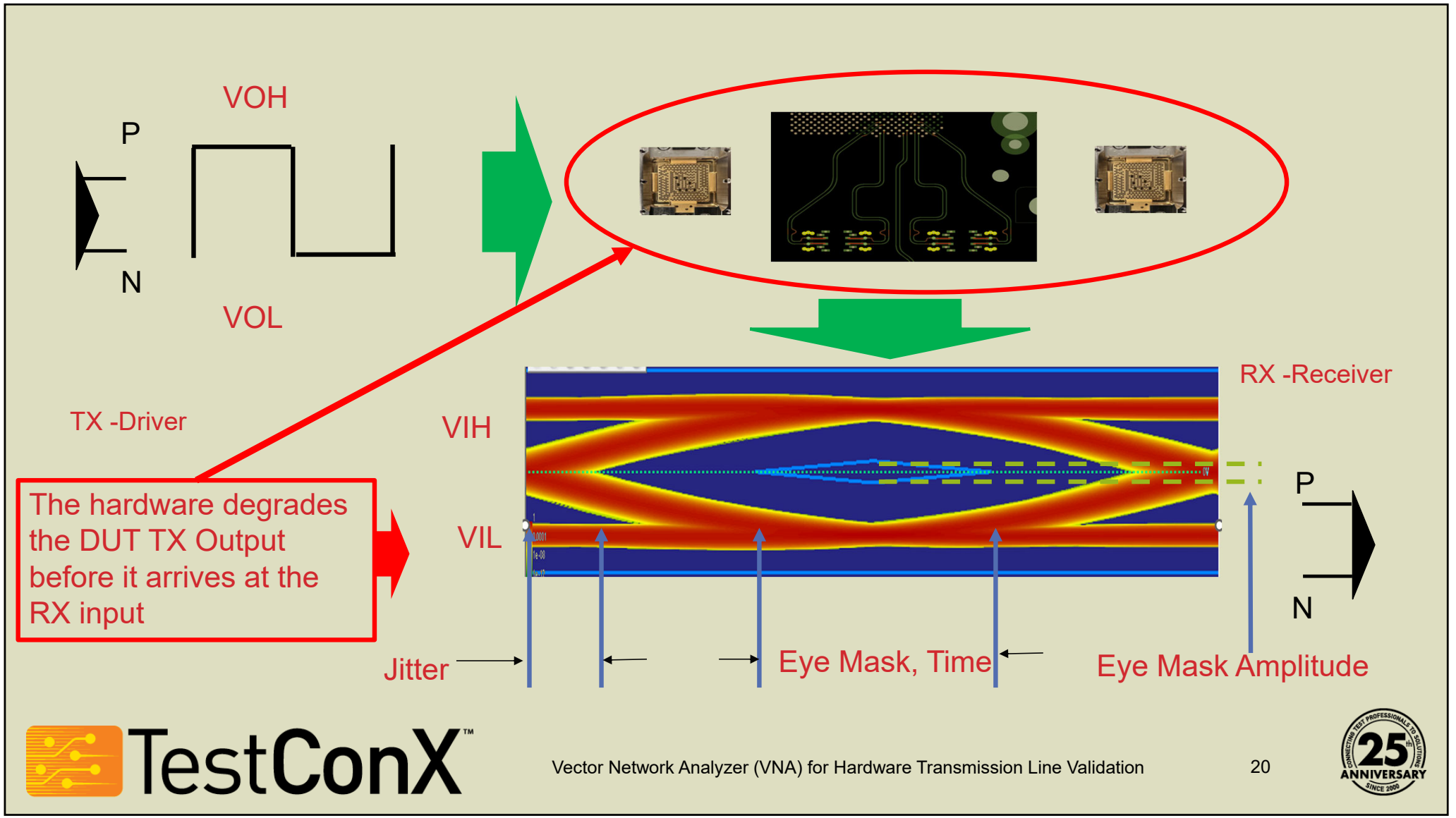
Impedance Ohms

10 Ohms HW Budget

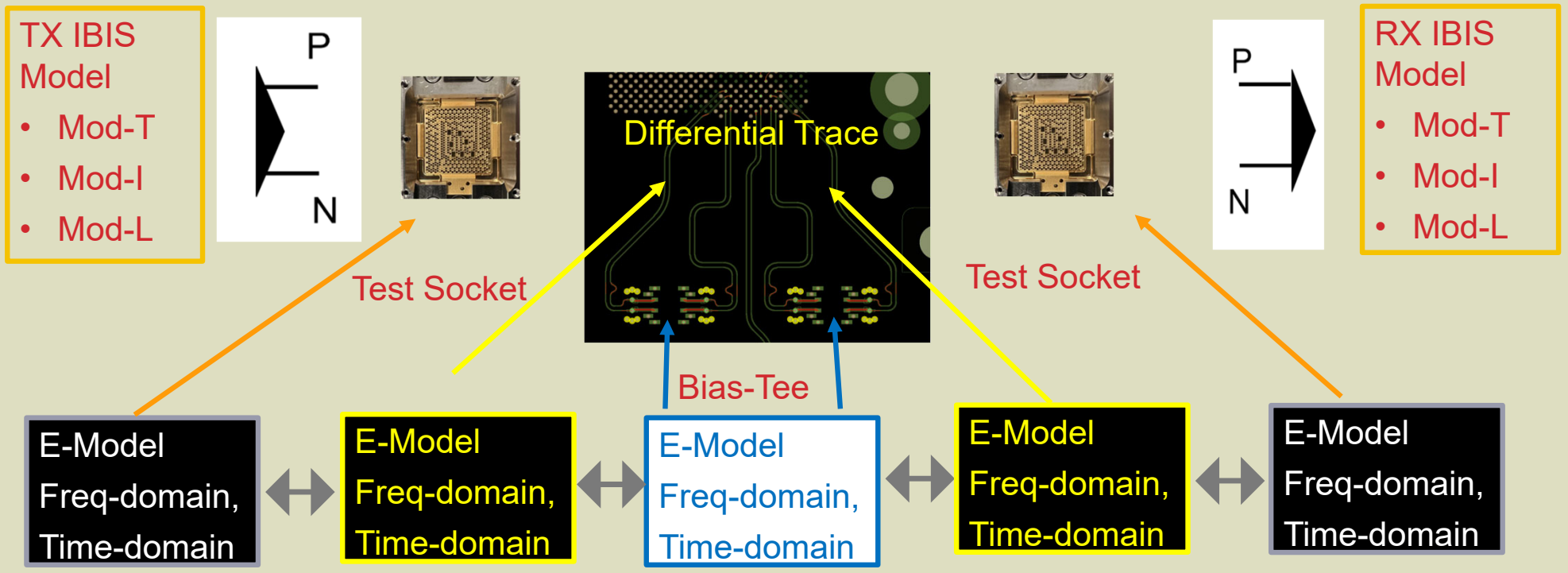


Test Hardware Signal integrity Design, Modeling, Simulation, and Validation.

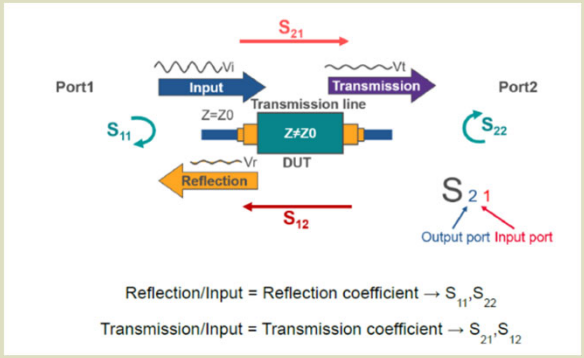
CLOSED LOOP HARDWARE DESIGN


VOH
P
N
VOL
TX -Driver
The hardware degrades the DUT TX Output before it arrives at the RX input
VIH
VIL
RX -Receiver
P
N
Jitter
Eye Mask, Time
Eye Mask Amplitude

Loop Back Testing Transmission Line Segments



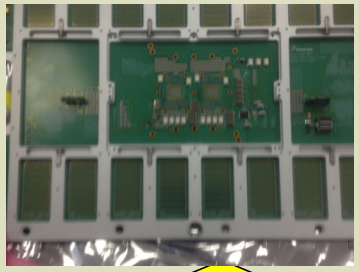
Closed Loop Hardware Design Concept



Hardware Design Budget
S-parameter, Impedance

6 Check for compliance?

2



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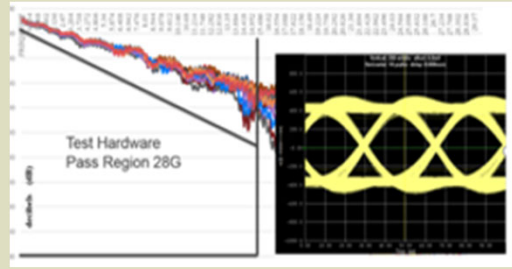
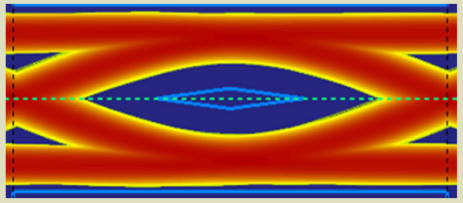


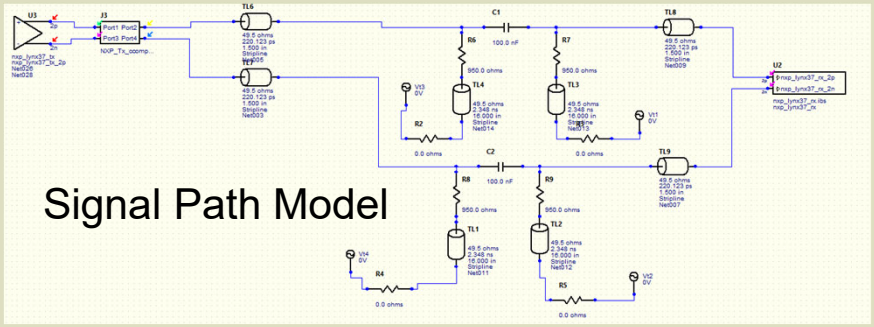
Measured Performance

5

1



DUT Data Sheet



Signal Path Model

Hardware Validation Lab

Conclusion

- Short wavelength , high speed data rate necessitates validation of transmission line performance of the hardware.
- The capability to ascertain the different segments of the transmission line individually, separately, and its impact on the complete signal path is key to successful high-volume production solution(zero hardware test issues).
- VNA is an irreplaceable instrument, tool to NXP's closed-loop hardware design strategy.

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