The Mix Is In: Tuning Socket Impedance for Optimal Validation Performance

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NXP HiCon HighRel, Inc.

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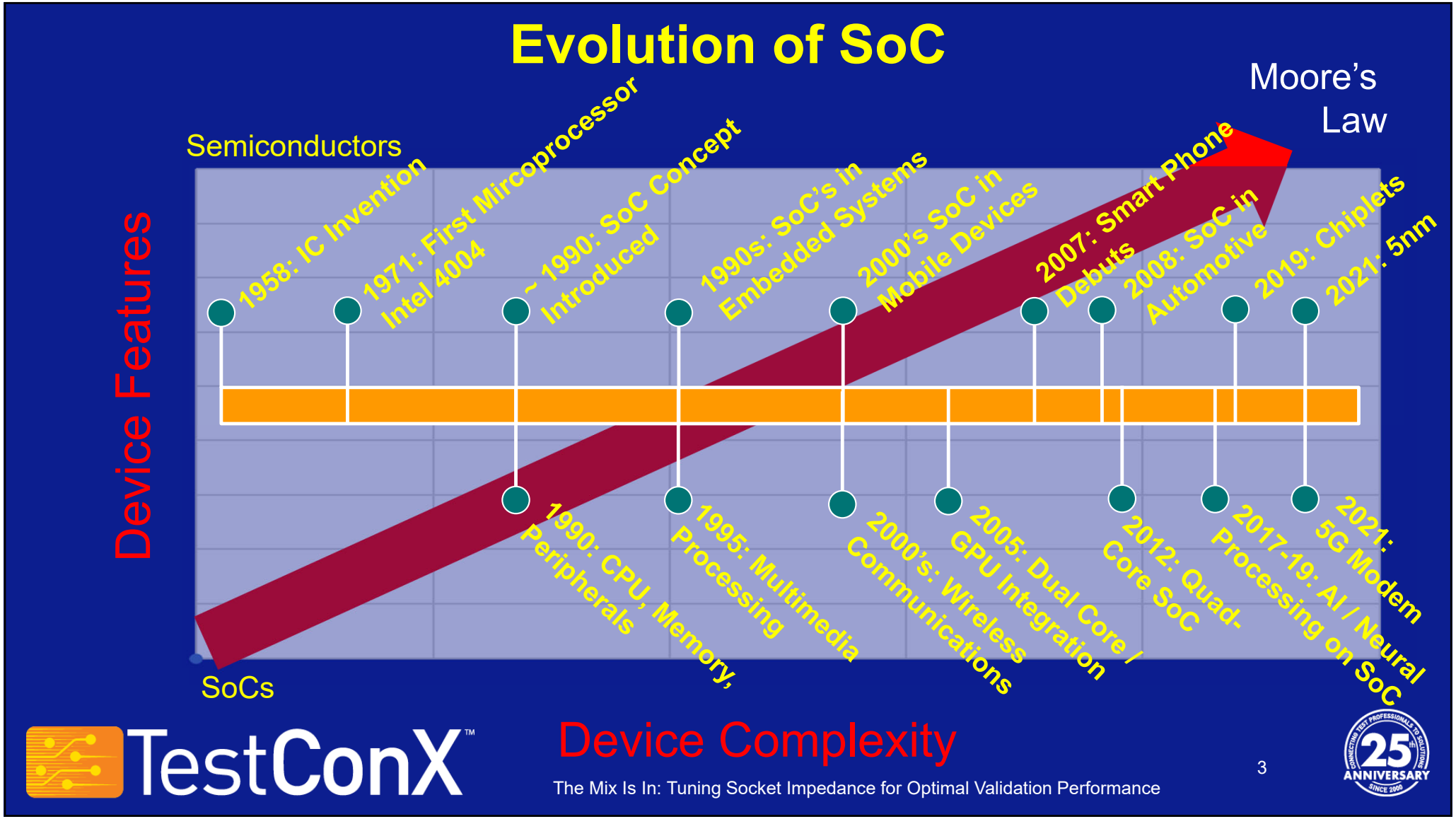
Evolution of SoC
Moore's Law
Semiconductors
1958: IC Invention
1971: First Mircoprocessor Intel 4004
~ 1990: SoC Concept Introduced
1990s: SoC's in Embedded Systems
2000's SoC in Mobile Devices
2007: Smart Phone Debuts
2008: SoC in Automotive
2019: Chiplets
2021: 5nm
Device Features
1990: CPU, Memory, Peripherals
1995: Multimedia Processing
2000's: Wireless Communications
2005: Dual Core / GPU Integration
2012: Quad-Core SoC
2017-19: AI / Neural Processing on SoC
2021: 5G Modem
SoCs
Device Complexity
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Mixing it Up – Key Drivers

USB 4

DDR-HDM6

HDMI

PCI-e

Wi-Fi

SER-DES

Ethernet

5G

UCIe

- Device features have historically been designed for different PCB impedance
- SoC feature growth has resulted in multiple impedances
- Sockets typically designed for a single impedance – One Size Fits All!
  - 85 – 100Ω

Is this the best approach?

Device Features and Impedance Requirements

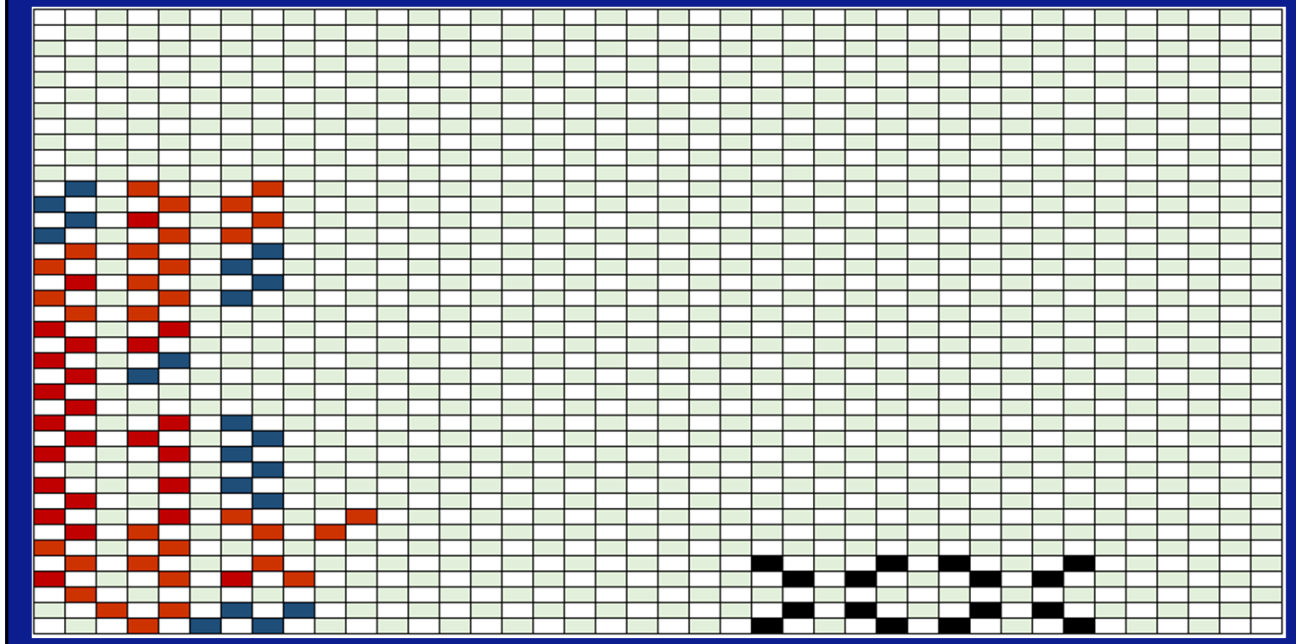
IP Type	Model	Impedance (Diff) (Specifications)	Data Rate
PCIE	T	85 Ohms	16G
DDR	T	80 Ohms(40 Ohms SE)	8G
Ethernet	I	85 Ohms	16G
PCIE	I	85 Ohms	10G
USB3	I	90 Ohms	10G
DDR	I	80 Ohms (40 Ohms SE)	4G
PCIE	L	100 Ohms	28/32G

To be tested

Changed to 100Ω in socket

- 7 different feature sets and impedance requirements
- Socket required to support 3 separate differential impedance targets

Device Pin Layout By Impedance



40Ω Single Ended Impedance

80Ω Differential Impedance

85Ω Differential Impedance

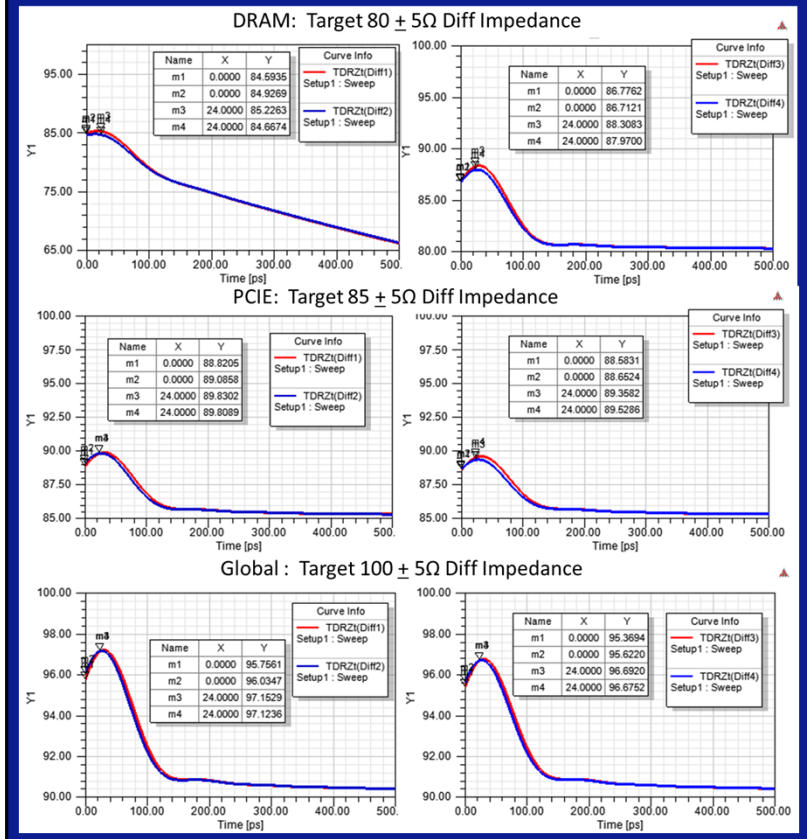
50Ω SE / 100Ω Differential Impedance

Device Layout: 800BGA / 0.65mm pitch

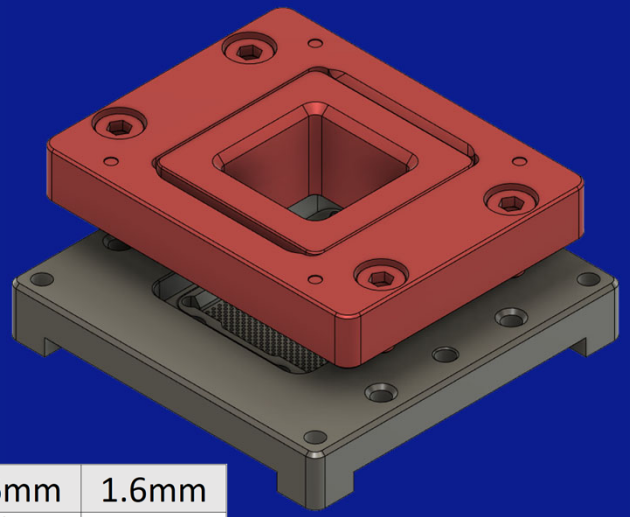
Evaluation Methodology

- Three different impedance targets:
  - 40Ω Single Ended / 80Ω Differential
  - 85Ω Differential and 100Ω Differential
- Simulations used to create the socket design
  - Contact pin configuration based on impedance target
- Measure mixed impedance socket on test bench and measure the impact of the socket on the insertion loss

Socket Design



Pin Impedance Design Simulations



Test Height	1.6mm	1.6mm	1.6mm
			
Model	05HRS	035HRS	025HRS
Diameter (mm)	0.36	0.26	0.16
Min Pitch (mm)	0.5	0.35	0.25
C-res (mΩ)	< 50	< 50	< 100

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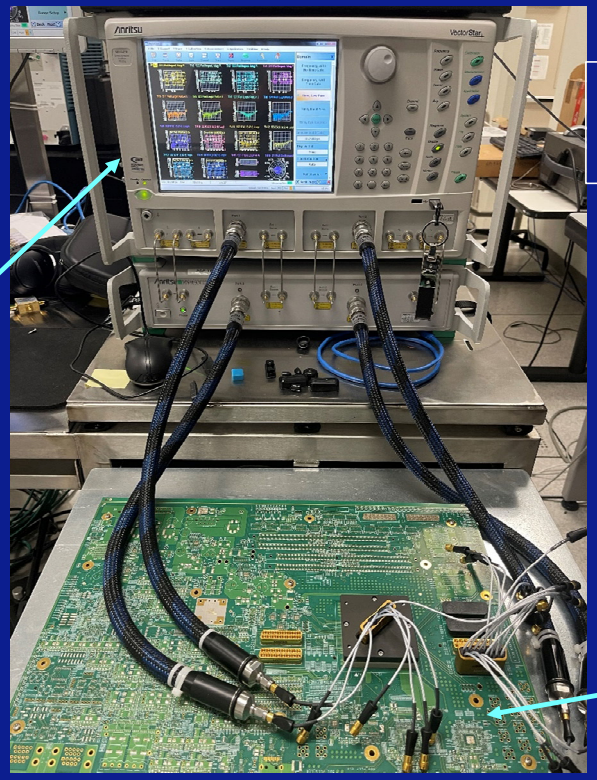
Measurement Setup



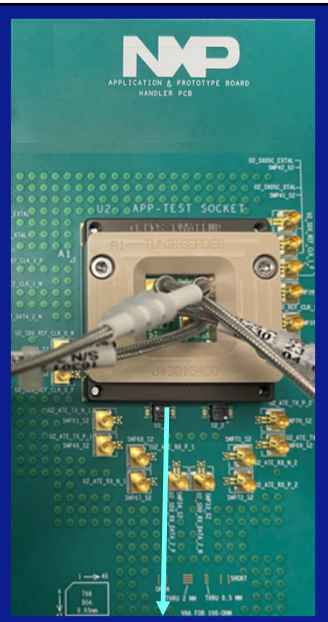
70GHz VNA

Test Bench Setup

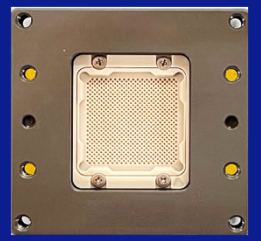
Phase Matched Cables

Application Board

VNA Validation Lab setup



Prototype ATE Test Board



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NXP Application Board Test Set up

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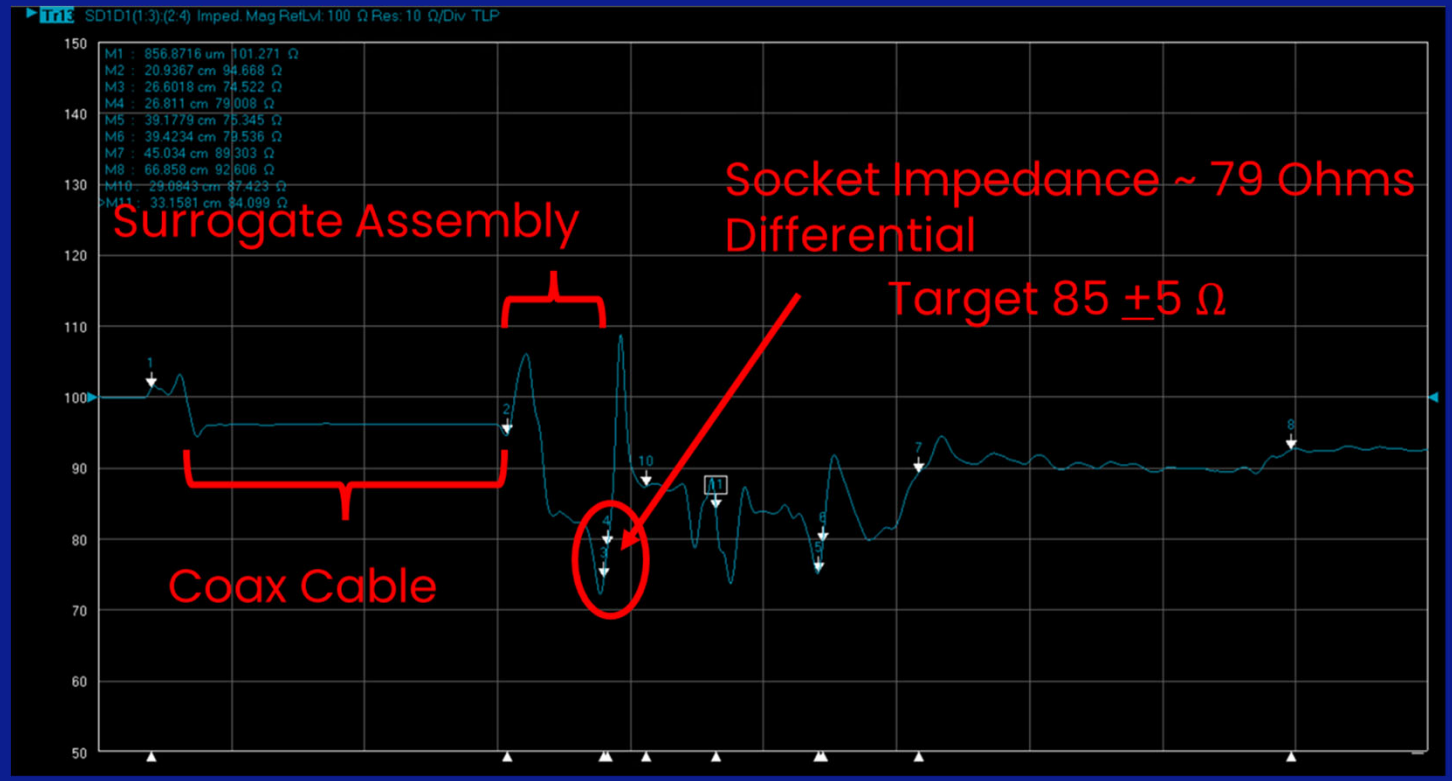
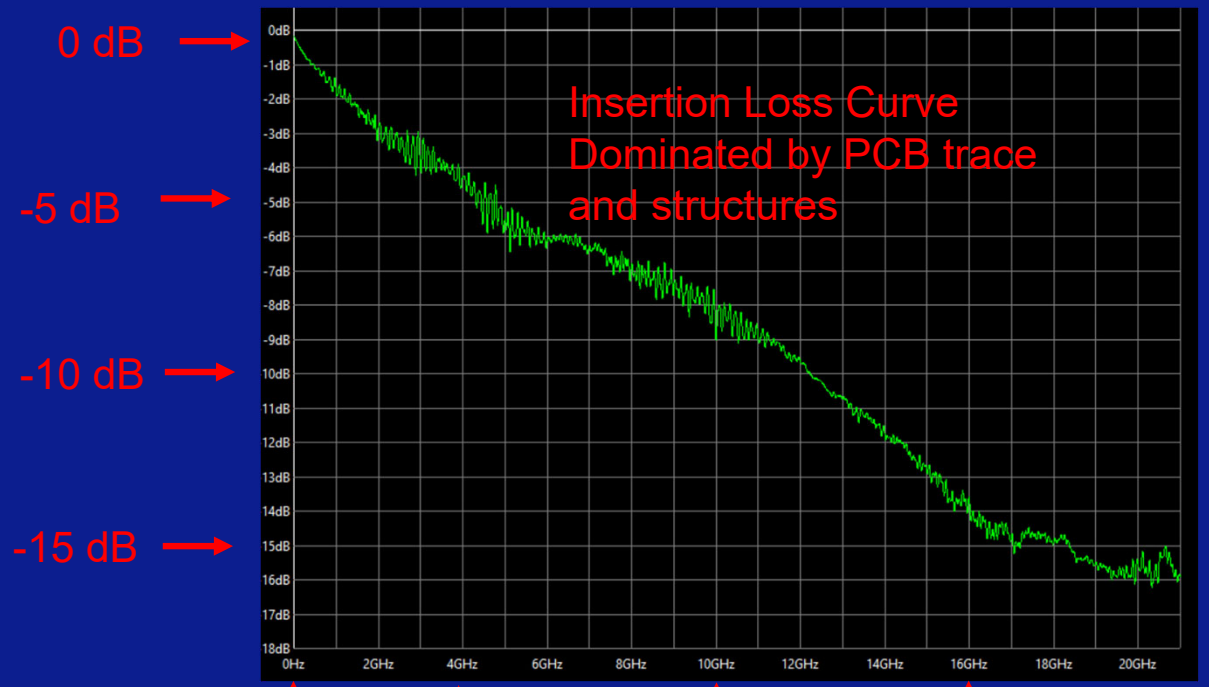
TDR Differential Measurement Results



PCIE Insertion Differential Loss– Apps Board

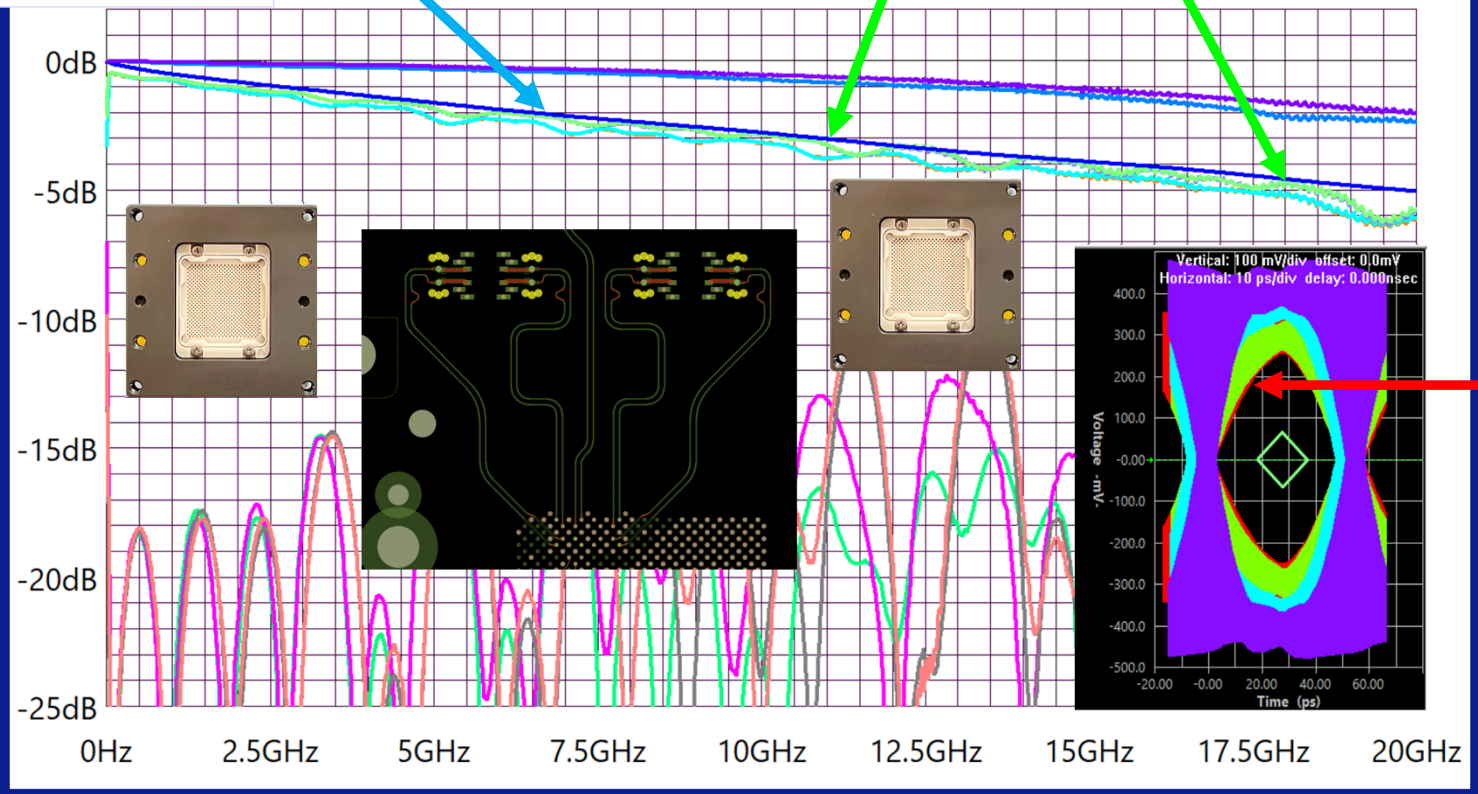


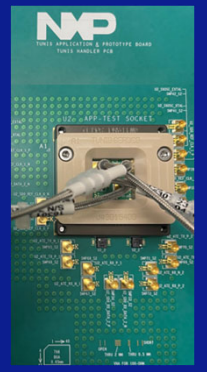
Apps Board Traces
> 7 inches long

PCIE Insertion Differential Loss– Proto Board

S2D1 INSERTION LOSS

Green Line is the Socket





Data Eye:

Red is the socket contribution

Socket Contribution Is Negligible!

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Key Learnings

- This is a true research project
  - Started with a hypothesis, no expectations, but felt there must be a benefit
- Socket simulation was effective in designing the specific impedances
- Measurement results
  - Insertion loss on prototype board showed pin with matched impedance had negligible impact
  - As data rate increases, the socket contribution will become more critical
- Hardware design can play a major role in the results
  - Board / design trace length

Conclusions

- The trend towards greater integration and functionality on SoC's will continue
- Si validation has traditionally relied on sockets with a global impedance target
- The ability to tune a socket to match impedance for specific device characteristics was shown to be effective
- As data rates increase, the negative impact of socket-to-device impedance mismatch will increase and the ability to tune sockets will become more imperative

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