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High Performance Compute Test Trends in The Chiplet Era

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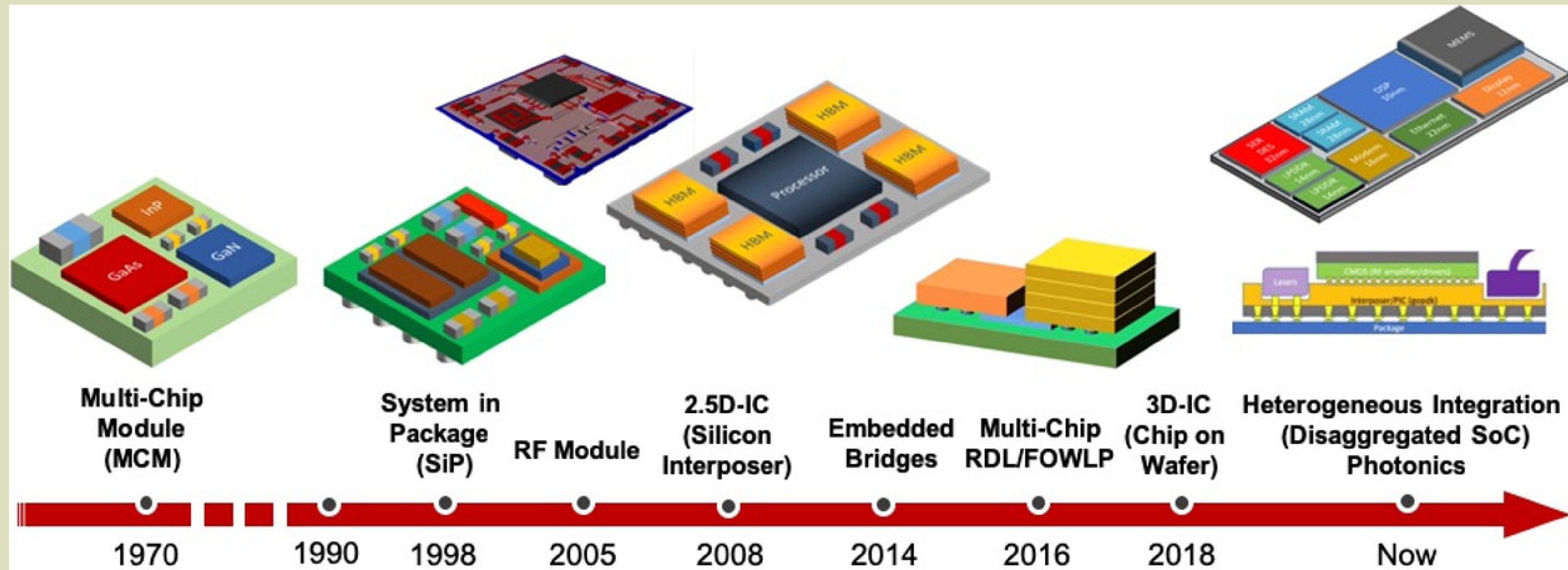
Agenda

- High Performance Compute (HPC) Device Testing Today
- Evolution to Multi-Die HPC
- Multi-Die Design Flows
- Test Data Volume
- TeraVector Multi-Core Conversion
- Replay Design to Test
- Paradigm Shifts in ATE
- Protocols in Semiconductor Test
- UCIe Overview and ATE Access
- Power Integrity (PI) High Power Simulation
- Fixture Protection Strategies
- Wafer Sort Power Management
- Package HIR
- Summary

HPC Device Testing Today

- Large Reticle limited (800mm²) or wafer-scale devices
  - Power Distribution Network (PDN) 500-1,200 Amp core power
  - 100’s to >80K Machine Learning (ML) / Graphics Processing Unit (GPU) / Compute cores
  - Device, fixture safety and protection are critical
- HSIO physical layer testing
  - Tera-bytes of I/O bandwidth for device workloads
    - 32-64 Gbps PCIe5/6
    - 40-120 Gbps USB4/V2
    - 112-224 Gbps PAM4/6
    - 1 to >512 lanes
- HPC data sets of 256 GByte for a single device
  - Long Vector memory loads
  - Compression, Pooling and Memory sharing
- Yield learning requirement for Zero overhead datalogging
- Test methodologies addressing Silent Data Corruption (SDC)

Evolution to Multi-Die HPC



Source: Cadence

- Multi-Chip integration technology has more than 30 years of history
- **What test challenges will the new era of multi-die integration bring?**

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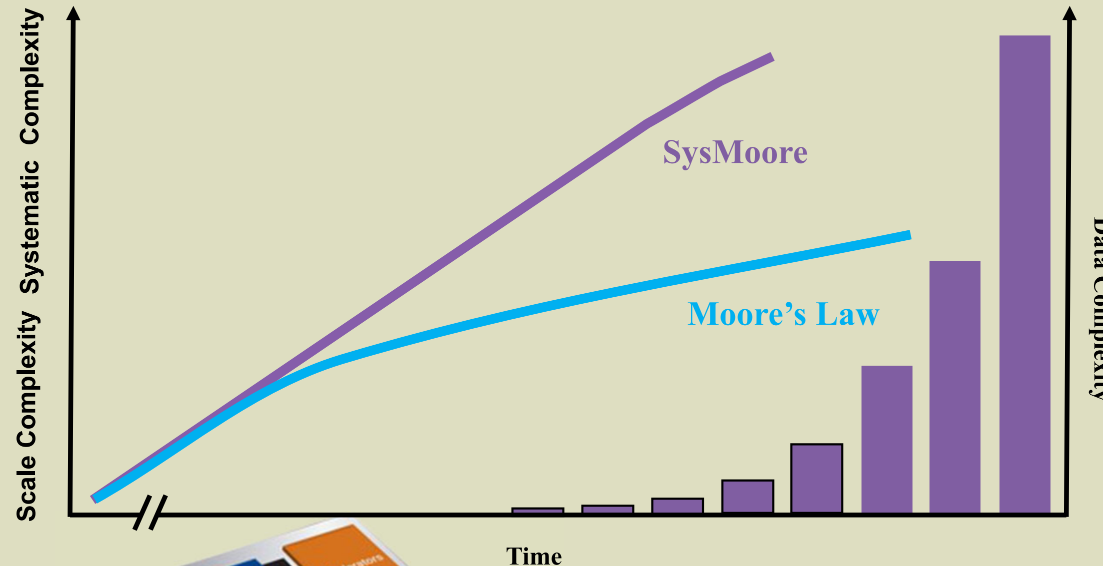
Multi-Die Design Flows



Motivation for Multi-Die Systems

Accelerated scaling of system functionality at a cost-effective price (>2X reticle limits)

Reduced risk & time-to-market by re-using proven designs/die

Lower system power while increasing throughput (up to 30%)

Rapid creation of new product variants for flexible portfolio management

Courtesy of Synopsys

Test Data Volume

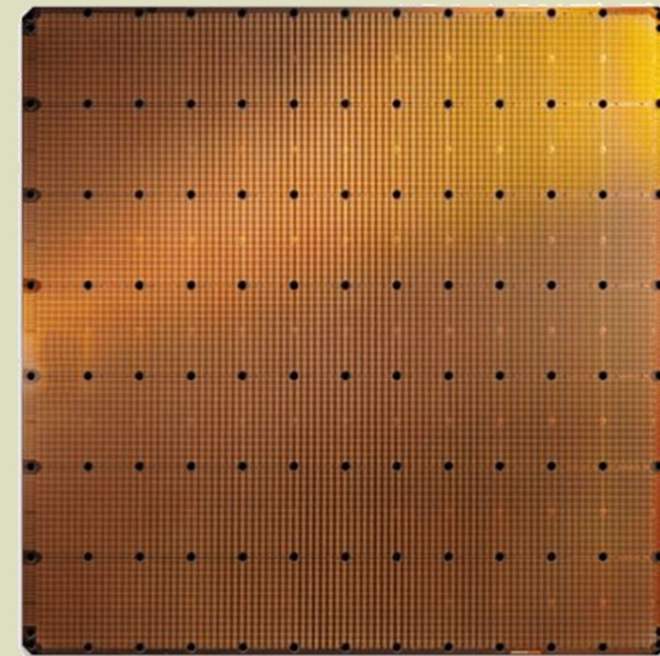
– Dan Hutcheson, TechInsights

In 1947 there was only one transistor; semiconductor production facilities made 250 x 10^{18} transistors in 2015

According to TechInsight's, the semiconductor industry produced almost 2 x 10^{21} transistors in 2021

Assuming only 80% of the transistors are tested and each transistor results in just one bit of data, that is >40 Tb per second in 2021

Largest GPU
826mm² Silicon
54.2 Billion transistors



Cerebras WSE-2
46,225mm² Silicon
2.6 Trillion transistors

How much data can test generate?

TeraVector Multi-Core Conversion

Design Files
1-10,000

Input

VelocityCAE
1024 Cores
Manages pattern to core assignments

Pattern 1
Core 1
Pattern 1024
Core 1024

Convert all design files in a day

Common Wavetable & Timing Specs

Maximum Vector Compression

Generate Executable Test Program/Flow

ATE Patterns & Test Program

Design Files
REPLAY_93k.v
REPLAY_93k.story
REPLAY_93k.evcd

Replay Design to Test

Verilog
Testbench
Synth.v

Input

Simulator
&
DUT
Verilog Model

Output

WGL/STIL/EVCD
PASS/FAIL
Simulation

Output

ATE
Program/Patterns

ATE.v
Virtual Test
0 X
1 X
0 X
…
SSN/DDR
Z L
Z H
Z L
Z H

From Simulation

ATE Rules Check
& Model Applied

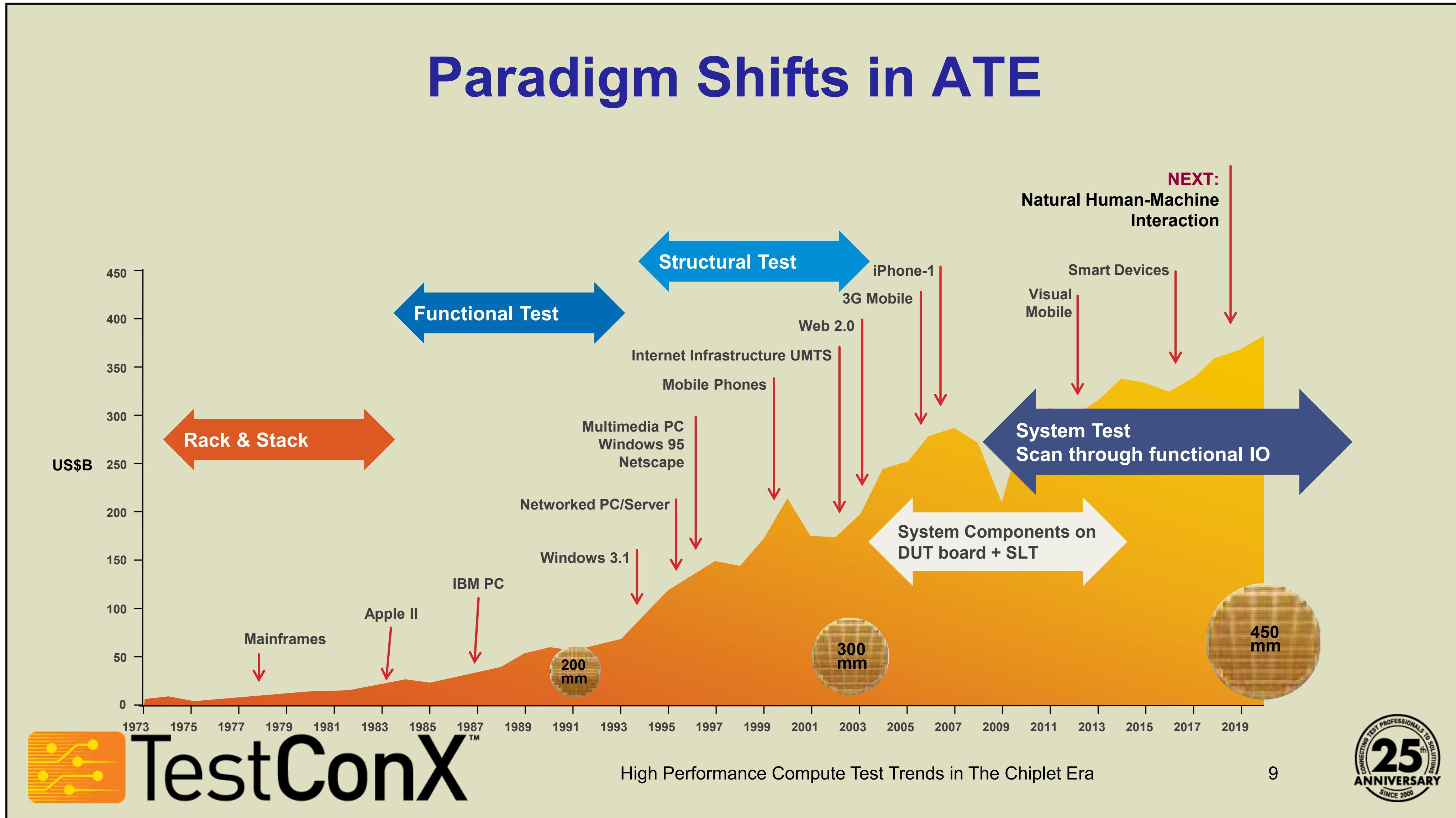
0 X
1 X
0 X
1 X
…
Z L
Z H
Z L
Z H

Virtual Test ATE.v File Input to Re-simulate

ATE.v (Verilog Test Bench)
SSN w/SDR/DDR Annotations
PVT Variables
Verilog ATE Datalogger

Verified ATE Compliant

ATE Transactions with
Virtual Test 93K encoded


Paradigm Shifts in ATE
NEXT:
Natural Human-Machine Interaction
Structural Test
Functional Test
Rack & Stack
System Test
Scan through functional IO
System Components on DUT board + SLT
iPhone-1
3G Mobile
Web 2.0
Internet Infrastructure UMTS
Mobile Phones
Multimedia PC
Windows 95
Netscape
Networked PC/Server
Windows 3.1
IBM PC
Apple II
Mainframes
Smart Devices
Visual Mobile
US$B
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350
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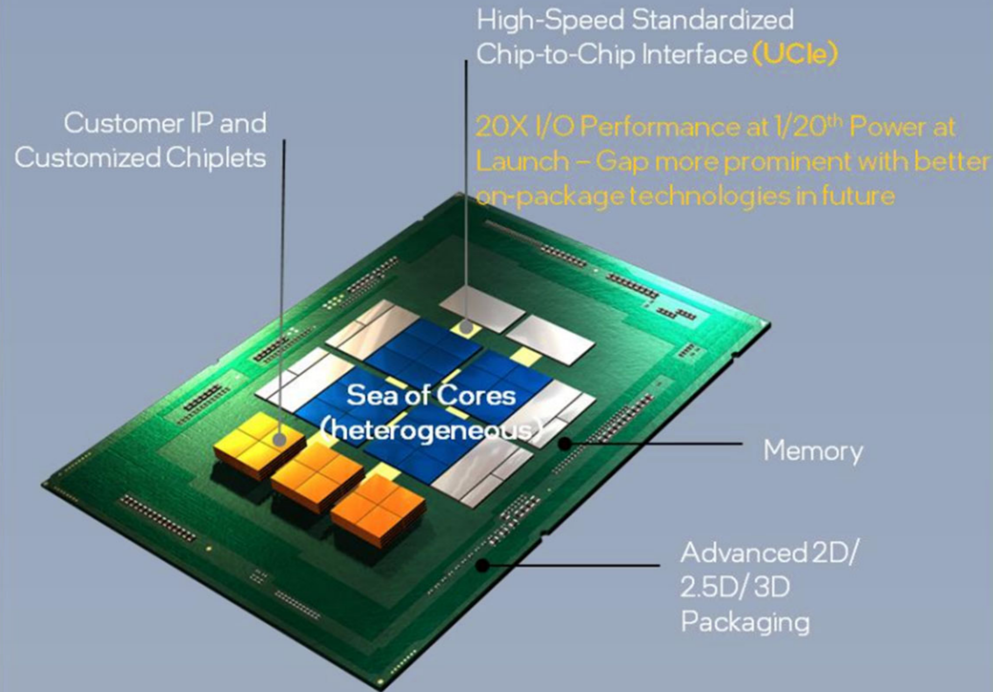
Protocols in Semiconductor Test

• UART	1971	2-wire 921,600 bps
• SPI	1980	4-wire 10 Mbps
• I2C	1982	2-wire 3.4 Mbps
• CAN	1986	2-wire 5 Mbps
• JTAG	1990	5-wire 25 Mbps
• SMB	1995	2-wire 100 Kbps
• MDIO	1999	2-wire 2.5 Mbps
• SWD	2003	2-wire 32 Mbps
• USB3.2	2017	2-wire 10 Gbps
• PCIe4	2017	4-wire 16 Gbps
• PCIe5	2019	4-wire 32 Gbps
• PCIe6	2021	4-wire 64 Gbps (32 GT/s – PAM4)

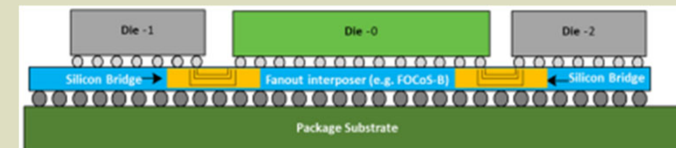
UCIe Overview

UCIe = Universal Chiplet Interconnect Express



- High-speed chip-to-chip interface (short reach)
- Open industry standard, Rev 1.1 released in 2023
- Very high bandwidth: Up to 1.3 TB/sec/mm^2
- Very dense pitch: 25µm ... 130µm
- Good power efficiency: 0.25 ... 0.5 pJ/b
- Two package types: Standard and Advanced
- Intended for in-package connections

Standard package

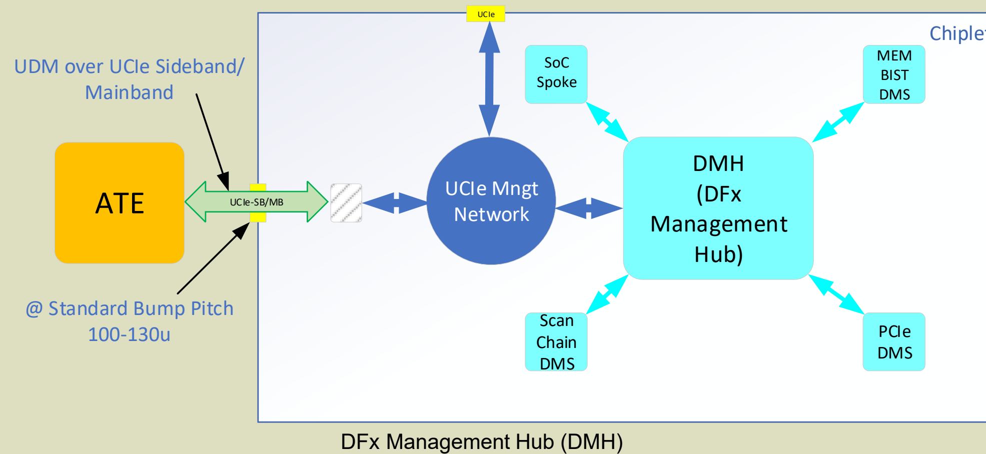


Advanced package

- This device has 13 chiplets
- With 99% "known good die" yield
- The compound yield will be 87.75%

Test Access (UCIe-enabled) Chiplet Logic

- **Chiplets will have large amounts of digital logic**



DFx Management Hub (DMH)

SCAN volume examples:

- Mobile device (i.E. Cell phone processor): 8 GByte
- High performance compute device: 72 ... 128 GByte
- High-end GPU / AI device: 256 GByte

Why so much test data ?

- Test pattern volume grows with transistor count
- New fault models for latest processes (i.E. Cell-aware)
- More stringent DPPM requirements -> more tests

Needs high throughput in production test:

- Wide bus with many pins at moderate speed (Mbits/sec)
- Small bus with few pins at high speed (Gbits/sec)

Example: 64 Gbyte on 8-bit bus @ 4 GBit/s = 16 sec test time

UCIe-S as Test Port for Chiplets

Optional UCIe-S Test Port (8 or 16 bit wide)

Figure xxxx: UCIe-S_t x16 Module used for testing

	m1rxcksb		m1rxdatasb		vccaon
m1txdatasb		m1txcksb		vccaon	
	vccio		vccio		vccio
vss		vss		vss	
	m2rxdata6		m2rxdata8		vss
m2rxdata4		m2rxckp		m2rxdata10	
	vss		vss		vss
m2rxdata5		m2rxckn		m2rxdata11	
	m2rxdata7		m2rxdata9		vss
vss		vss		vss	
	m2rxdata2		m2rxdata12		vss
m2rxdata0		m2rxtrk		m2rxdata14	
	vss		vss		vss
m2rxdata1		m2rxvld		m2rxdata15	
	m2rxdata3		m2rxdata13		vccio
vccio		vccio		vccio	
	vss		vss		vccio
vccio		m1txdata7		m1txdata9	
	m1txdata5		m1txckn		m1txdata11
vss		vss		vss	
	m1txdata4		m1txckp		m1txdata10
vss		m1txdata6		m1txdata8	
	vss		vss		vss
vccio		m1txdata3		m1txdata13	
	m1txdata1		m1txvld		m1txdata15
vccio		vss		vss	
	m1txdata0		m1txtrk		m1txdata14
vss		m1txdata2		m1txdata12	

Fixed Shoreline (388.8um)

Bandwidth considerations

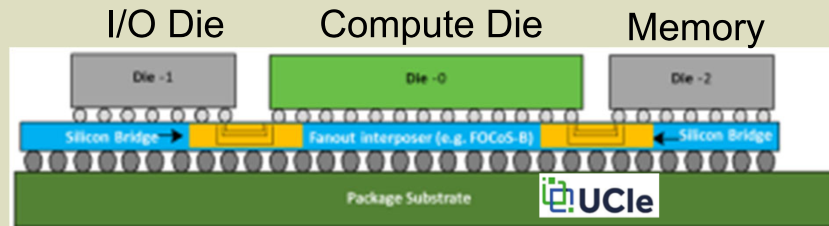
- Current trend for SCAN access is to use scan bus schemes which connect to ATE at 400…800 Mbit/sec
- Time-multiplexed, packetized scan data transfer
- Easy to scale up in speed into the Gbit/sec range
- Access through UCIe provides very high BW for SCAN:

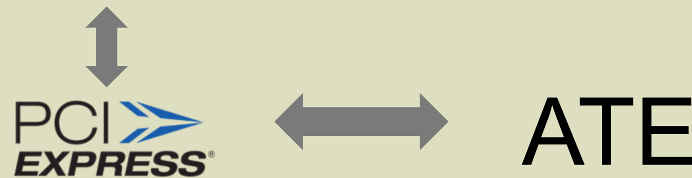
	4 I/Os	8 I/Os	16 I/Os
4 Gbit/sec	16 Gbit/sec	32 Gbit/sec	64 Gbit/sec
8 Gbit/sec	32 Gbit/sec	64 Gbit/sec	128 Gbit/sec
12 Gbit/sec	48 Gbit/sec	96 Gbit/sec	192 Gbit/sec
16 Gbit/sec	64 Gbit/sec	128 Gbit/sec	256 Gbit/sec

Massive bandwidth for (scan) test data transfer!

Package Test Through Functional I/F or DFT

I/O Die Compute Die Memory



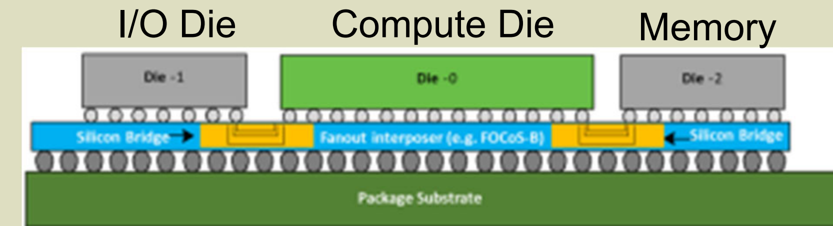


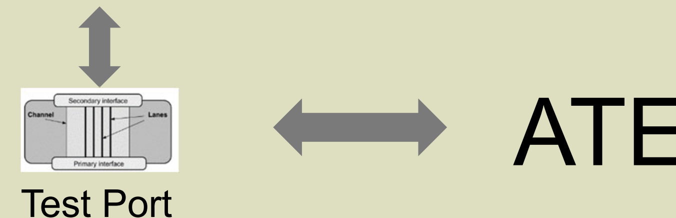
ATE

I/O Die with HSIO I/F (i.E. PCIe) connects to ATE
Test data travels to other chiplets through UCIe

- Needs IP for test through functional I/F
- Needs protocol card in ATE (i.E. Link Scale)

I/O Die Compute Die Memory





Test Port

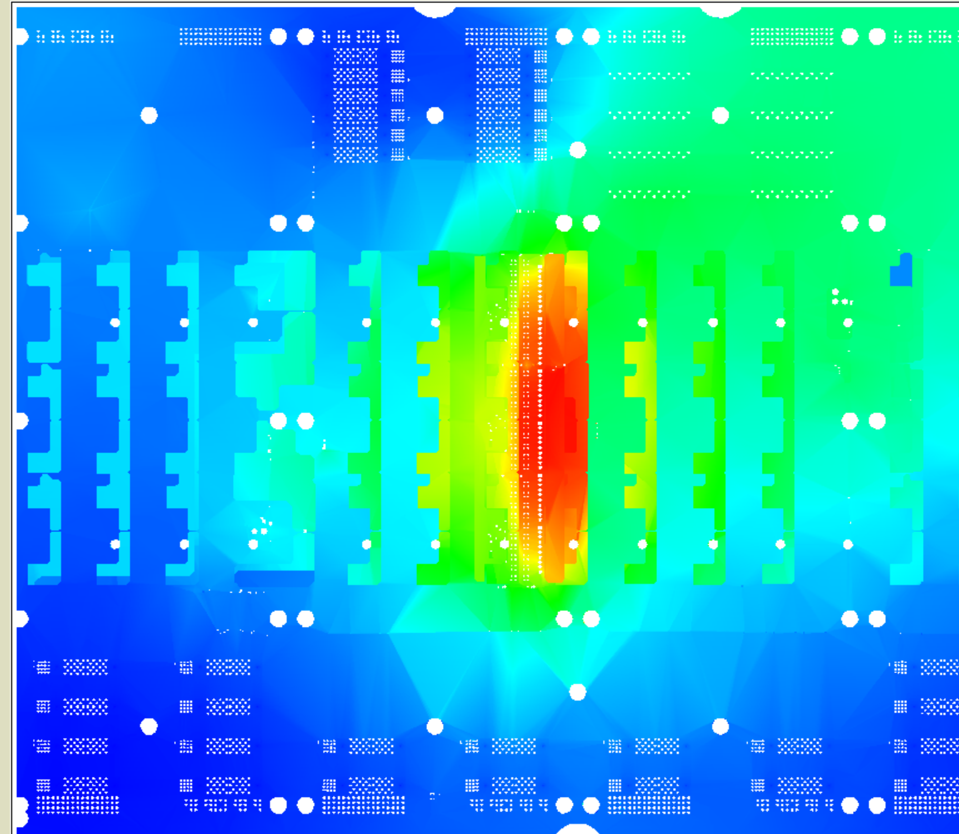
ATE

Test Port available on package
Test port forwarded to neighbor chiplets

- Needs test port routing in addition to UCIe
- Works with standard digital tester channels

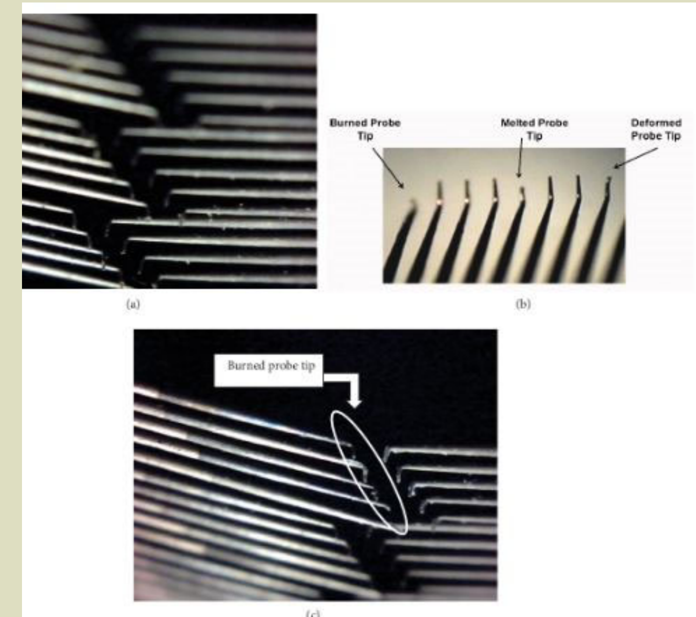
PI High Power Simulation

- PI-SI S/W
  - ADS, HyperLynx, Sigrity
- DC Drop Analysis
  - Excessive Voltage Drop
  - Excessive Current Density
- AC Analysis
  - Analysis including layout parasitics
    - Vias (RL), resistive paths, board capacitance
- PDN Analysis and optimization
- Temperature simulation profiling



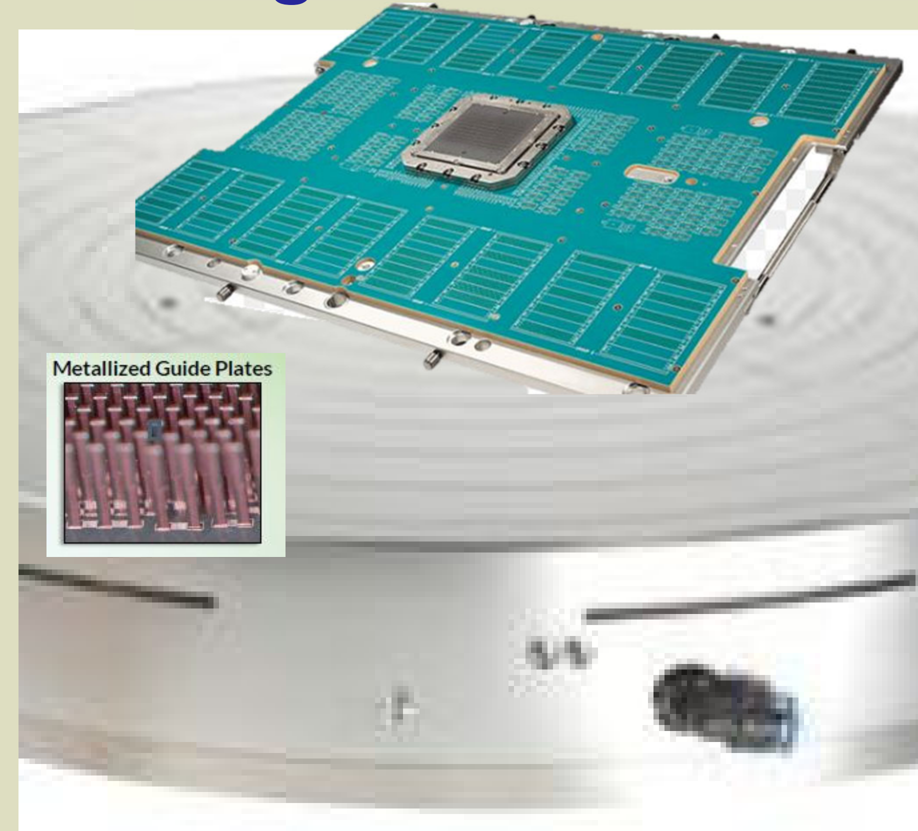
Fixture Protection Strategies

- Voltage and Current Profiling Test Flows
- Fast current clamps – XPS256/Next Gen HPC supplies
- DVS/HVS lower current pre-tests
- Higher Current Carrying Capability (CCC) probes
- Engineered power and signal pogo pins on FT sockets
- Thermal pre-triggering for high power events
- Develop overcurrent and probe burn Best Known Methods (BKM)



Wafer Sort Power Management

- Probe burn on ganged rails
  - Next-gen probes for higher CCC
  - Metallized Guide Plates
  - Fast Clamping Supplies (<35 µS)
  - Active Temperature Control (ATC) w/pre-triggering from tester
- Design PDN for maximum active current and wattage
  - HPC devices can have >1 KW for single location
  - Memory testing on wafer approaching 4 KW for entire chuck
- Multi-Zonal thermal chuck temperature mapping and cooling
  - TC or RTD calibration wafer
  - Variable Coolant flow
  - Nonconsecutive die stepping to minimize D2D heat leakage



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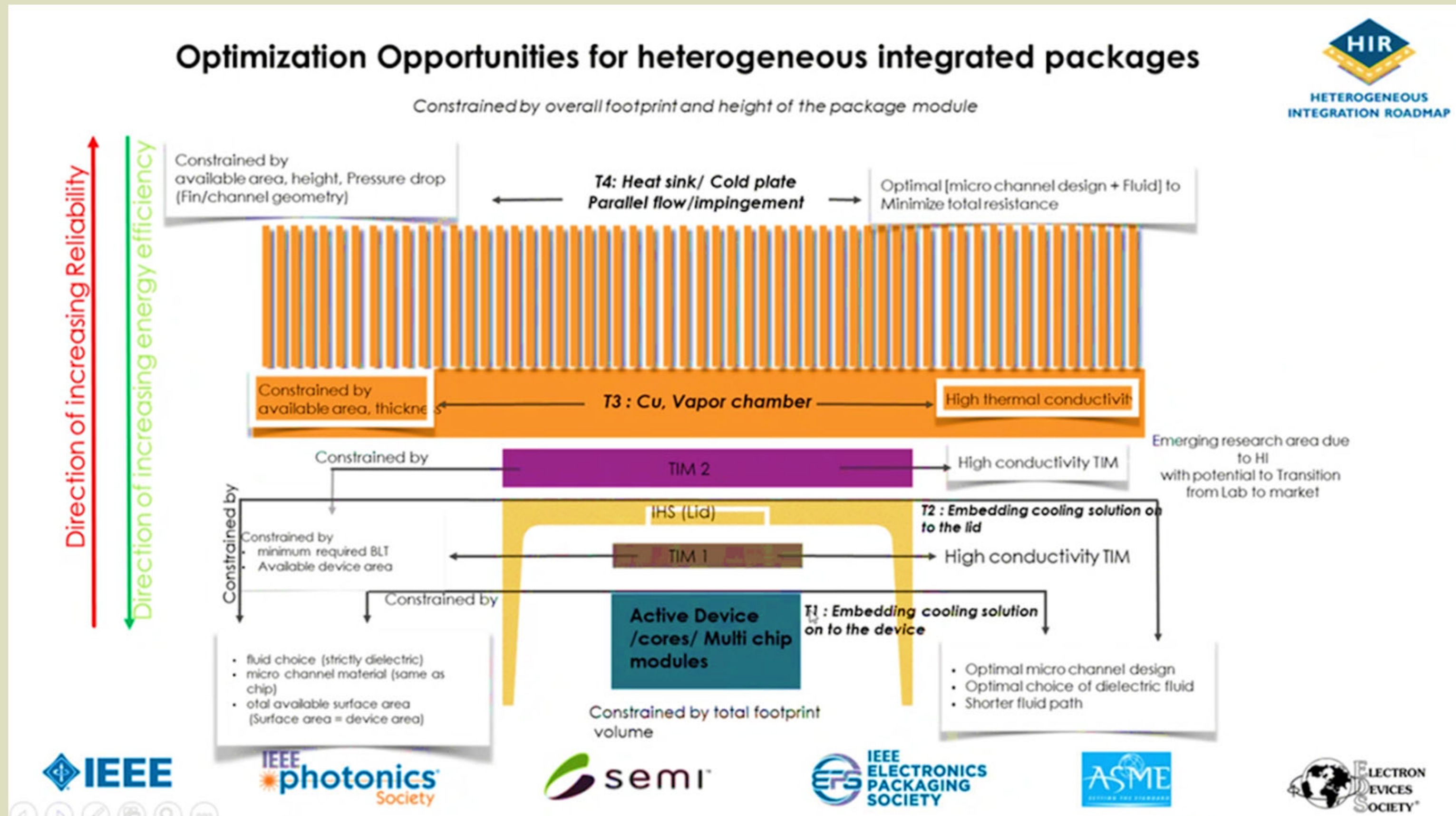
Package HIR



Summary

- High-Bandwidth test access required for compute chiplets at all test insertions
- Device data volumes increasing with Chiplet based HPC designs
  - UCIe-S as test phy >= 4 Gbps per lane (up to x16) – Wafer/mid-bond
  - SSN SDR/DDR SCAN test access – Wafer/package
  - HSAT SCAN fabric testing – Wafer/package
- Shift left requires access controlled through:
  - JTAG, I2C, GPIO, IEEE1838/1687, Bunch of Wires (BOW), etc
  - UCIe-S test port (SCAN/FUNCTIONAL/DEBUG)
    - UCIe sideband (800 MHz) for lower bandwidth interfaces
- Accommodate new SCAN BUS schemes for more parallel chiplet/die test
- Software based functional/scan test at engineering & HVM
- HVM High Power Delivery and Thermal Management
- UCIe 1.1 ESD spec: 30V charged-device model (CDM)
  - ESD Class 0Z handling; CDM going to 5V then 3V

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- 37 - HPD - Wafer-Level Stress: Current Flow Adaptive Control During Voltage Stress on an AI/HPC Device
- 65 - TM - HVM Test of UCIE-Enabled Chiplets for 2.5D and 3D Devices: The Case for a Dedicated Test Port
- 126 - TM - Utilizing DC Scale XPS256's Background Profiling Capabilities as an Effective Safety Measure in Production and Debug Tool in Engineering
- Advantest Voice 2021 Paper
  - 161-TM-V93000 HSIO Loopback - The Challenges and Obstacles of Testing 112 Gbps

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