TestConX™

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Mesa, Arizona
March 3-6, 2024

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Complex Challenges with Chiplets

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Elevate Semiconductor

Mesa, Arizona • March 3–6, 2024

Technology is Evolving

"Technology is a word that describes something that doesn't work yet."
-*Douglas Adams*

https://en.wikiquote.org/wiki/Douglas_Adams

What is a Chiplet?

- **Basics:** Chiplets are modular components of a processing unit within a larger circuit.
- **Architecture:** Non-heterogeneous, suitable for complex device structures.

- **Applications:**
  - **Computer Processors:** Enhances core count.
  - **Mobile Devices:** Boosts power efficiency and processing capabilities.
  - **Automotive:** Integral for microelectromechanical systems (MEMS) and processing tasks.
  - **Data Centers**: Improves memory speed and efficiency.

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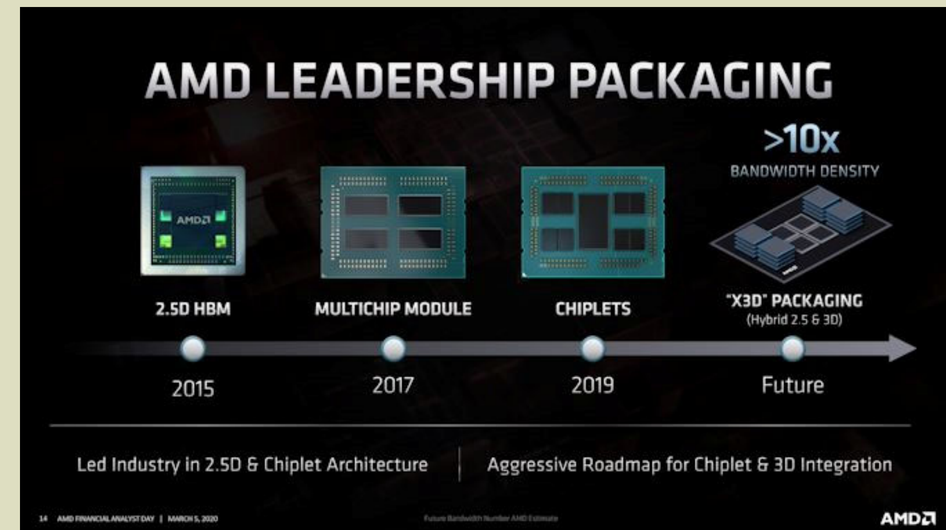
SLO

Why Do We Need Chiplets?

Advantages of Chiplet Technology

- **Flexibility:** Enables the creation of versatile, customizable modular chips.
- **Performance:** Utilizes specialized processors for optimized task execution.
- **Innovation:** Expands engineering boundaries beyond what was previous possible.
- **Reuse:** Chiplets can enable reduced development cost as each chiplet can be used like a “lego block” and combined to create different product solutions



https://www.anandtech.com/show/15590/amd-discusses-x3d-die-stacking-and-packaging-for-future-products-hybrid-25d-and-3d

Slide 4

SL0 Add reuse - e.g. mix and match approach

Simon Leigh, 2024-02-20T00:39:03.918

What Challenges Do Chiplets Bring?

Challenges to Testing Chiplets- Probe

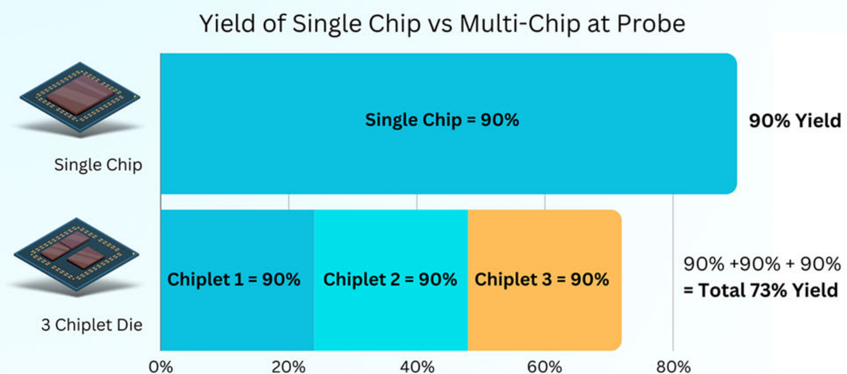
Importance of probe: When putting together multiple die, it is important to make sure everything works before it is assembled

Pre-assembly Testing: Essential for verifying functionality before integration.

Yield Impact: A single faulty chiplet can significantly reduce overall yield.

Example: 90% yield per chiplet → 73% yield for a 3-chiplet system.

Yield and coverage at probe must increase as chiplet complexity goes up



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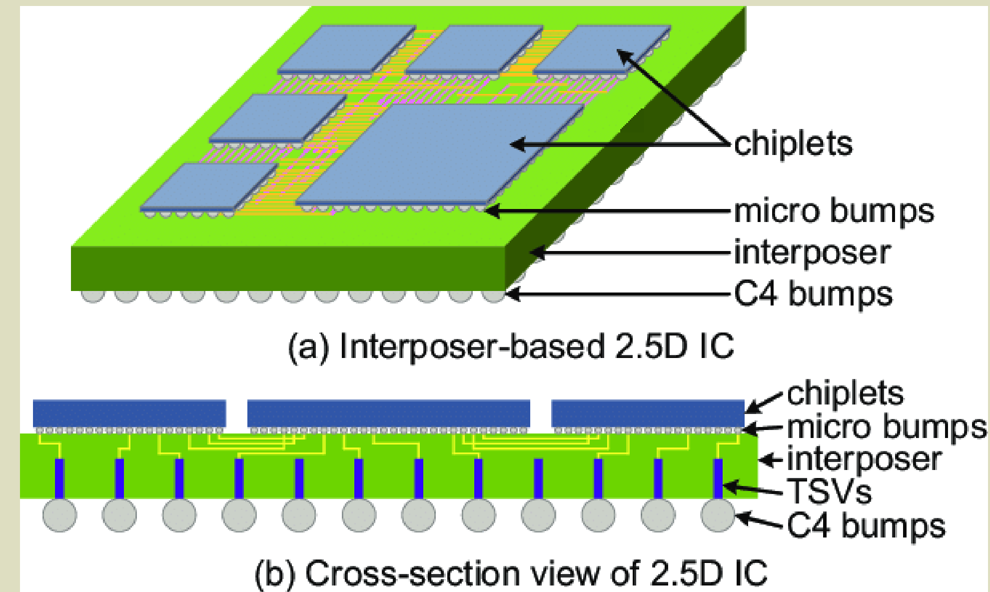
Challenges to Testing Chiplets- Signal Integrity

Testing Challenges with Chiplets come down to intra-chiplet signals

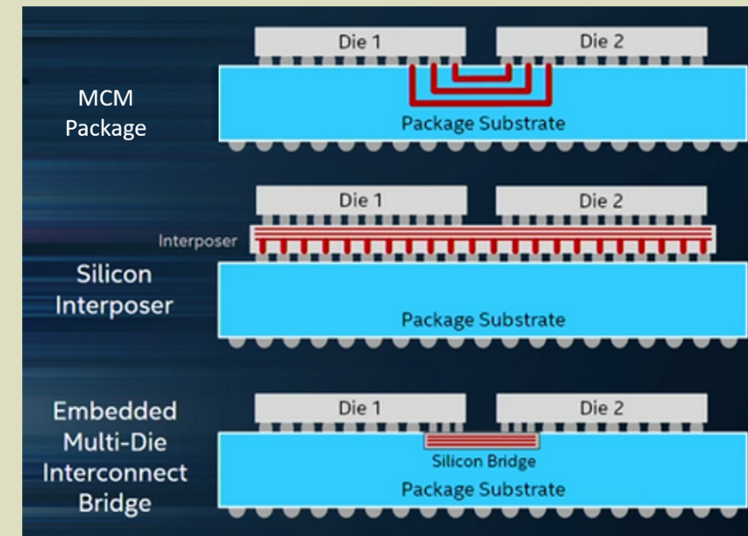
- **High Speed:** Standards such as UCIE are designed to be very high speed (32Gbps)
- **Signal Isolation:** For power reasons intrap-chiplet buffers are typically designed to drive very short lines in order to communicate only between chiplets and are not suitable for driving the much larger load of a tester
- **Testing Difficulty:** Current best solutions involve testing with loopback, lower speeds or dedicated test ports. All of these are workarounds that help, but do not provide a complete solution



https://www.researchgate.net/figure/25D-chiplet-integration-with-an-interposer_fig1_333334245

Challenges to Testing Chiplets- Complex Interconnects

- Chiplets often serve as protocol translators.
- They enable communication across multiple interfaces in the final product.
- Protocols require die-level verification.
- At-speed testing is often necessary despite signal loss because a protocol simply may not be designed to work at lower speeds
- Testing at speed is challenging due to chiplets' low drive strength.
- Protocols



https://www.eejournal.com/article/from-chiplet-to-chiplet/

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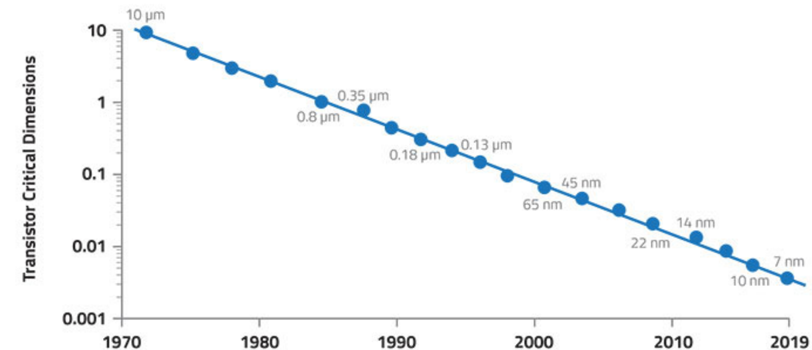
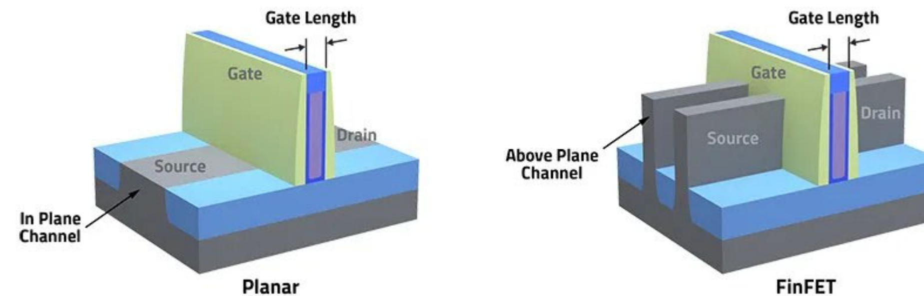
Challenges to Testing Chiplets- Complex Designs

Complexities in Chiplet Design Testing

- Chiplets often utilize advanced FinFET or GAA technologies. SL0
- These methods result in highly complex designs.
- Testing is slower and more complicated due to design intricacy.
- I/O speeds may need reduction to maintain signal integrity and address interconnect issues.





https://semiengineering.com/scaling-up-and-down/

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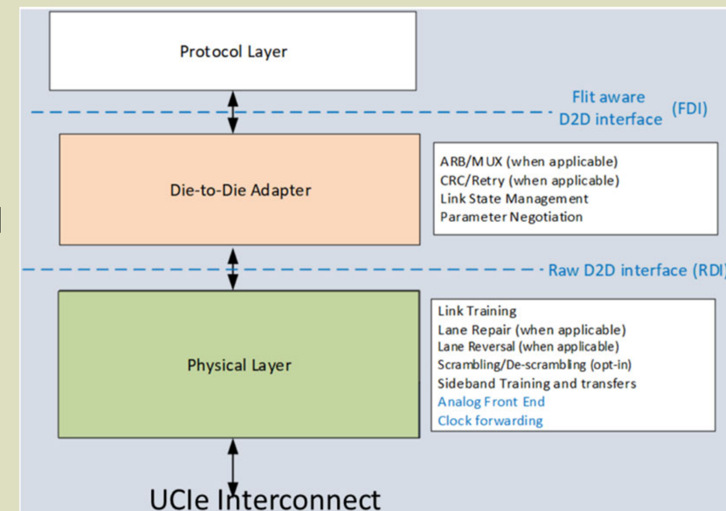
Slide 9

SL0 Not sure what to say here, are we trying to say that complexity means just bigger data? Larger scan patterns and so on - in which case that should be on BIST?
Simon Leigh, 2024-02-20T00:55:29.650

Challenges to Testing Chiplets- Throughput

I/O Count

- Chiplet based products often use far more I/O's than monolithic parts as many I/O's are purely for intrachiplet interconnect
- HBM for example is a memory bus that can be instead of a DDR link when using chiplets. It uses 1024 bit wide bus instead of DDR's 64 bits.
- While parallel testing of multiple dies is ideal for efficiency, this may be a limitation without rethinking how testers need to be built
- Test solutions will necessarily have to become more dense to support chiplets with orders of magnitude more capability
- As the channel count of testers increase to add this capability, the power efficiency of solutions must likewise increase even as the speeds and specifications increase in difficutly.



https://www.uciexpress.org/_files/ugd/0c1418_c5970a68ab214ffc97fab16d11581449.pdf

Challenges to Testing Chiplets- Power

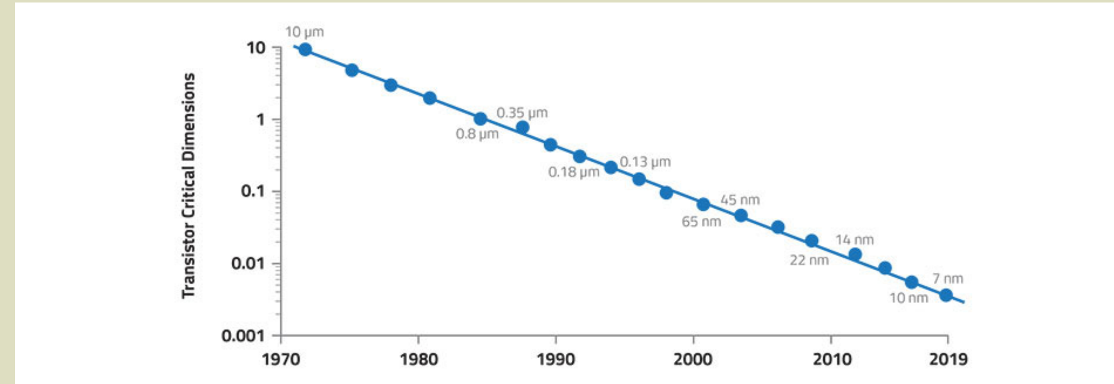
As advanced nodes continue to lower in geometry complexity increases, while operating voltages lower.

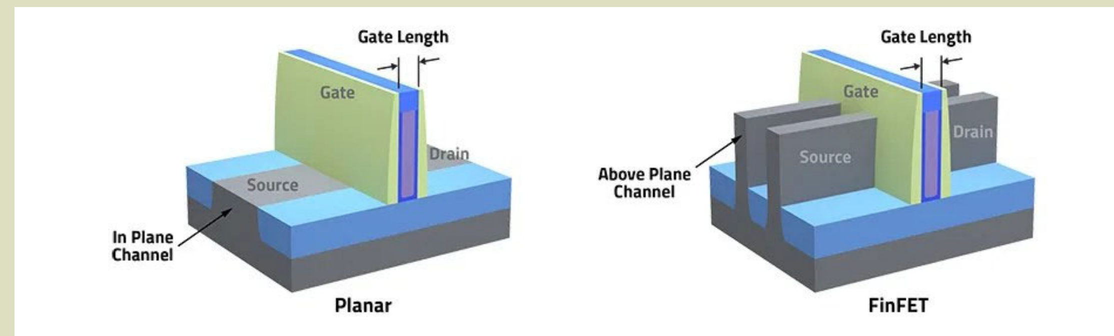
AI has been a big driver in new processor designs often with very high currents.

Low voltages push a bigger challenge for power supplies in terms of droop/kick which can be a major factor in resultant yields.

Power supplies at probe also need to be smarter and better controlled because:

- Connectivity is more important as circuits may not be connected to a full plane or power bus and rely on individual bumps and expect those to be well connected to a plane in the package
- Probe needles can be damaged when current limits are exceeded and poor
- Higher currents coupled with higher pin counts means more power and more power supplies. Density and efficiency is again the concern!



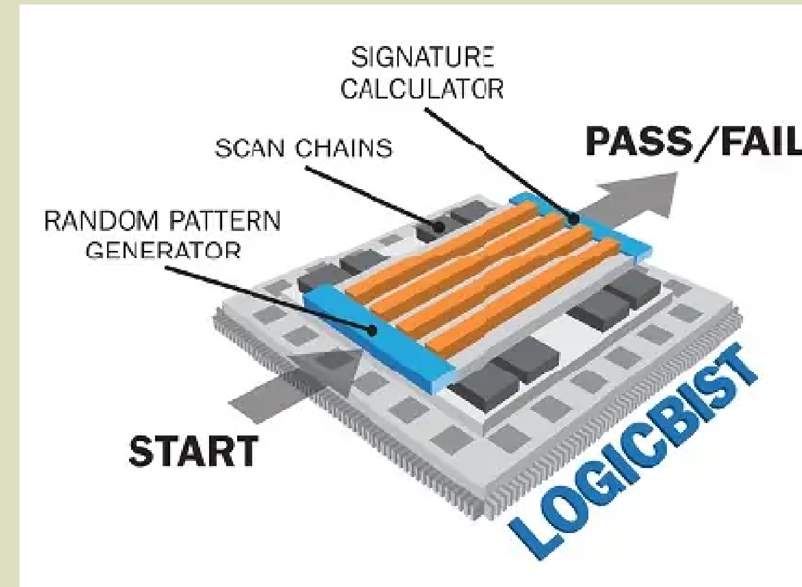


https://semiengineering.com/scaling-up-and-down/

Challenges to Testing Chiplets- BIST

The complexity increases also affect BIST

- Lower geometries and increasing design complexity means increased challenges for BIST
- SCAN data will get larger and becomes a challenge to get on/off chip
- More BIST circuits are required for circuits that can not be handled by current test solutions
- Standards and problems may rapidly evolve faster than the rate at which test solutions can be launched.
- Test is increasingly done in IC design prior to Test engineers and Test Vendors getting involved. If you're not part of the conversation you can't be part of the solution



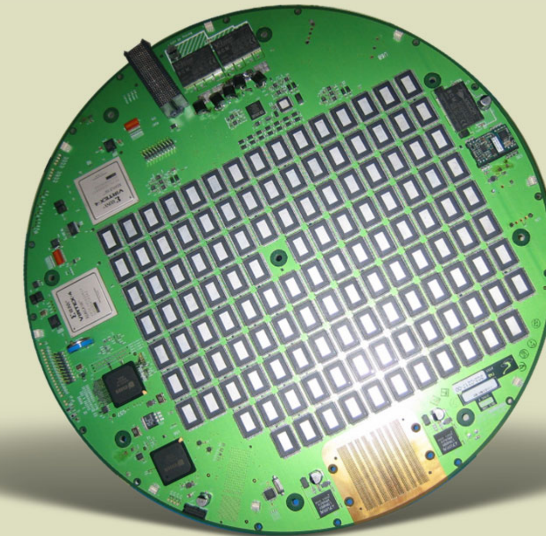
https://www.electronicdesign.com/technologies/embedded/article/21204297/testing-two-birds-with-one-stone

How Do Chiplets Affect Elevate As a Supplier?

Chiplet-Based Testing- Improved Signal Integrity

Enhancing Test Quality with Improved Signal Integrity at Probe is the logical path forwards

- Integration of Pin Electronics/DPS:
  - Located on the probe card near the DUT means removing all the challenges and limitations of the tester
- Benefits:
  - Shorter and simpler signal routes.
  - Lower signal loss and better integrity.
- Testing Advantages:
  - Facilitates high-speed 'at speed' testing.
  - Leads to more thorough testing and higher yields.
  - Power Supply Stability - Minimized voltage droop.
  - Fewer false errors and enhanced test consistency.



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Chiplet-Based Testing- Reduced Tester Complexity

Optimizing Test Infrastructure with Advanced Probe Cards

- **Trade-off:** Increased probe card complexity can reduce required tester complexity.
- **Probe Card Customization:** Tailoring for each chiplet improves test performance and speed.
- **Cost Efficiency:** Simplified testers lower large capital expenses. Custom probe board based solution may be cheaper than universal tester based one that has to be higher performance.
- **Consistency Across Tests:** Probe card-originated signals ensure uniformity in 'copy exact' processes for different testers and setups. Increasingly we can shift to being agnostic about tester hardware

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Chiplet-Based Testing- New Solutions New Problems

Building out the tester onto the probe cards brings new problems:

Area – probe cards may not have any spare pcb area to add hardware

Cooling & Power – adding hardware requires power and cooling. Many testers aren't design to support this and long-term solutions may require more creative thinking at the tester level

Ease of use - Probe Card designers are more time constrained than those developing a card for a tester. Creating complex hardware and software to build out "traditional" tester functionality is likely not possible or cost effective.

These are problems ElevATE is familiar with as we develop next generation products that solve problems not currently served by the ATE market. We often have to customize our own test solutions to add the capability we need.

What is clear – current solutions will not scale cost effectively for where the semiconductor industry is going

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Chiplet-Based Testing- Building the Future

ATE Manufacturers should:

- Architect new tester generations with increased support for probe card based solutions – area, power, cooling and interconnect
- Focus on the system and software being the value add and become more agnostic on the hardware solution (linux not apple)
- Standardize software and hardware interfaces to enable quick TTM for probe card developers
- Not keep doing the same thing!

ATE ASIC Vendors should:

- Design new products with probe in mind
  - Product should be “plug and play”
  - Single power supply
  - Zero to no calibration
  - Standardized simple interfaces
  - No external components
  - Family of interchangeable parts that are easy to swap
  - Provide example PCB layouts, software, firmware

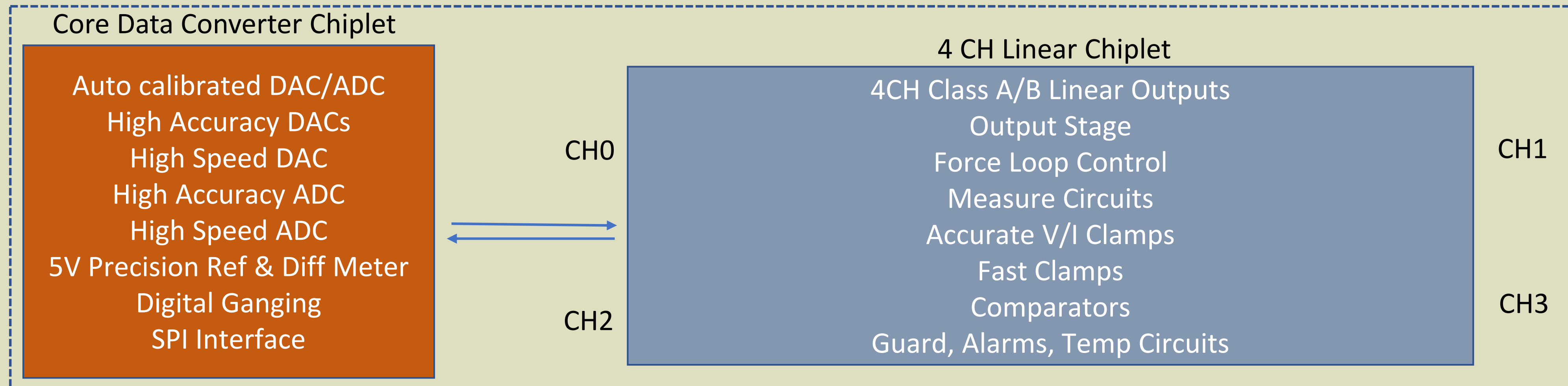
Probe Card Designers and Test Engineers should

- Think outside the box for new solutions
- Push your vendors for the infrastructure so that the sandbox is more useful

How Do Chiplets Affect Elevate As a Consumer?

How is Elevate affected As a Consumer?

Linear DUT Power Supply – Simple Chiplet Implementation



How is Elevate affected As a Consumer?

More Complex Implementation with Switching DPS (Class H)

Switching Power Supply Chiplet

Switching Class D Supply
with Envelope Tracking per channel

Core Data Converter Chiplet

Auto calibrated DAC/ADC
High Accuracy DACs
High Speed DAC
High Accuracy ADC
High Speed ADC
5V Precision Ref & Diff Meter
Digital Ganging
SPI Interface

4 CH Linear Chiplet

CH0
CH1
CH2
CH3

4CH Class A/B Linear Outputs
Output Stage
Force Loop Control
Measure Circuits
Accurate V/I Clamps
Fast Clamps
Comparators
Guard, Alarms, Temp Circuits

How is Elevate affected As a Consumer?

Complex SOC Implementation of Next Gen Pin Electronics

Regulators

Core LV Chiplet
- Auto calibrated DAC/ADC
- High Accuracy DACs
- High Speed DAC
- High Accuracy ADC
- High Speed ADC
- 5V Precision Ref & Diff Meter
- Digital Ganging

Reused PMU Support Chip
- Per Pin Parametric Measurement Unit
- Force and Measure Circuitry
- Comparators
- Clamping
- Alarms

MEMS Relays

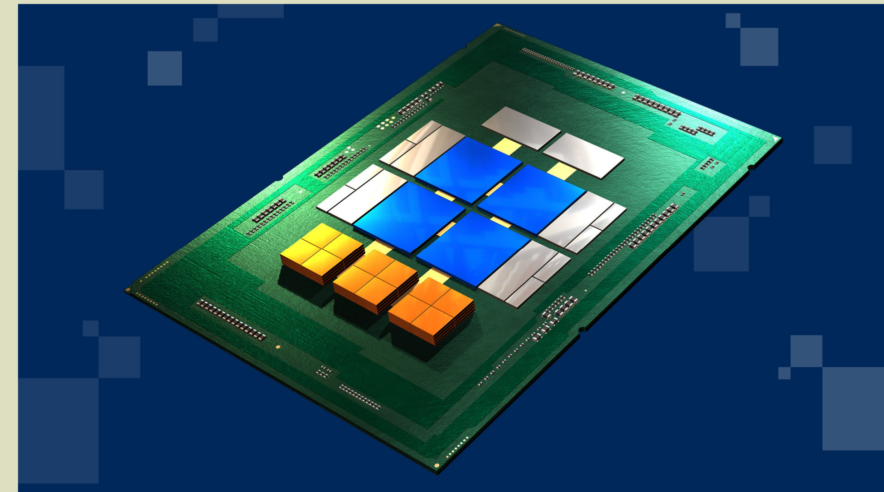
Memory

FPGA
- Pattern Generator
- Formatter

High Speed ASIC
- High Speed Driver
- Active Load
- Comparators
- Dynamic Timing Verniers
- Time Measurement Unit

Conclusions

- Chiplets are going to continue to be driving innovation into the future
- Chiplets are bringing on new challenges for test and probe
- ATE vendors and ASIC designers must adapt and architect solutions with chiplets in mind in order to offer real value added solutions



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