Addressing Test Challenges with Solid Contact Technology

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Johnstech®

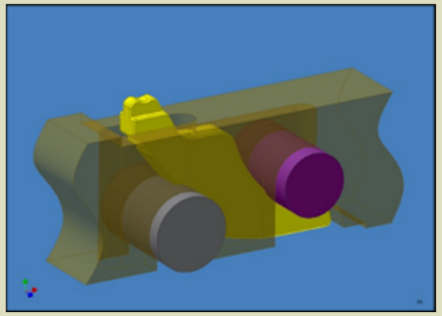
Agenda

- The Challenges and Solutions
  - Linearity, Gain and Noise in RF Amplifiers
  - Testing Devices Susceptible to Ground Inductance
  - Testing CRES-sensitive devices
- Evolution of Solid Contacts
  - New VROL Technology

About Solid Contact Technology

Solid Contact Technology

- Short, rigid, single-piece construction.
- Plated or monolithic variety.
- Wiping action on device.



Other Contacts Types

- Multiple components or flexing single piece construction.

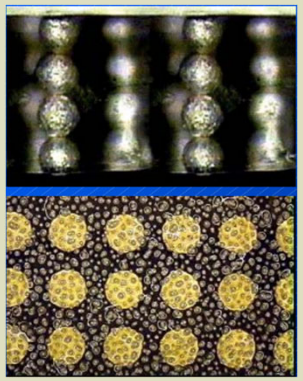


Figure 1 [1]

Figure 2 [2]

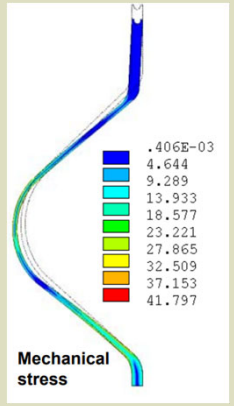


Figure 3 [3]

Testing RF Amplifiers

- The 1 dB compression point (P1dB) is the output power level at which the gain decreases 1 dB from its constant value.
- Once an amplifier reaches its P1dB it goes into compression and becomes a non-linear device, producing distortion, harmonics and intermodulation products.
- Accurately measuring the P1dB and gain are one of the most important tasks to verify specifications for power amplifiers, as it is up to this point that we consider an amplifier to operate linearly.

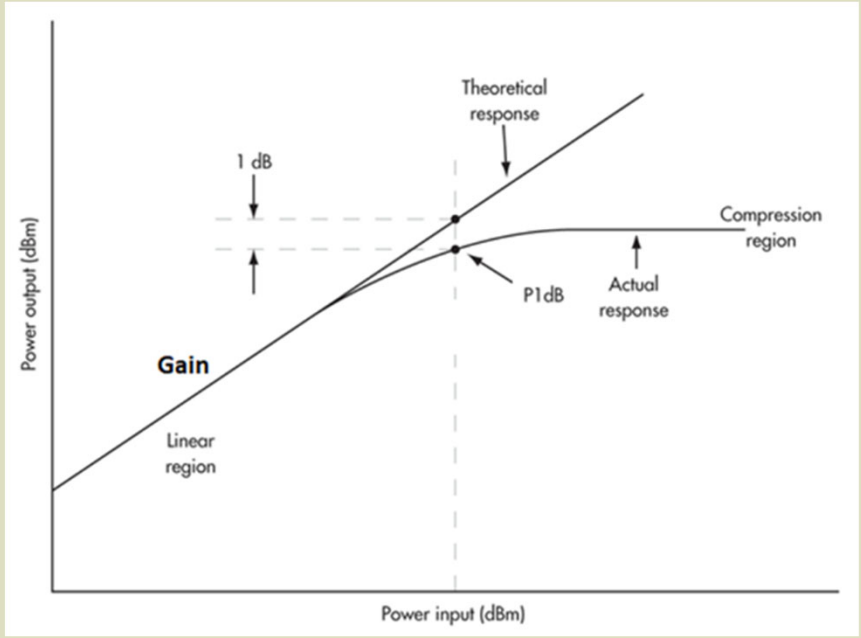


Figure 4 [4]

Testing RF Amplifiers

- Factors that impact measurement accuracy of P1dB and gain:
  - Source/load impedance mismatch
  - Noise figure (increases with losses incurred before the amplifier input)
  - Frequency Response

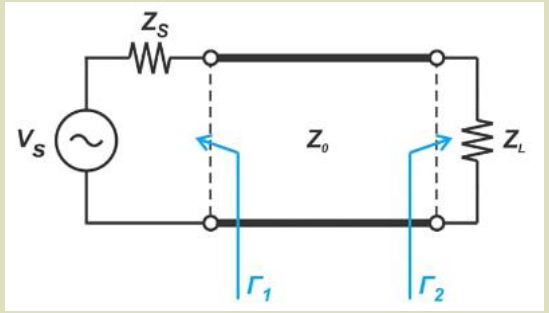


Figure 5 [5]

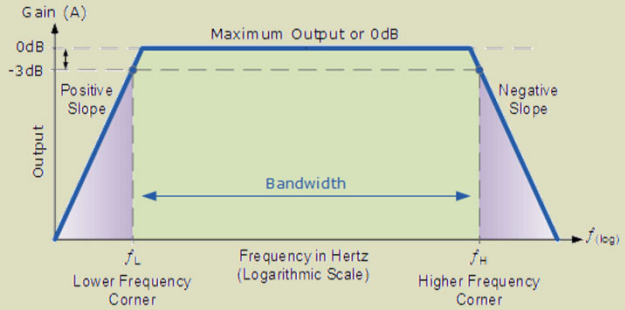
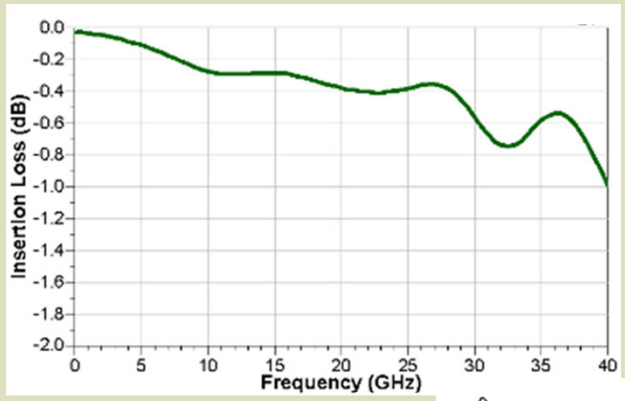


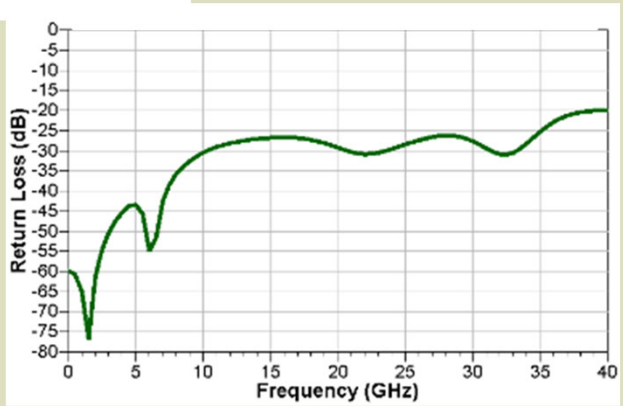
Figure 6 [6]

Select a contactor with
- low consistent CRES
- very low loss and well impedance matched across a wide frequency band

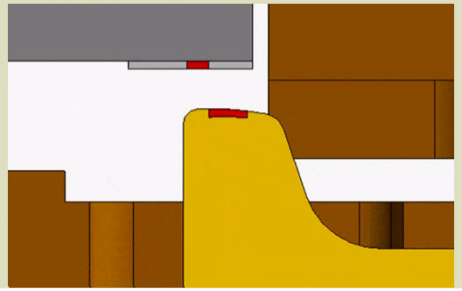
Solution for RF Amplifiers – Solid Contacts

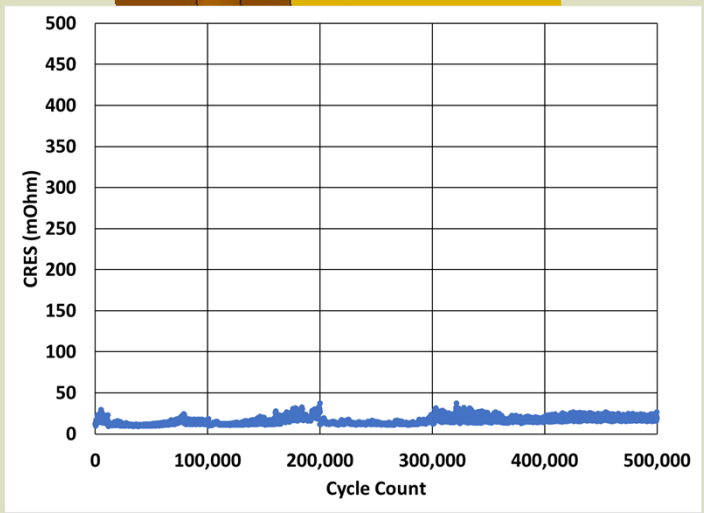
Low loss and matched impedance





Self cleaning scrub and low consistent CRES





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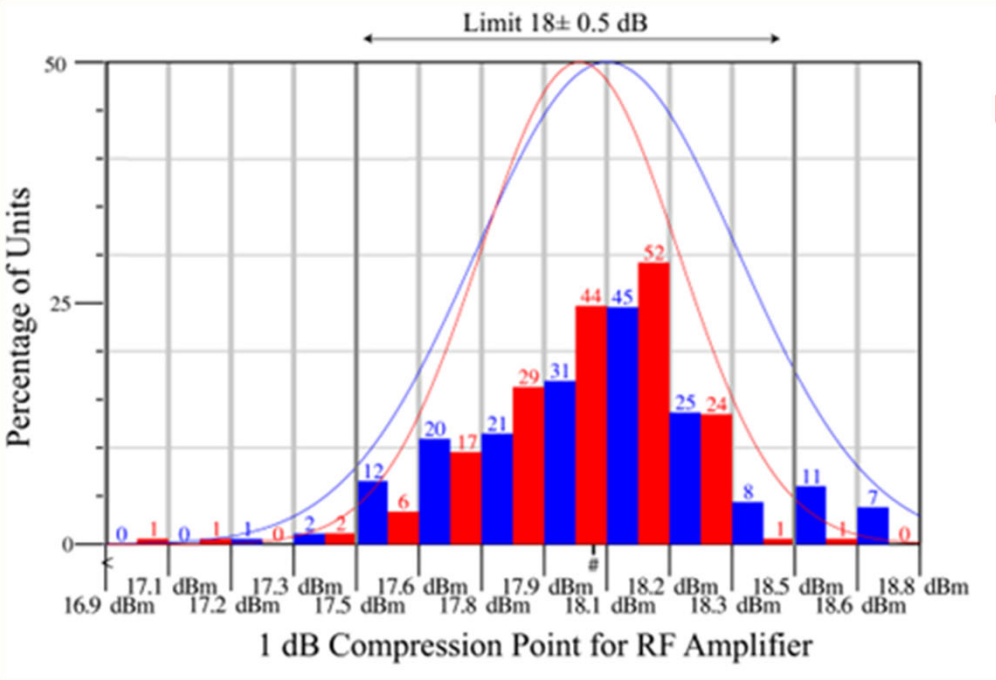
Customer Application #1
RF Amplifier 1dB Compression Point



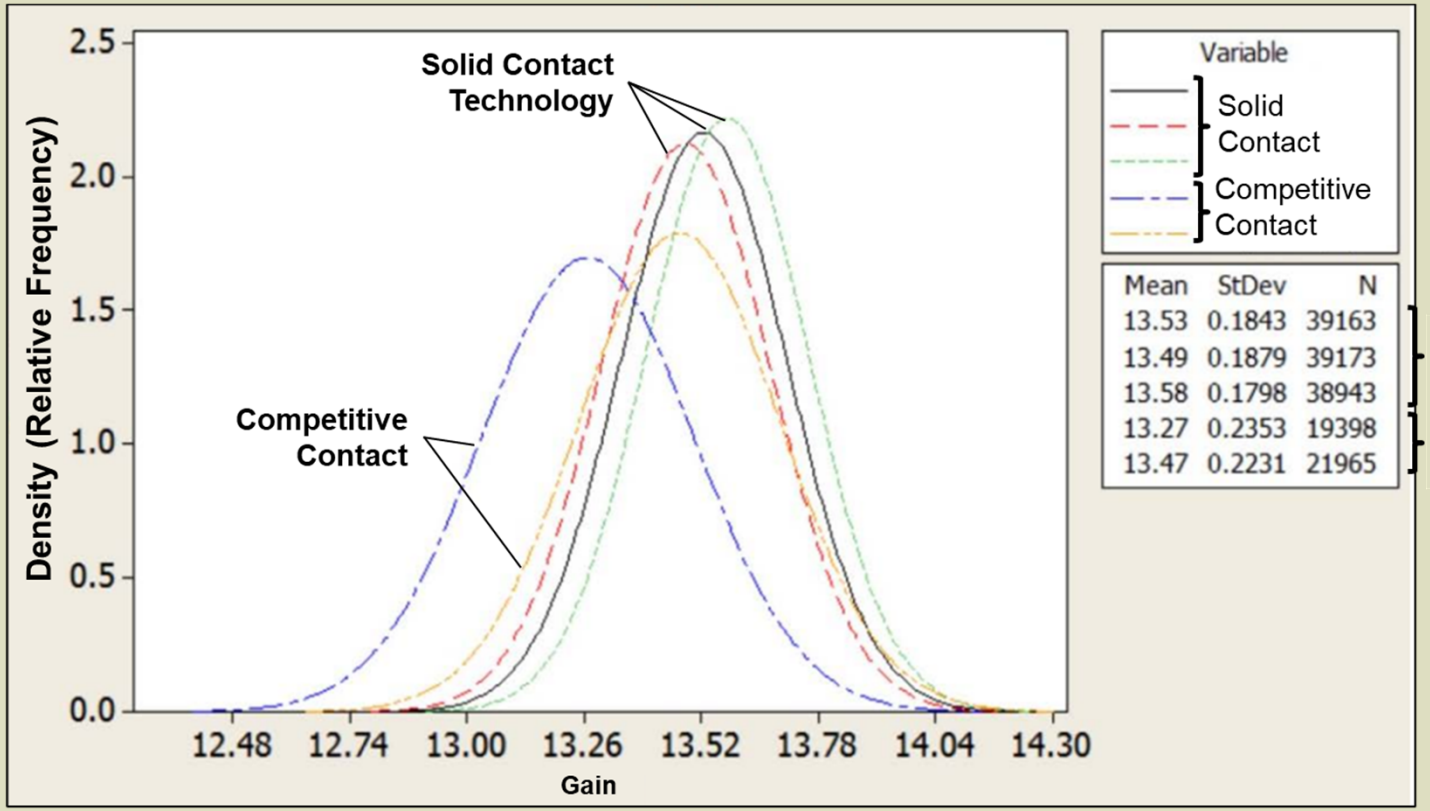
Solid Contact Technology

Competitive Contact

Yield Summary

Contacts	Solid Contact Technology	Competitive Contact
Pass	173	162
Fail	5	21
Total	178	183
Yield	97.2%	88.5%

Customer Application #2
Amplifier Gain



Mean	StDev	N	
13.53	0.1843	39163	Solid Contact
13.49	0.1879	39173	
13.58	0.1798	38943	
13.27	0.2353	19398	Competitive Contact
13.47	0.2231	21965	

Higher and more repeatable gain with solid-contact technology

Customer Application #2
Return Loss Performance

Return Loss Performance

	Mean	Stdev	N
Solid Contact Technology	-26.08	0.9766	39163
	-26.20	0.9862	39173
	-25.91	1.152	38943
Competitive Contact	-24.09	1.964	19398
	-24.30	1.514	21965

Solid contacts provided better matched impedance and more repeatable performance.

Effect of Inductance on Power Amplifiers

For Power Amplifiers, additional inductance leads to ground bounce, introducing voltage noise in the high inductance return path. [7]

The inductance will affect the efficiency and gain of the power amplifier.

- Efficiency decreases as output power increases
- Output power is reduced

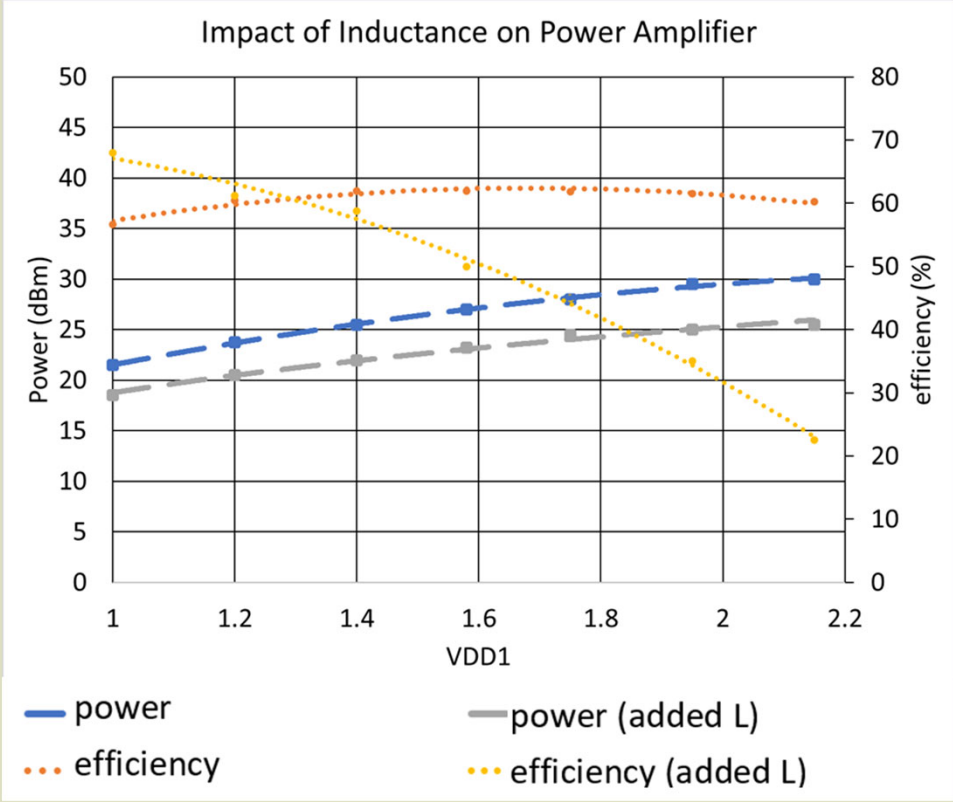
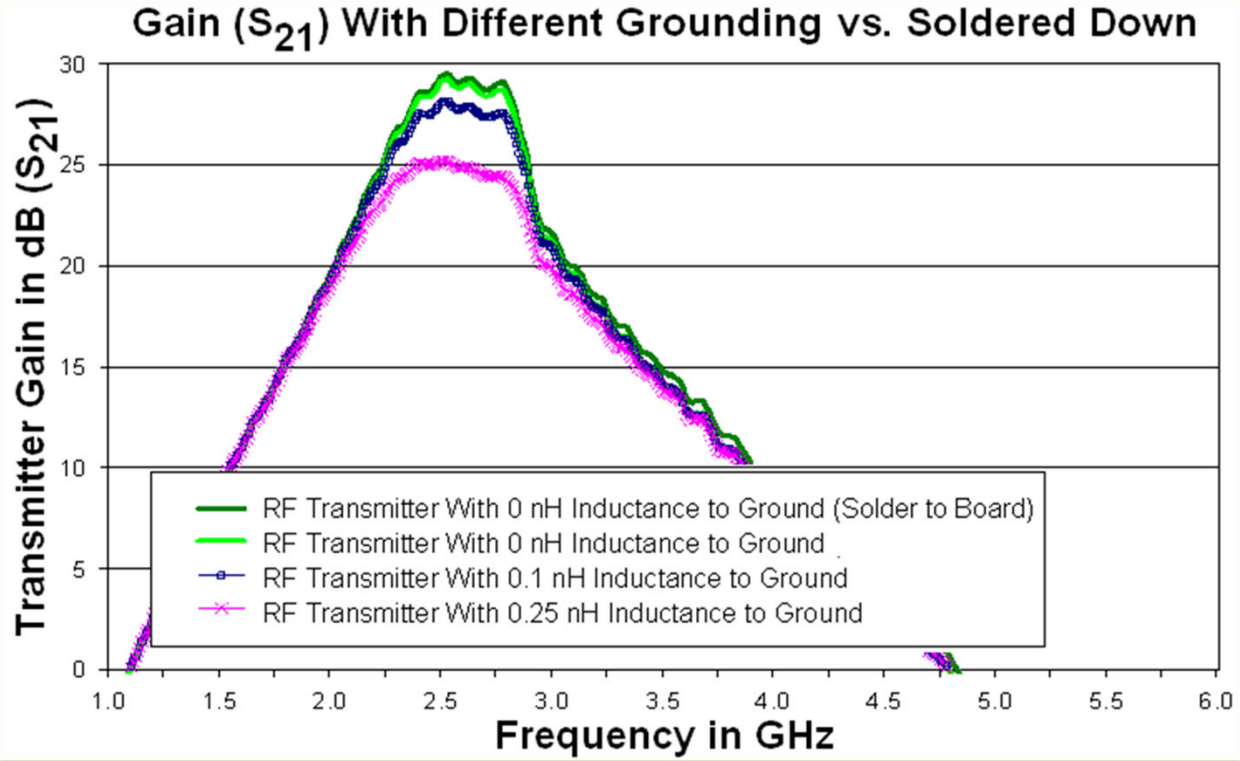


Figure 7 [8]

Effects of High Inductance on Power Amplifiers



Amplifier gains above 20 dB more sensitive to ground inductance

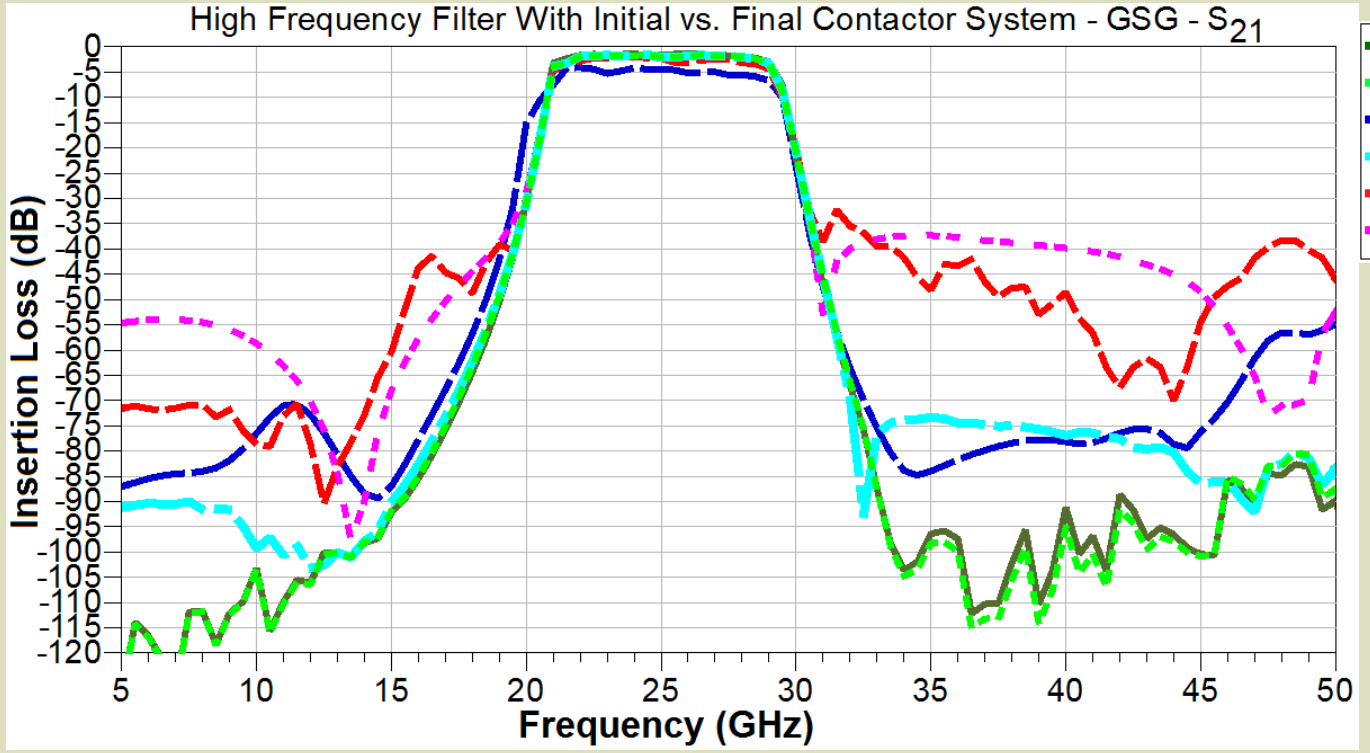
The higher the amplifier gain the more important it is to use short rigid contacts to maintain low inductance

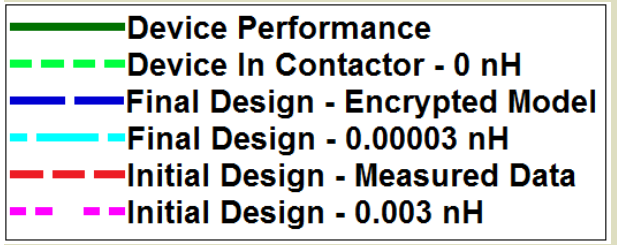
Devices that are Susceptible to Ground Inductance in Test System

- Power Amplifiers
- High Gain Amplifiers (Above 20dB)
- Filters Surface Acoustic Wave (SAW) and Bulk Acoustic Wave (BAW)
- High-Frequency Designs – Above 3GHz
- High-Speed Digital Designs – Above 10 GBits/sec
- High Gain Devices like RX and TX Devices (above 20dB)
- Voltage-sensitive devices – (i.e., High BIT count DACs and ADCs - Voltage per BIT small)

[9]

Impact of Ground Inductance on Bulk Acoustic Wave Filters

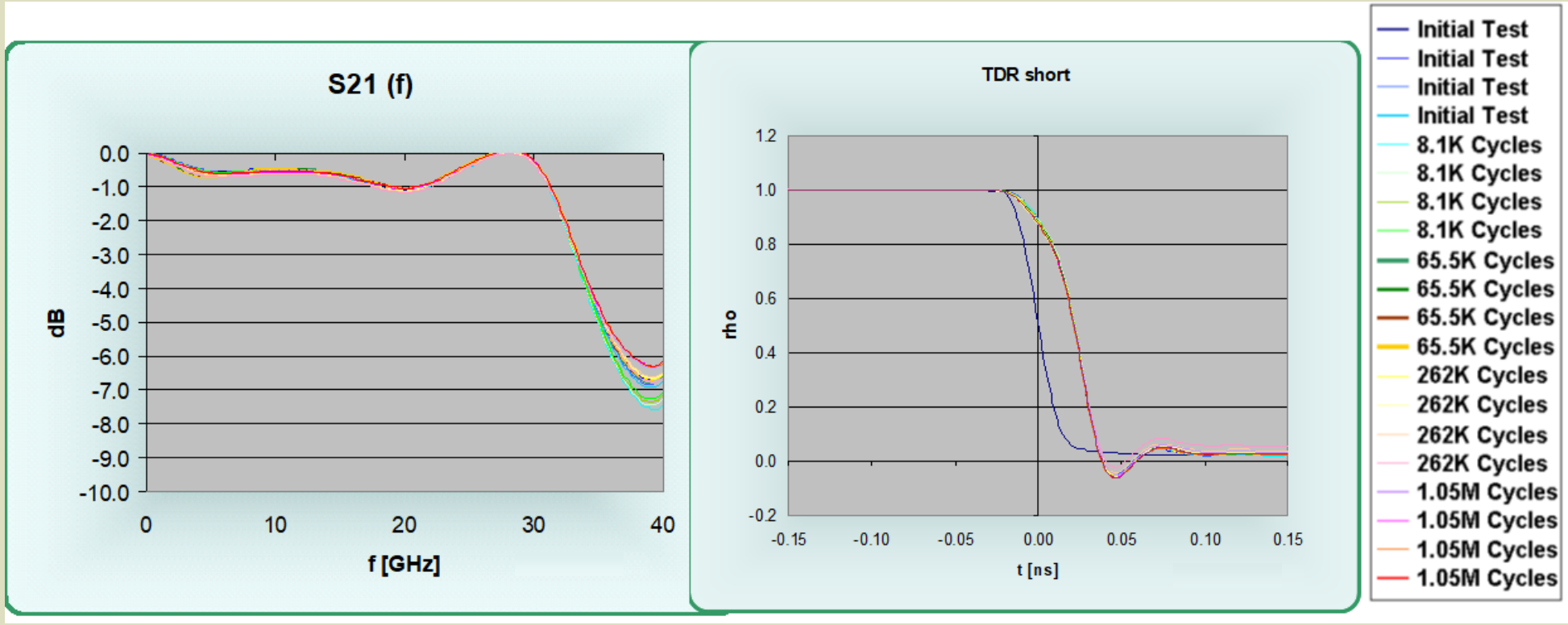




The steeper a filter skirt the more important it is to use short rigid contacts to maintain low inductance.

Figure 8 [9]

Electrical Performance Repeatable Over Life



ADC Errors – Input Resistance

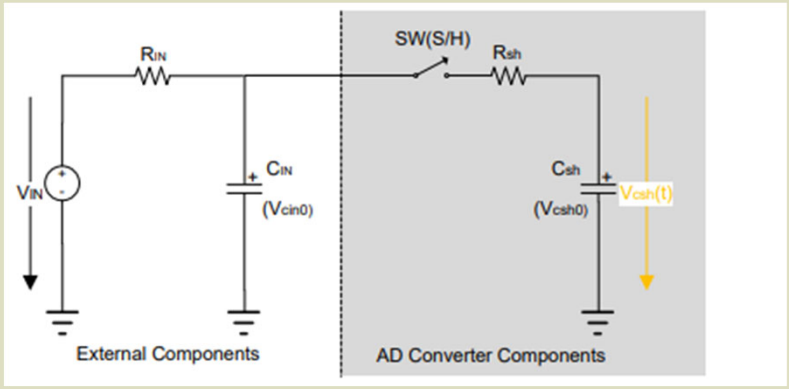


Figure 9 [10]

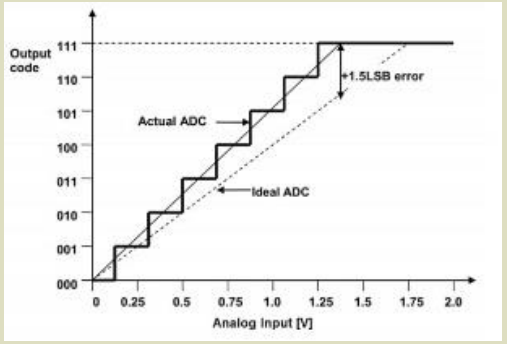


Figure 10 [11]

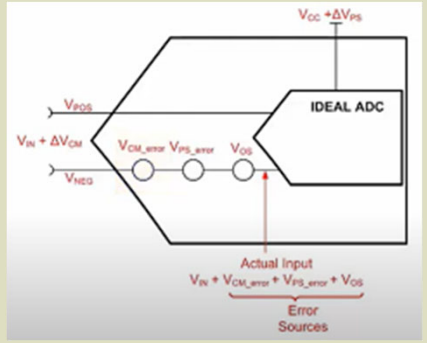


Figure 11 [12]

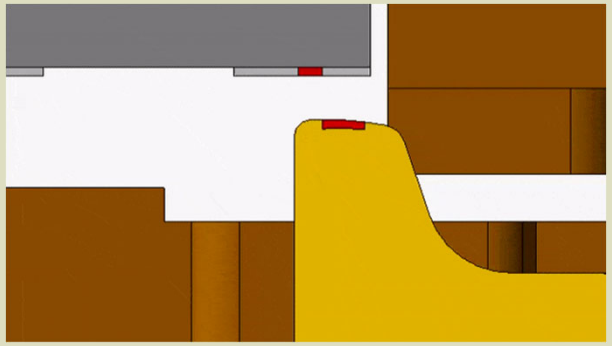
- Excessive analog signal source resistance can impact the settling time which introduces ADC errors
- With additional sources of resistance, the time required to fully charge the hold capacitor increases.
- Offset and Gain errors cause deviation from ideal performance due to increased source resistance.

High Resistance and Impact to Production

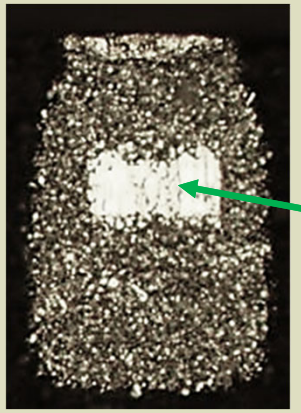
- Oxide-rich matte tin causes increased and highly variable contact resistance, resulting in lower yields.
- Matte tin from the package quickly builds up on the contact pins, which causes yields to fall, due to the increased variability of contact pin resistance values.
- While more frequent cleaning seems to counter the oxide buildup of matte tin, the increased contactor cleaning may also result in a throughput drop.

Oxide-Penetration with Solid Contact Self-Cleaning Scrub

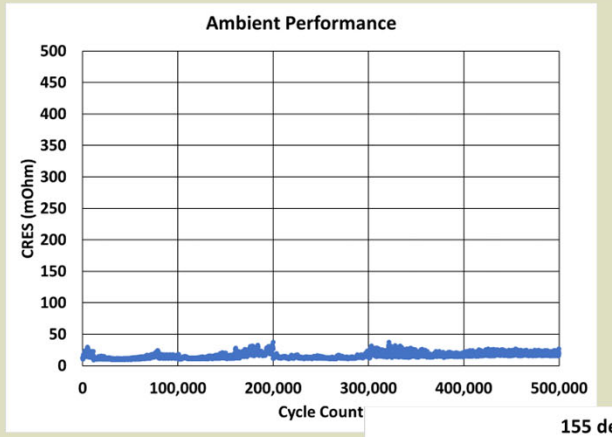
- Contactor with a self-cleaning feature can help reduce the frequency of contactor cleaning. A self-cleaning feature will also help delay amalgamation between the gold plating and tin.

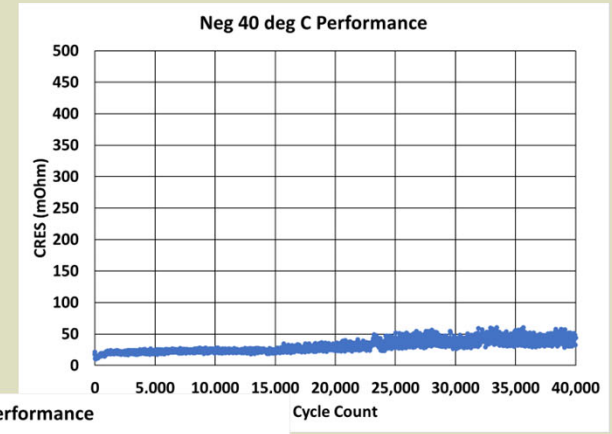


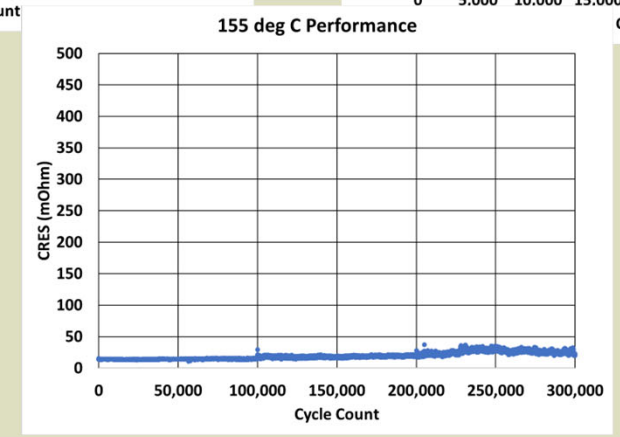
- Contacts that wipe across the surface of the I/O will remove oxides from the I/O and contact the tip on every test.



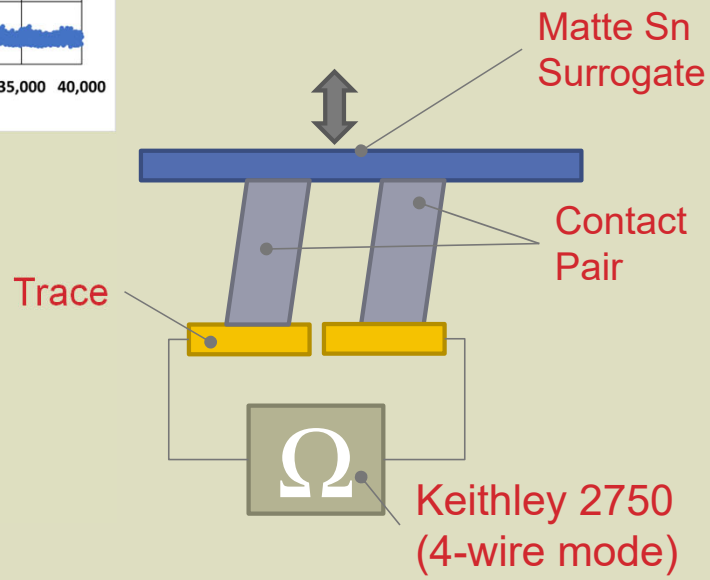
Tri-Temp CRES Performance





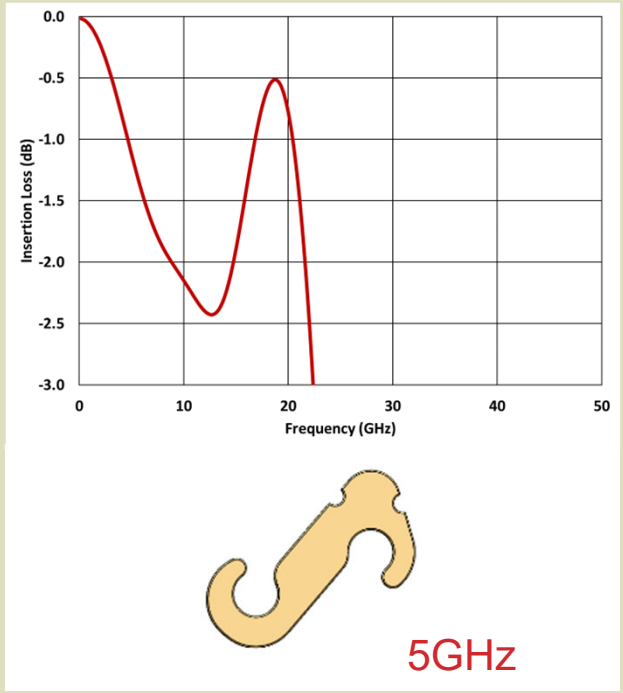


Self-cleaning wipe effective across temperature extremes

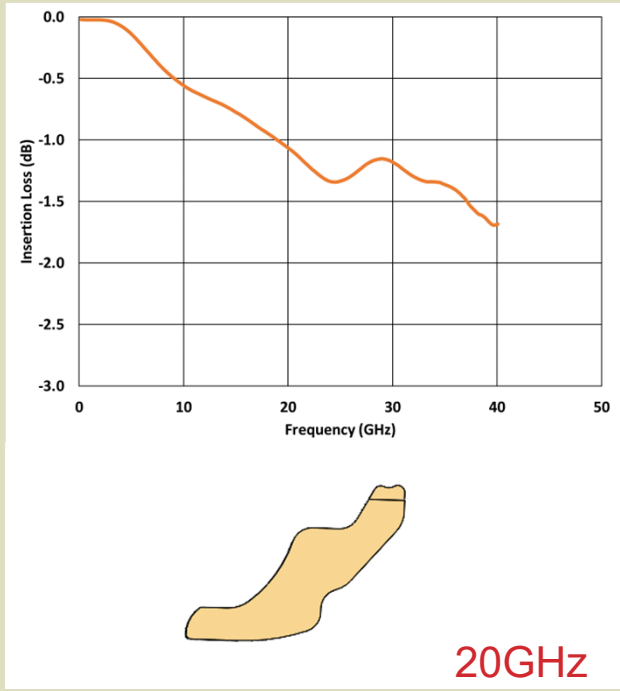


Evolution of Solid Contacts

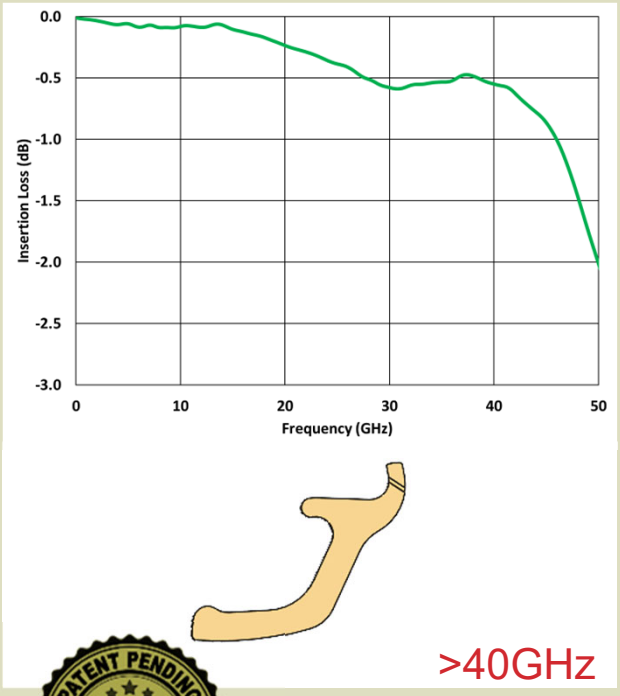
S-pin



ROL®



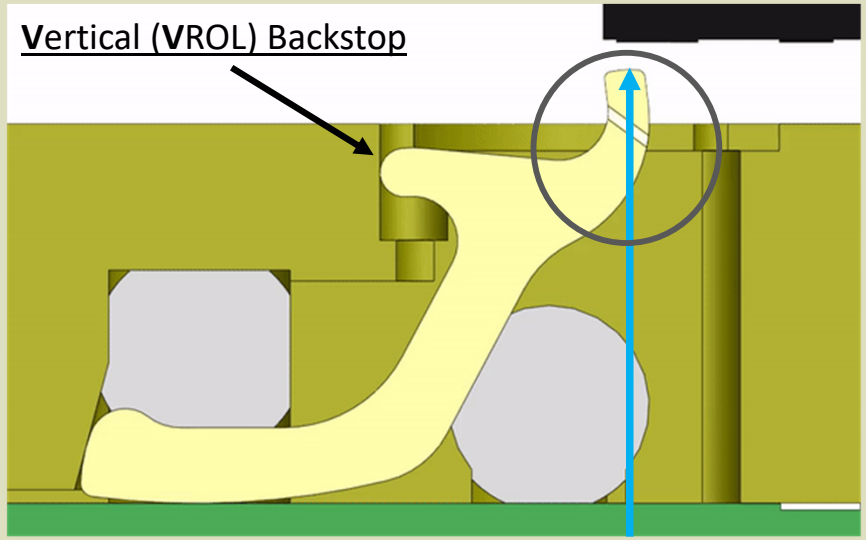
VROL®



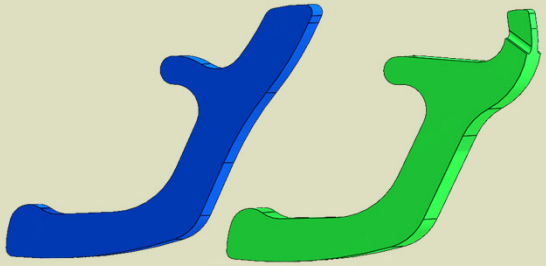
PATENT PENDING

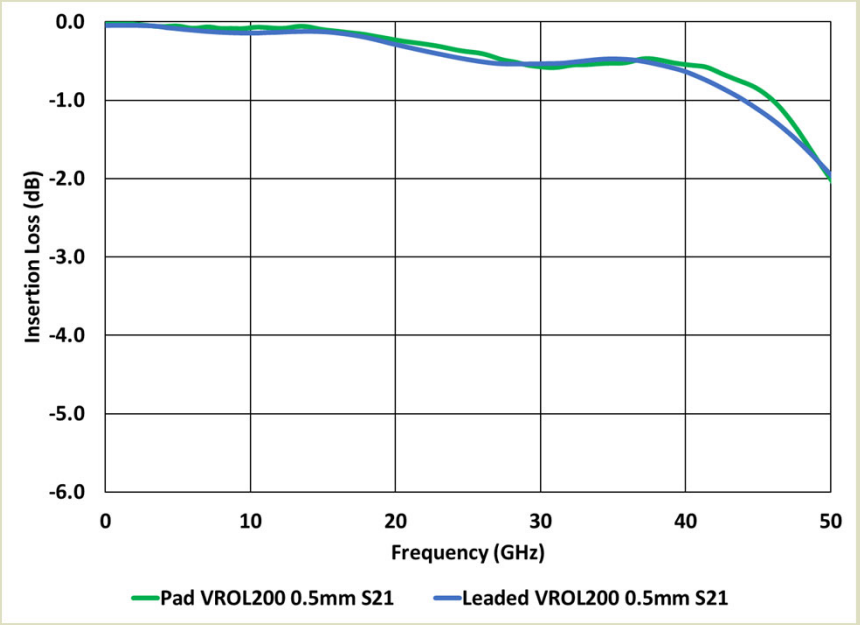
New VROL® Design
Flex-Proof Contact Alignment

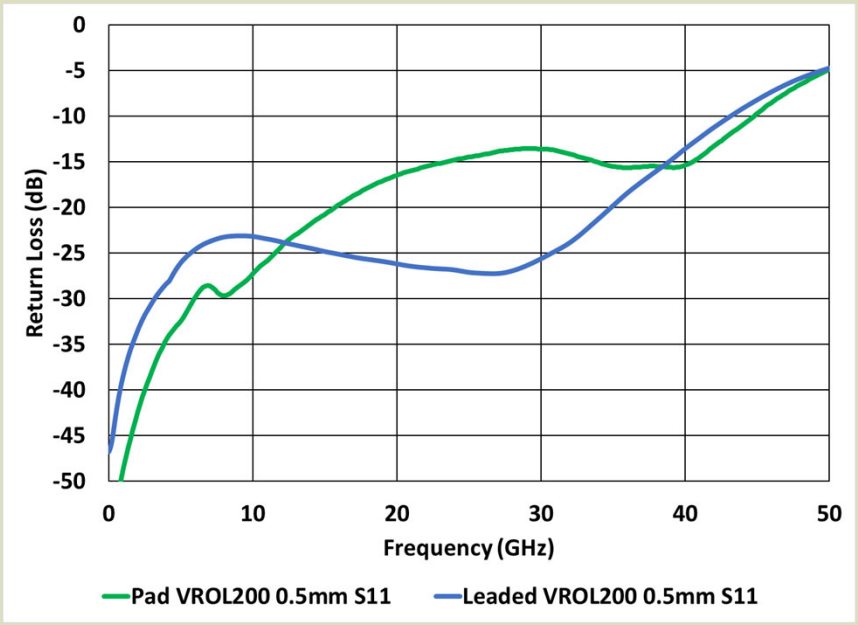
The new VROL® design has a vertical-back-stop eliminating potential positional tolerances due to PCB flexing. Thus, the tip is optimized for a consistent starting point on the device pad.



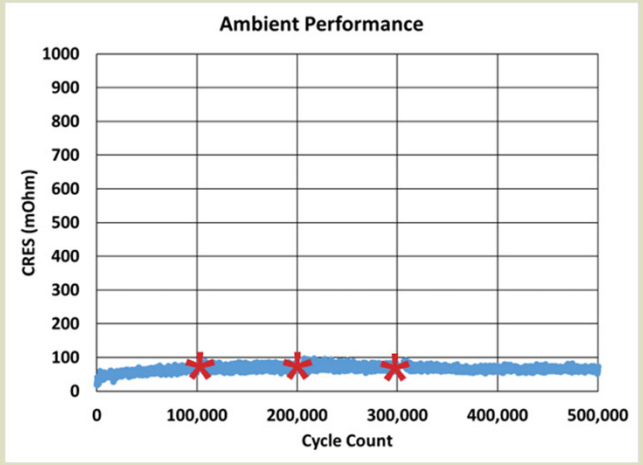
New VROL® Design Frequency Performance

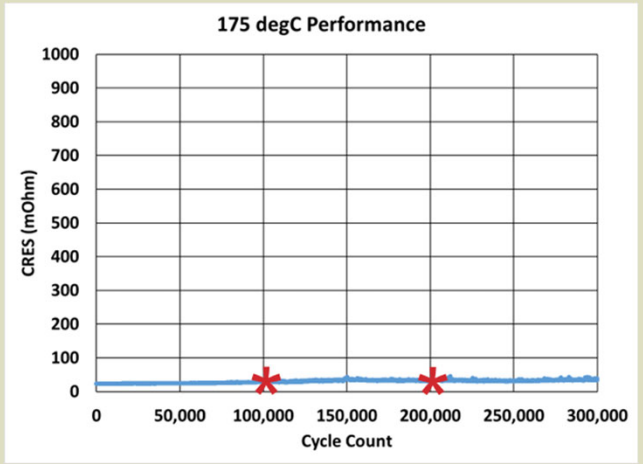


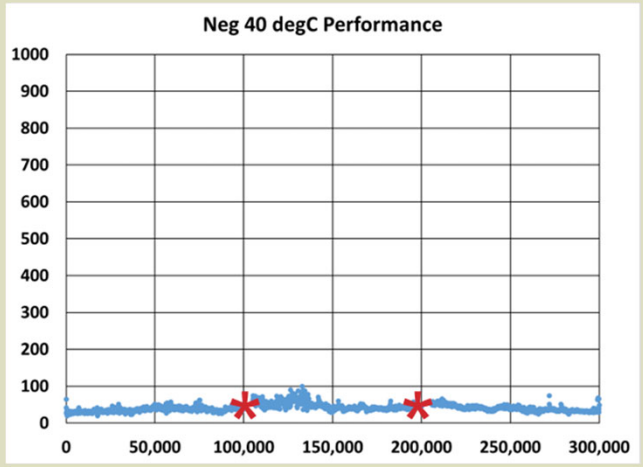




New VROL® Design CRES



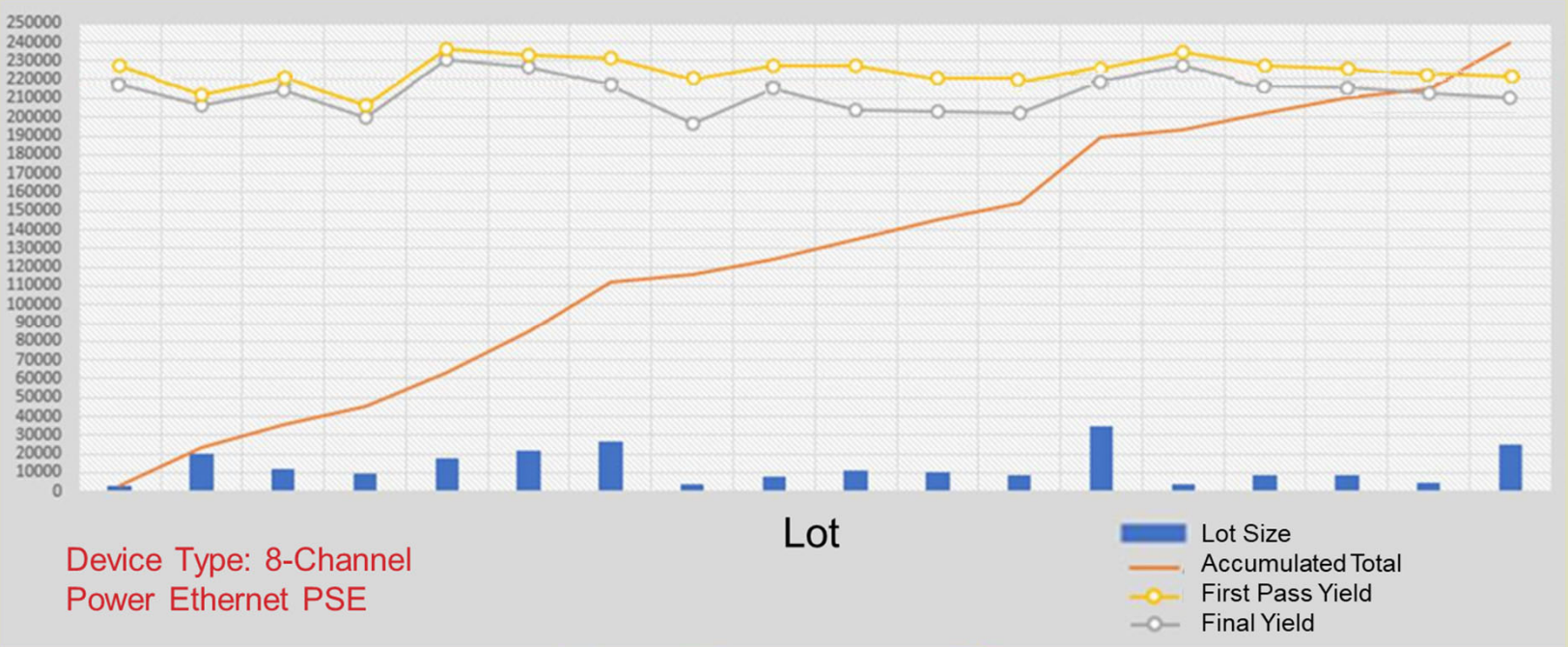




Self-cleaning wipe effective over temperature

*Contactor evaluated at intervals

VROL Customer Data



VROL Solid Contact Technology provided customer with < 2% Yield Gap, comparable to the expected performance from the incumbent ROL contactor. Data tracked over 240k devices tested.

Conclusions

- Single-piece solid contact construction offers minimum contact resistance
- Self-cleaning scrub maintains low contact resistance in production test
- Reduced contact height for lower ground inductance for filters, amplifiers and other sensitive to ground devices
- Rigid, one-piece contact provides RF, Digital and Cres repeatability

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