Qualification Execution Challenges with High Voltage Devices

Justin Wadley
Texas Instruments

Mesa, Arizona • March 3–6, 2024

High Voltage Spacing Standards

- High voltage trace lines have standardized spacing rules to prevent arcing of current between the traces
- Spacing standards cause limitations to your board layout and choice of sockets

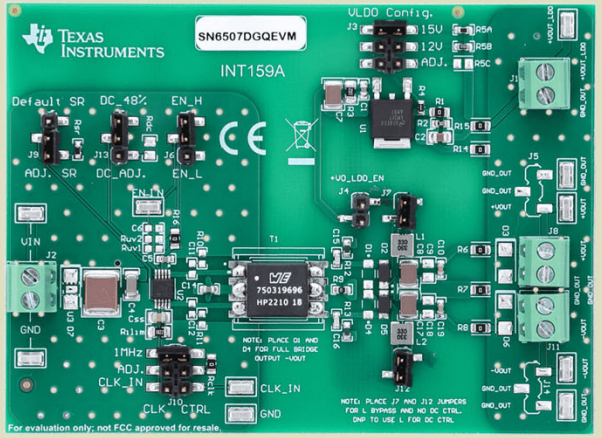
IPC-2221B Spacing Recommendations	
Uncoated Application - HAST/THB	
Voltage (V)	Minimum Spacing (mils)
>500	1 mil/Volt
251-500	492.1
171-250	252
101-170	126
51-100	59.1
0 - 50	2.5
Coated Applications - HTOL/PTC	
Voltage (V)	Minimum Spacing (mils)
>500	0.12 mil/Volt
301 - 500	31
101-300	16
0-100	5.12

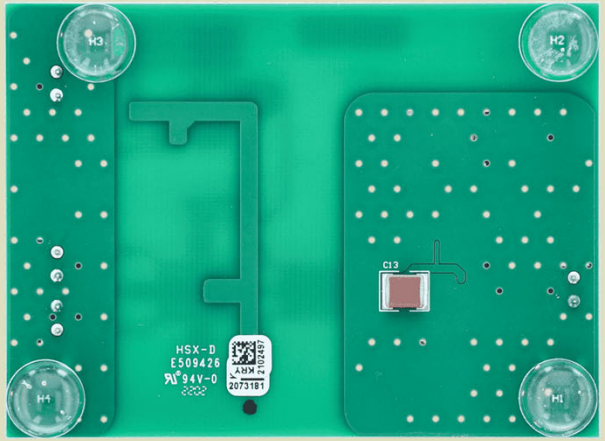
High Voltage Spacing Standards

- High Voltage qualification experiment
  - 200V devices tested in high stress lab environments with 0.1mm spacing showed no degradation significant to the DUT qualification.
  - Spacing did not cause an issue, printed circuit boards held up throughout 1000 hours of oven time with low leakage post stress
- This brings up the question, is following the standard relevant to ATE boards and Reliability Hardware?

High Voltage Spacing Standards

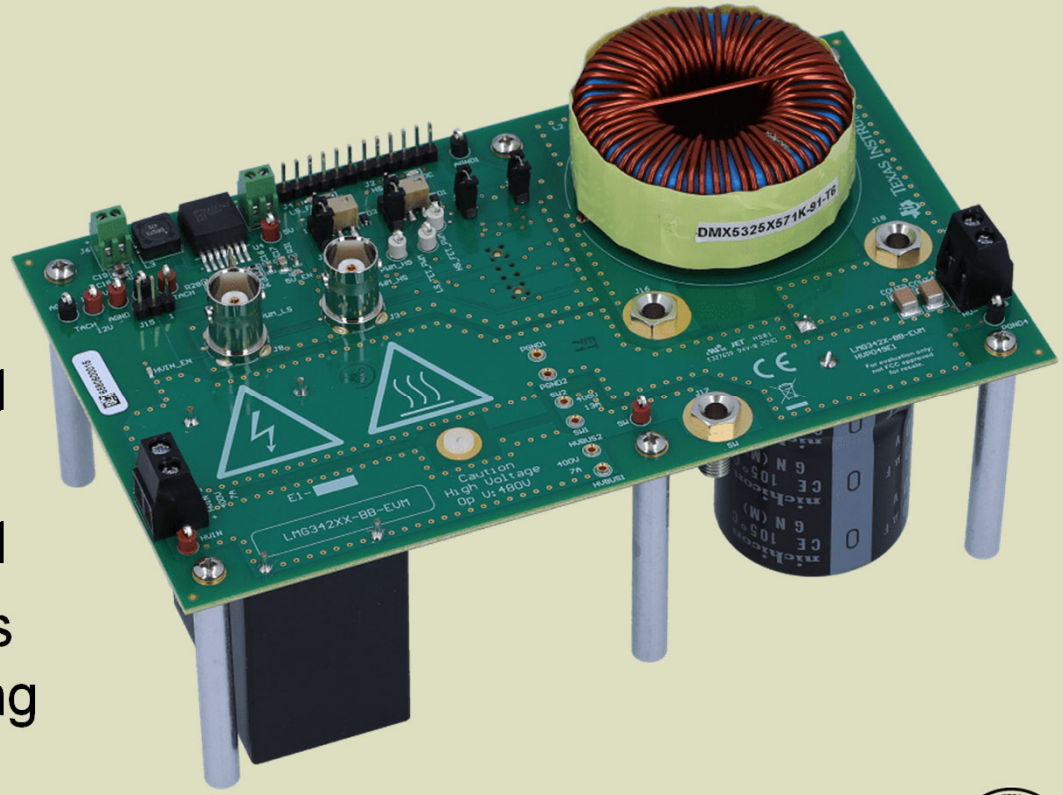
- IPC-2221B is over 10 years old
- Improvements in the board manufacturing process, as well as the quality of oven environments has made the standard obsolete
  - Lower risk of dirt and debris getting in the oven
  - Higher quality materials used in PCB





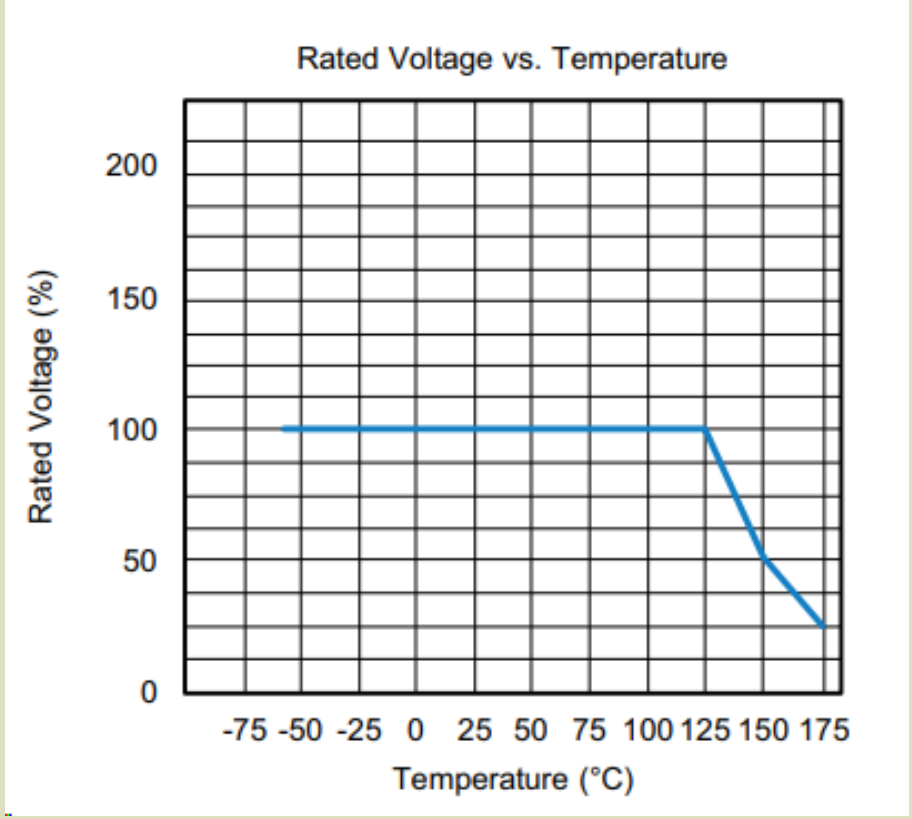
Component Selection

- Selecting high voltage components presents additional challenges
- High Voltage parts are more expensive and harder to find
- Temperature and Voltage derating must be considered
- Replacement of components can cause problems with long lead times



Component Selection

- Temperature Derating should be considered when picking components
- Consider ambient temperature vs junction temperature
  - HTOL oven temp 125C, but junction temp could be higher, degrading functionality of the part
- This can severely limit the number of options to choose from

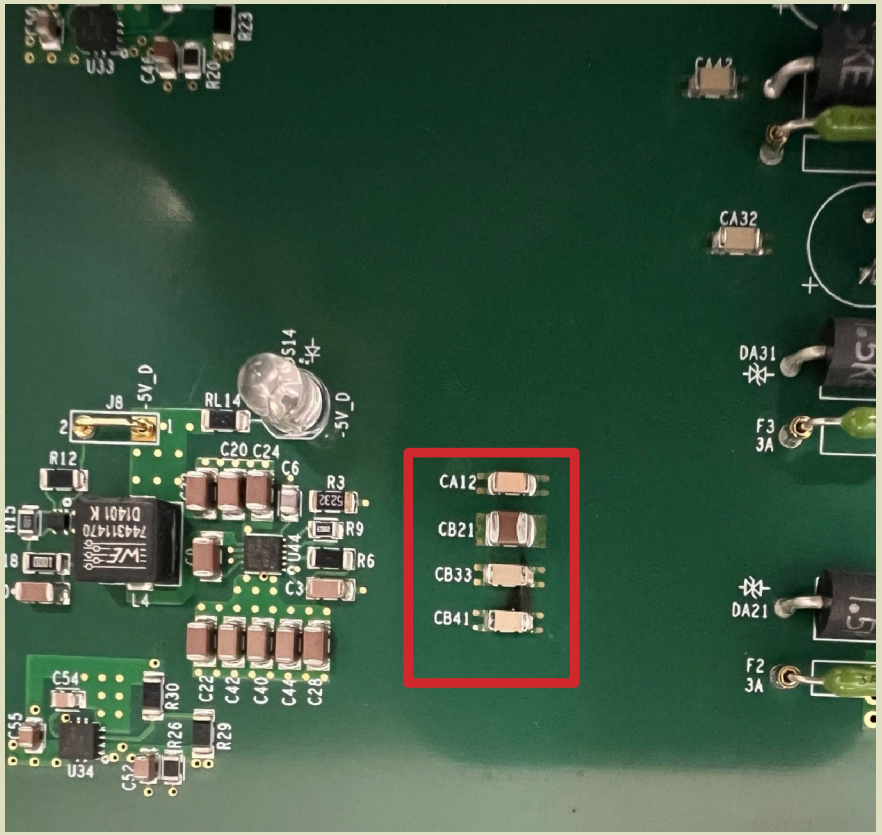


Component Selection

- Challenges faced on a 1000 hour HTOL at 125C and +/- 100V supplies
  - Only one capacitor rated for 100V and 150C was available within a 6 week lead time
  - Capacitors were failing at 25C with no devices on the board
  - Went through two separate batches of the part, both showing similar failures
  - Each time boards sent back to vendor is a loss of over a week

Component Selection

- Forced to remove all failing capacitors
  - Could lead to unstable power supplies
  - Device can enter undesired mode due to power supply fluctuation
- These parts are more expensive than a standard component
  - Lead times for replacement parts cause problematic delays
- Rate of failure has shown to be higher



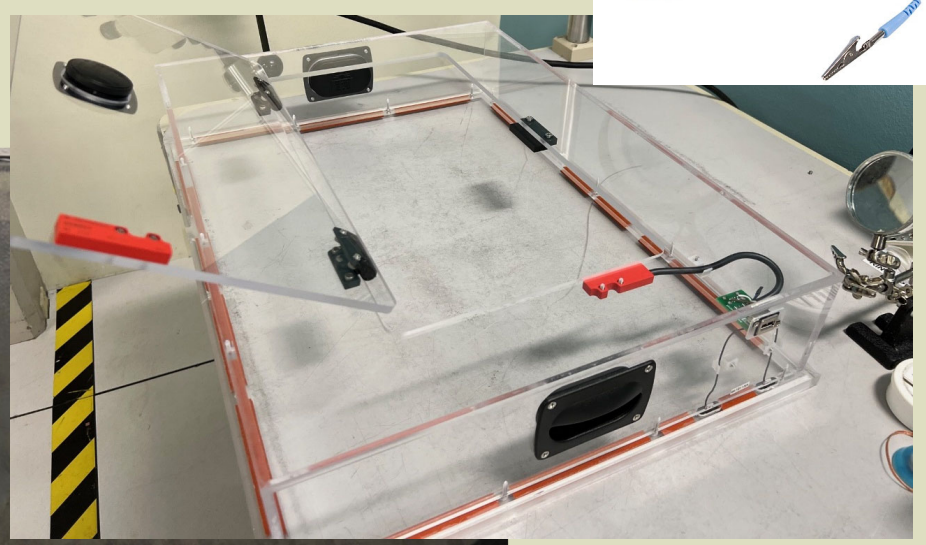
Power Sequencing

- Powering up the high voltage supplies after the digital and analog supplies reduces the load on the board
- Oven needs to have power sequencing capabilities
  - During a loss of power, board still needs to shut down in correct sequence
  - Failure to shut down correctly can cause a spike in current on a High Voltage supply
  - Could lead to damage of part, board, or oven itself

Power Supply Identity	Power Up Sequence	Power Down Sequence	Bias Voltage (V)	Sequence Current per Device (uA)	Run Current per Device (uA)
PSA	4	2	+100	500	500
PSB	5	1	-100	500	500
PSC	2	4	+1.9	9375	9375
PSD	1	5	-5	500	500
PSE	3	3	+5	3500	3500

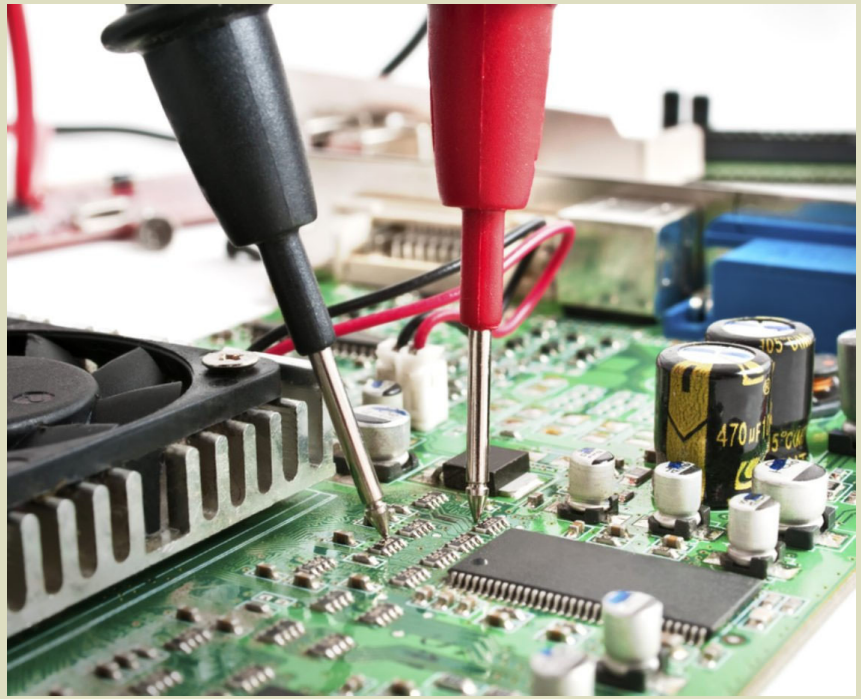
Electrical Safety

- Standard wrist straps are not safe for use in HV conditions
- High voltage covers can be used instead
  - During ATE testing, HV covers reduces efficiency
- Debugging is more challenging when HV covers are in use
  - More difficult to measure voltages, probe signals with an oscilloscope



Call to Action!

- Tighter quality control for boards and components
  - Test a sample of components from each batch
  - Power up the boards once fully assembled
- Prioritize reliability and quality of build over cost when choosing components
- Easier to access test points considering the space taken up by HV covers



COPYRIGHT NOTICE

The presentation(s) / poster(s) in this publication comprise the Proceedings of the TestConX 2024 workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the TestConX 2024 workshop. This version of the presentation or poster may differ from the version that was distributed at or prior to the TestConX 2024 workshop.

The inclusion of the presentations/posters in this publication does not constitute an endorsement by TestConX or the workshop's sponsors. There is NO copyright protection claimed on the presentation/poster content by TestConX. However, each presentation / poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

www.testconx.org