Monte Carlo “FEA” - fast solutions for fast interconnects

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Problem

- Optimization of PCB parameters for a given interconnect demands manipulation of several parameters to achieve the best results.
- Performance is often found to be optimal over a limited frequency range, i.e. what's best at lower frequencies doesn't necessarily yield a good high-end response. That means just requesting optimization in the high frequency range will not give us a good idea what is possible at lower frequencies.
- This leads to a need to run many time consuming full frequency range 3D FEA simulations although the basic problem is not overly complicated.

Simulation platforms

3D FEA

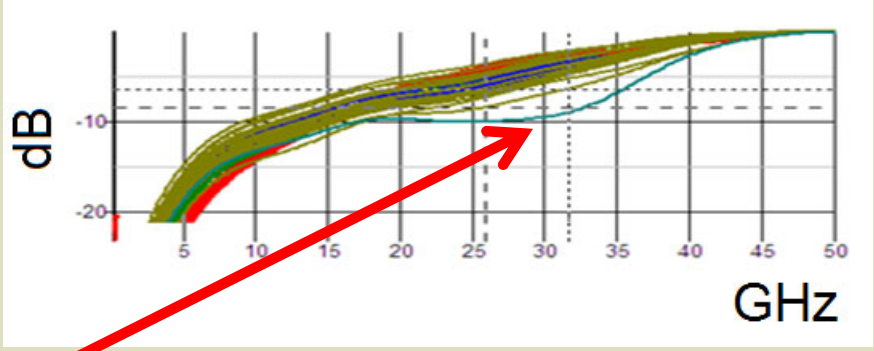
- Very competent solution
- Expensive
  - Initial acquisition
  - Annual maintenance
  - Optimization option
  - Hardware requirements
  - Operator qualifications
- Slow
  - CPU/RAM
  - Occasional non-convergence

SPICE circuit analysis

- Affordable
  - Acquisition
  - Basic EE understanding
  - Low/no maintenance
  - No special hardware necessary even for complex problems
- Fast
  - Low CPU requirements
  - Low RAM needs
- Cannot be directly applied to problem (or can it ?)

The FEA 'speed conundrum'

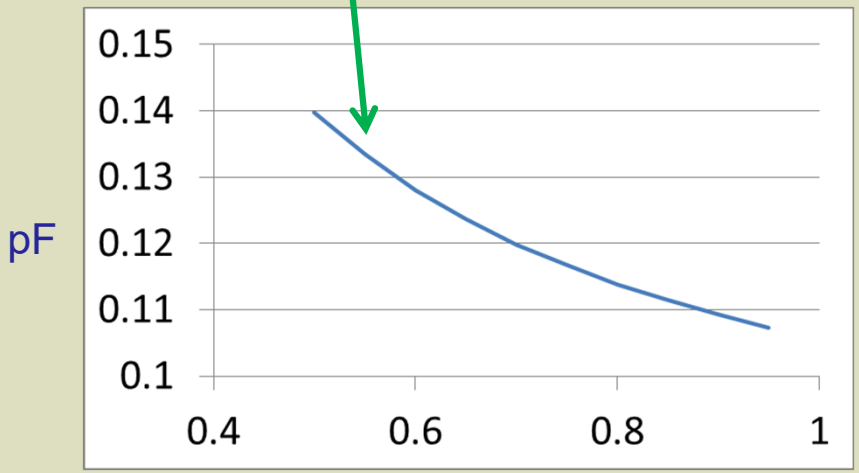
- Typical 3D FEA software is too slow to allow for generation of a large number of solutions to assess which parameter set leads to the most favorable outcome:



- Here, only **one of 100** different parameter combinations gives the best solution. With 3D FEA it might be *many days* before all permutations are run.

‘Repetitive’ 3D FEA

- Basic problem is relatively simple, yet we must compute a full 3D FEA run for each individual curve/solution over and over again.

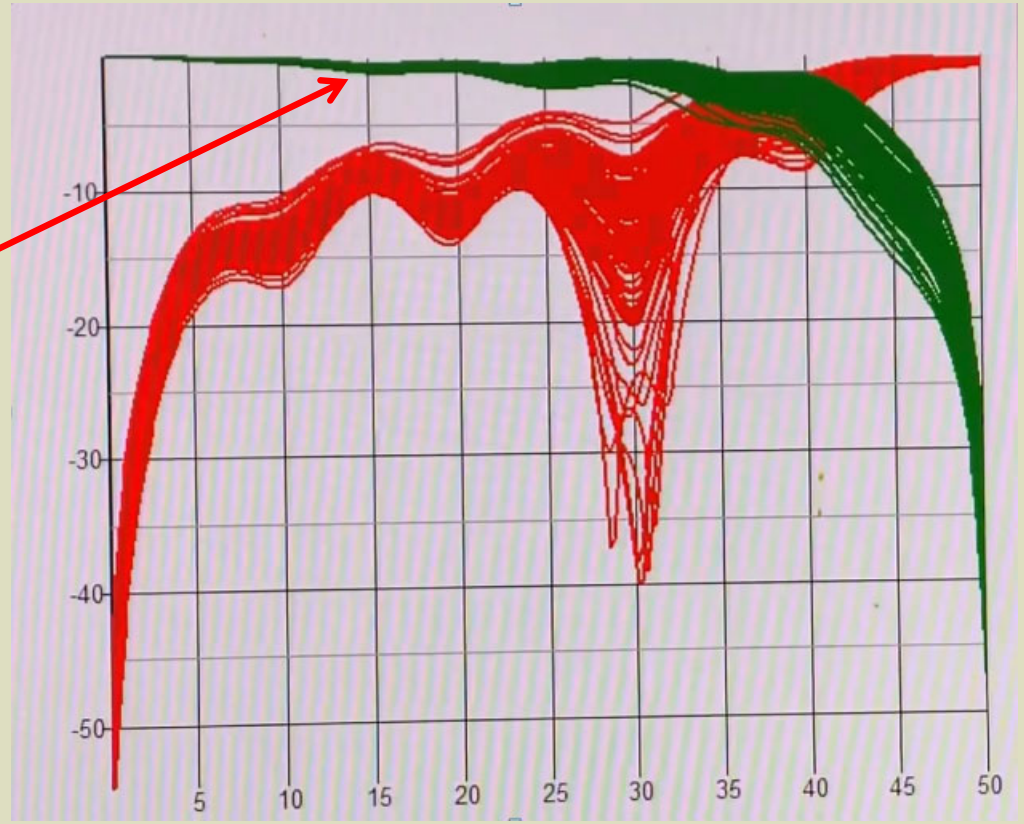


Example: Capacitance as a function of antipad diameter for a single pad/antipad combo (select dielectric constant)

It seems as though it should be possible to operate from ‘lookup tables’ instead.

Lookup table reward: Speed of solution output

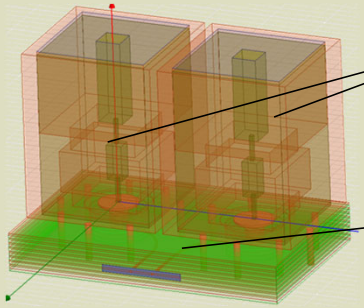
Note the run number advancing rapidly to a total of 100 simulation cycles in 3 seconds



This SPICE simulation is for a non-optimal configuration and is only meant to demonstrate range and speed of solutions.

Potential solution: SPICE simulation

- Establish a SPICE equivalent circuit for the chosen architecture.



Coaxial cable* to PCB connector

PCB with ***stripline**** on inner layers

- Identify parameters of interest, e.g. various L,C components.
- Define possible range of these parameters.
- Establish SPICE equivalent circuit for chosen architecture.
- ***Run Monte Carlo*** analysis and inspect results.

****analytical solutions are available, no 3D FEA required***

Monte Carlo Methods

From Wikipedia (partial excerpts, in black):

- Monte Carlo methods…are a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results…are useful for simulating systems with many coupled degrees of freedom…
- …the computational cost associated with a Monte Carlo simulation can be staggeringly high. In general the method requires many samples to get a good approximation, which may incur an arbitrarily large total runtime if the processing time of a single sample is high.
  - *Thus, performing exhaustive Monte Carlo analysis inside a finite element computation environment for 3D field analysis incurs large time and computation resources penalties.*
  - *The use of traditional SPICE simulators, however, allows generation of solution sets literally within seconds.*

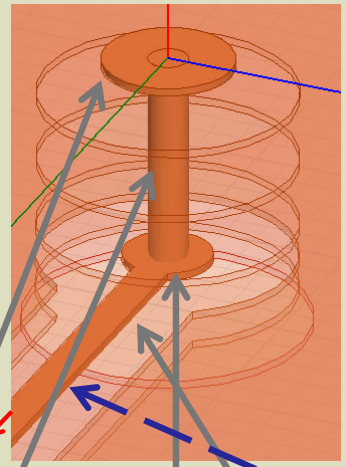
Methodology

- Establish equivalent circuit for chosen architecture
  - Please also see “Into the PCB at 90–high GHz signal launches, 2022 TestConX”
- Identify all parameters that are free to vary
- Determine upper and lower limits for these parameters
  - This requires either a priori simulations or a broad database
- Enter into SPICE simulation setup
- Run multiple Monte Carlo analyses
- Identify most desirable individual run and extract parameter set
- Refer to prior simulations or database to convert SPICE results to physical parameters, run 3D FEA on solution

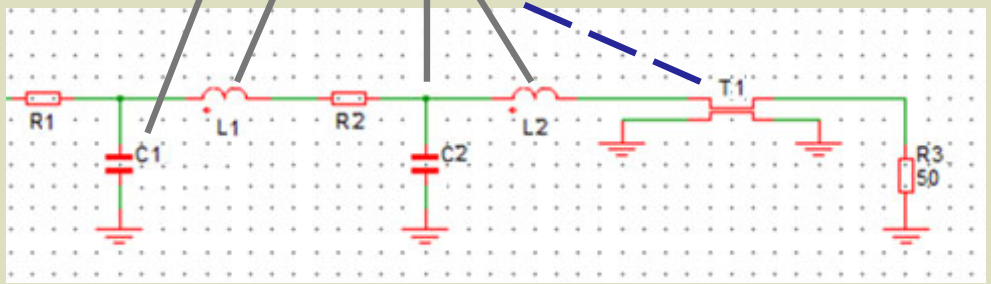
Simplified PCB only equivalent circuit

Physical circuit:

The internal structure representation shown here is simplified. In reality it possible that multiple transmission line sections or multiple L/C components instead of one single transmission line must be used.



SPICE circuit:



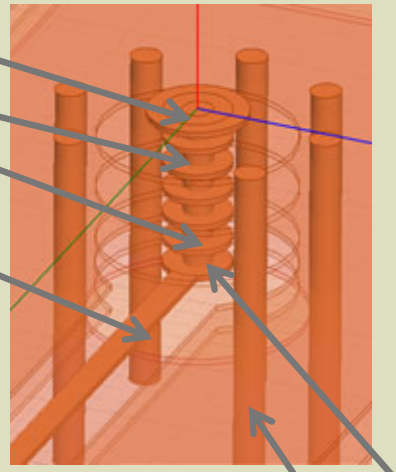
PCB with microvias

Contact pad (C to ground)

Microvia capture pad (C to ground)

Signal layer capture pad (C to ground)

Signal layer trace (transmission line)



C => capacitance
(typically to ground except for additional terms in case of coupled line/via sections for example in differential designs
L => inductance

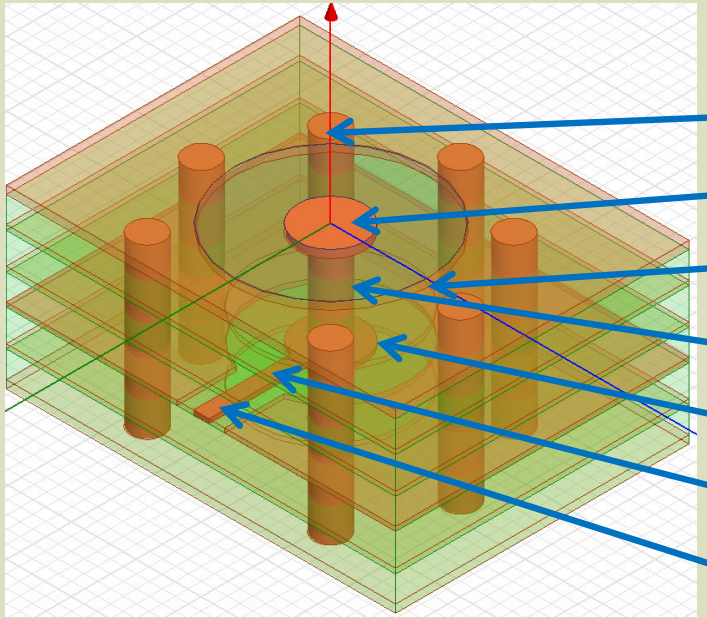
The complex internal structure requires representation either by multiple transmission line sections or multiple L/C components instead of one single transmission line

Signal via (L in series)

Ground vias (L in series between planes)

PCB only design limits

- PCB Parameters that can be adjusted



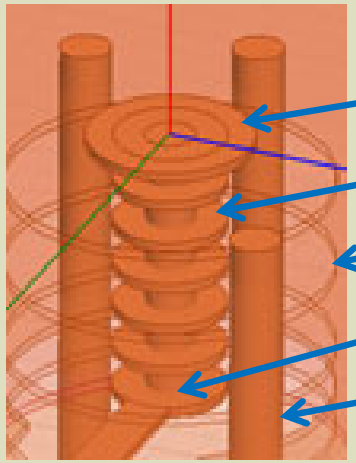
» Ground bolt circle
» Contact pad
» Antipads
» Signal via
» Capture pad(s)
» Feed section
» Incoming trace width

Adjustment range:

- Pad, Via and Bolt circle diameters
  (all have lower limits set by PCB manufacturing capabilities)
- Trace width
  of incoming line
  (typically set to required characteristic impedance)
  of pad feed section
  (if present, not shown here)

SPICE parameter extraction from 3D FEA models

- Stacked vias and their capture pads



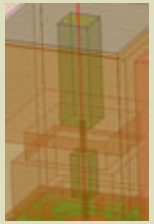
» Contact pad
» Capture pads
» Antipads
» Signal via
» Ground vias

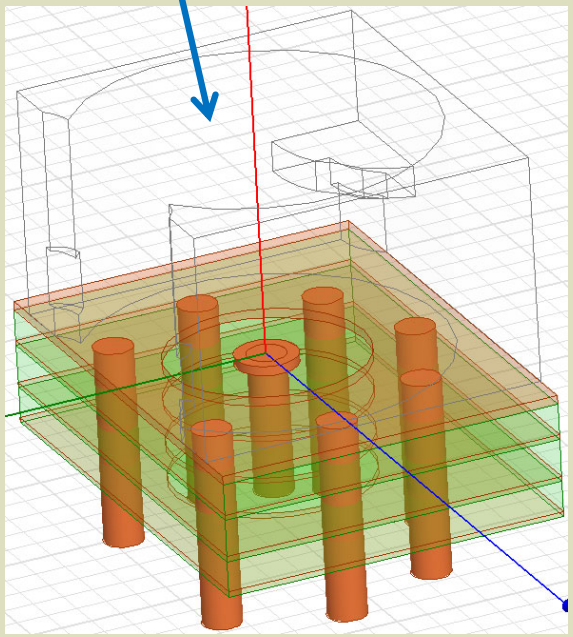
To be extracted:
- Pad capacitance
- Via inductance

It has thus far been difficult to compose this from individual L/C/Tmline sections because of parasitic contributions from pad to pad.
Thus it appears best to model this as one piece.

SPICE parameter extraction from 3D FEA models

- **Coax connector =>**





» Extraction of SPICE parameters will require 3D model from manufacturer

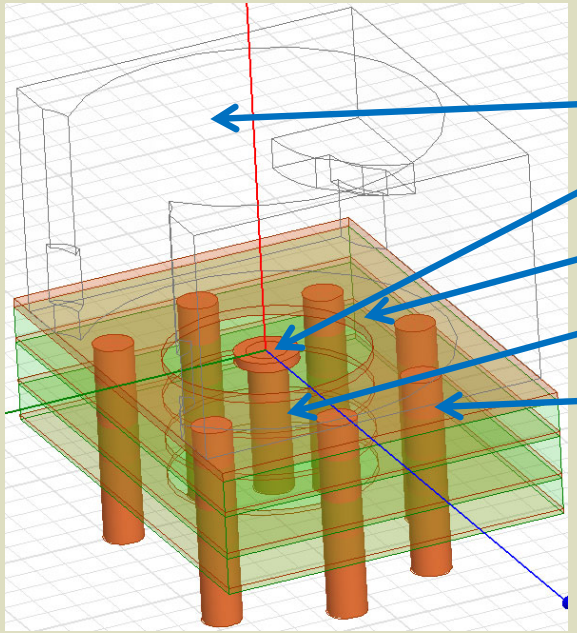
To be extracted:

- Line impedances
- Connector inductance
- Connector capacitance

Alternately it may be possible to establish a connector equivalent circuit from time domain reflectometer (TDR) measurements

SPICE parameter extraction from 3D FEA models

- **Connector to PCB interface**



» Coax connector
» Contact pad
» Antipads
» Signal via
» Ground vias

To be extracted:
- Contact pad capacitance
- (Via inductance)

It is important to include parasitic contributions from surroundings.

Monte Carlo Demo Simulation Parameters

Vary dimensions:

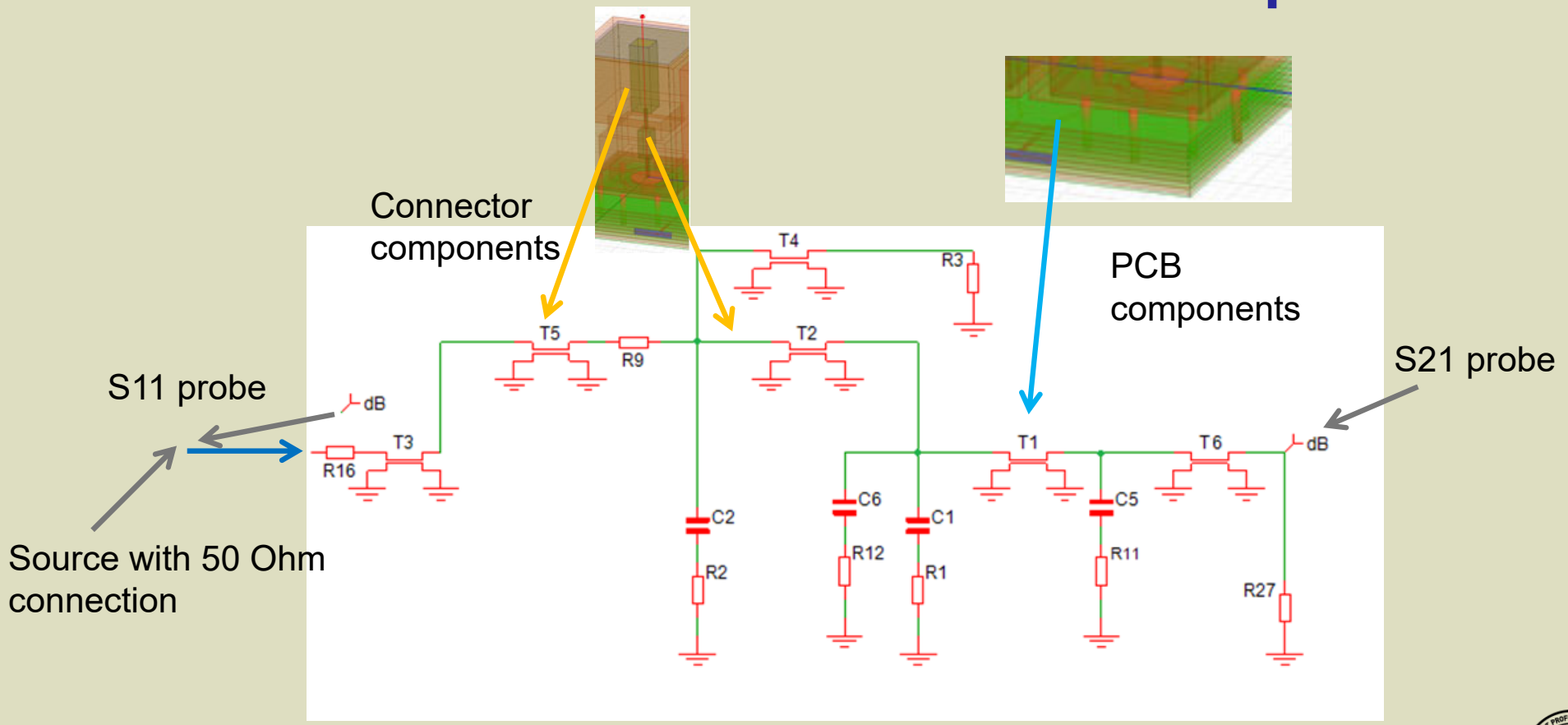
- Contact pad diameter*
- Capture pad diameter*
- Signal via diameter**
- Antipad diameters*
- Ground via bolt circle diameter**

Note:
All presented solutions are case specific. While trends can be established, it is not possible to generalize answers.

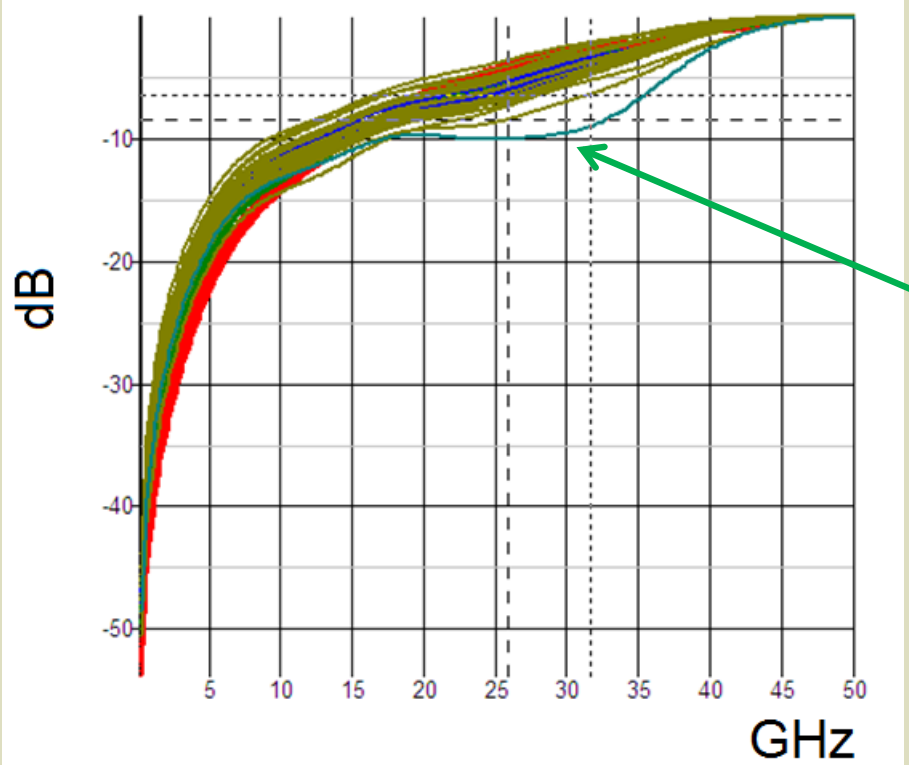
* Pad diameters and antipad dimensions together affect capacitance to ground

** typically set before commencing optimization, adjusted only if no satisfactory results are available at all.

Demo SPICE circuit for an interconnect plus PCB



Return loss S11



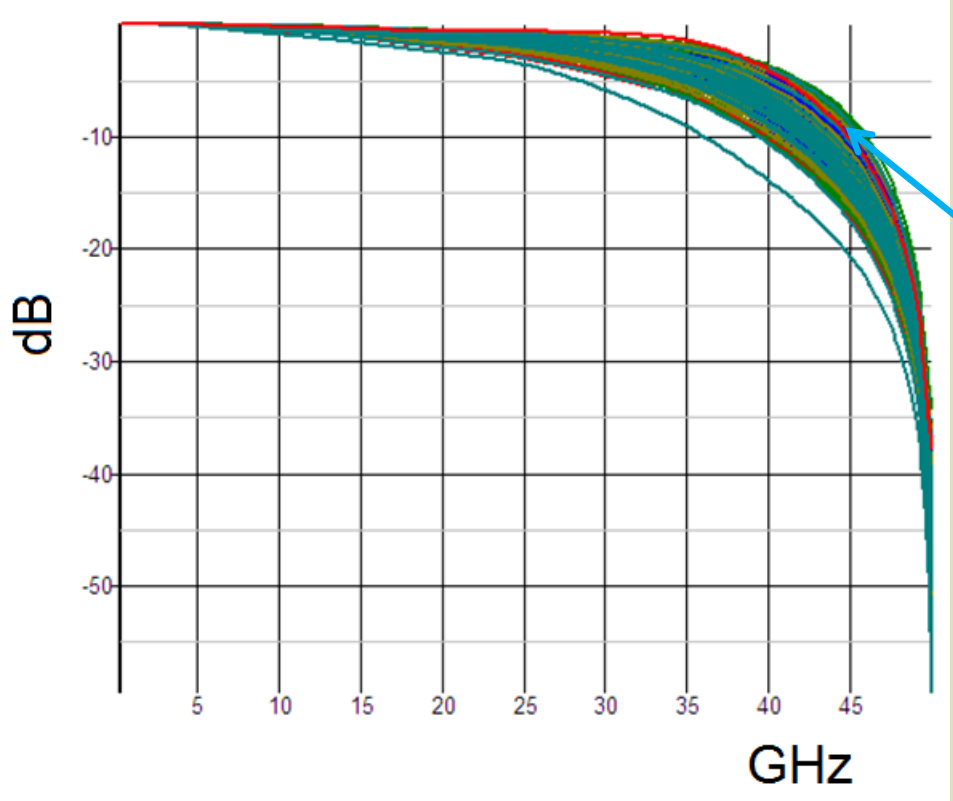
MC:

Run multiple times until best or near best performance is obtained

- Here only one mix of parameters gives best performance at high frequencies

(the interconnect model was not selected to demonstrate optimal overall performance but the power of the Monte Carlo approach)

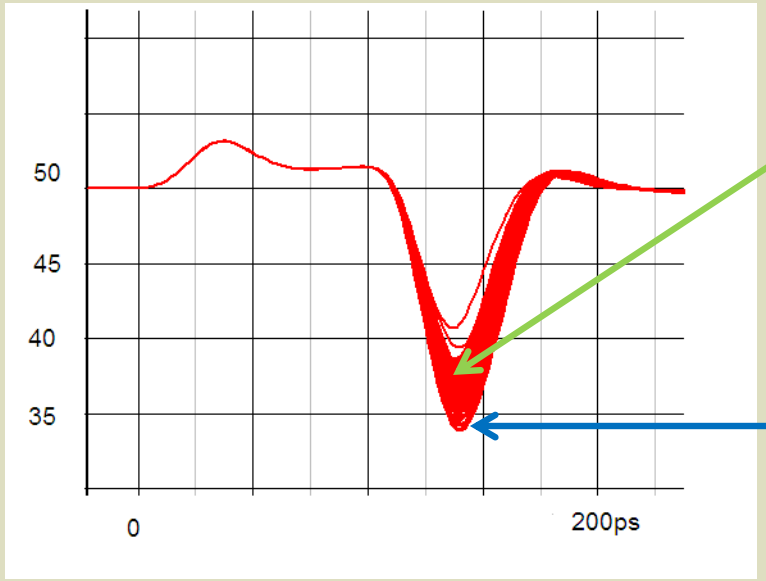
Insertion loss S21



Corresponding S21 set to the S11 solution set above

Red curve shows good, but not best performance at high frequencies for the parameter set selected above

Time Domain Reflectometry



Corresponding time domain reflection measurement set to the S11 solution set

- TDR results are not very useful for selecting the optimal solution

(the best high frequency performance curve lies somewhere within this group of solutions)

- The impedance dip down to 35 Ohms explains the relatively poor performance of this interconnect

(the model was not selected to demonstrate optimal performance but the power of the Monte Carlo approach)

Comments

- 3D FEA models for individual circuit elements must be carefully set up in order to arrive at accurate circuit element representations.
- It is essential to include parasitic contributions from components and feed structures during evaluation.
- Correlation between SPICE and 3D FEA models has been demonstrated on a limited case basis to date.
- Failure to execute the 3D element models properly will lead to failure of the Monte Carlo method with SPICE.

Pros and Cons

- Pros
  - Very fast generation of very large solution numbers
  - A large number of variable parameters may be specified
  - Random parameter selections offers good chances that a ‘near best’ or the best solution will be present in the output dataset
- Cons
  - Setup requires a good understanding of how to generate a valid equivalent circuit
  - A large number of a priori 3D simulations may be required to develop a comprehensive database that allows for quick parameter range selection

Conclusions

- Optimization of PCB parameters is mandatory to achieve good performance at high frequencies.
- Monte Carlo methods aid in optimization scenarios with multiple “optimal” designs that may in conventional simulation approaches otherwise not be identified. This applies to SPICE simulations as well as potential 3D FEA solutions.
- Experience with proper parameter selection and knowledge of their possible ranges will allow for very fast ‘visual’ selection of optimal performance via Monte Carlo simulation results.

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