Effective back-drilling strategies for 200G+ PAM4 Designs

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- Scope and Objective of the Test
- Test Definition and Measurement Setup
- Simulation Results and Measurement Correlation
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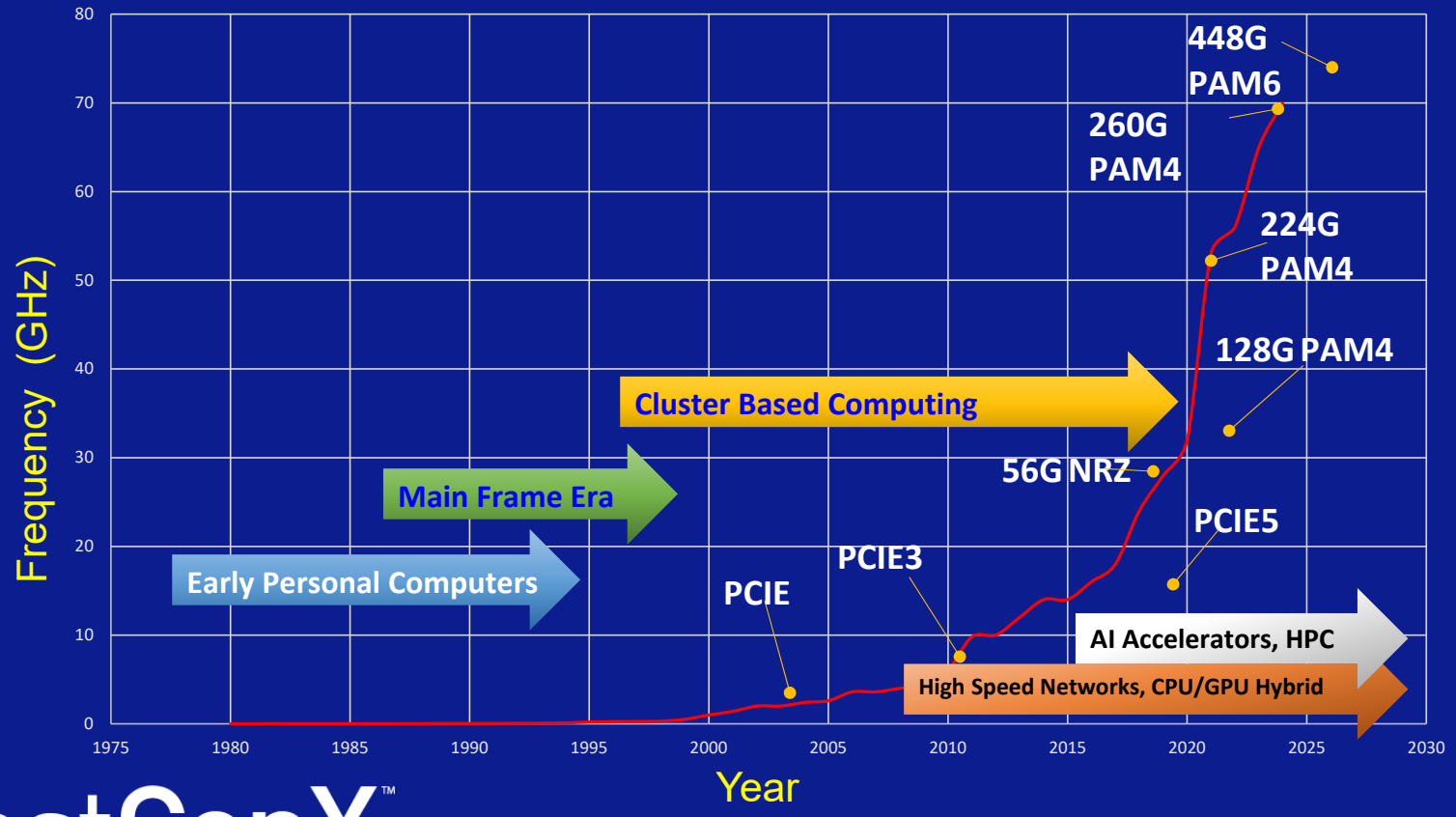
The Era of High-Performance Compute



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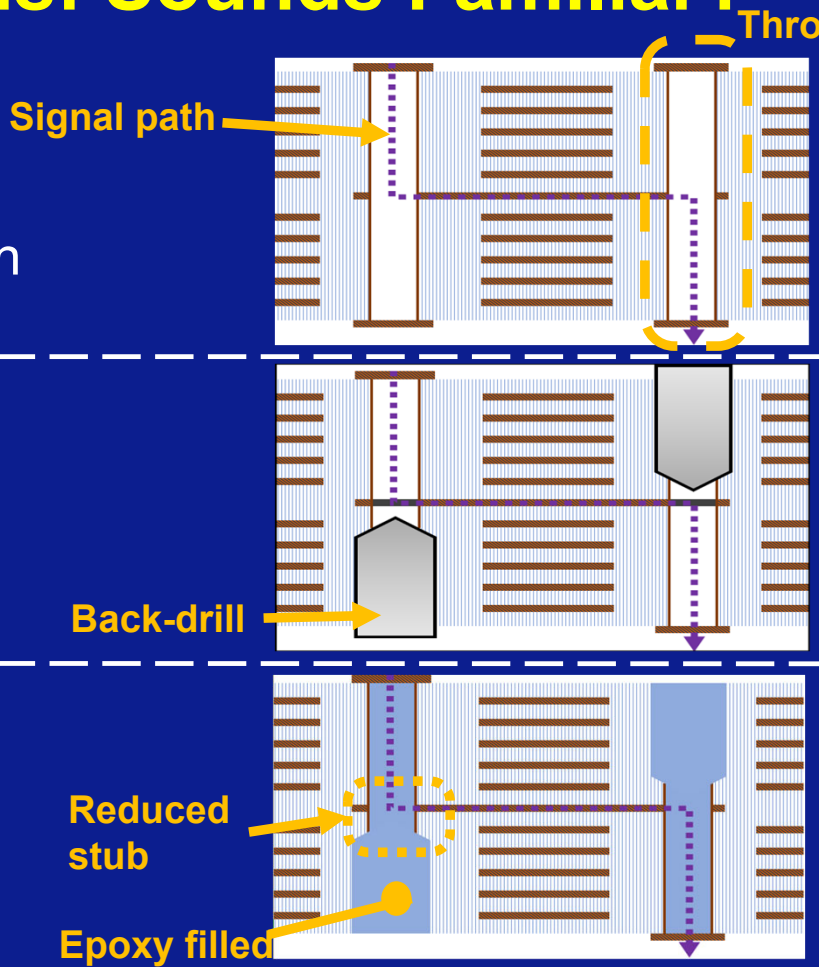
Back-Drill in HS Designs: Sounds Familiar?

- Signal path has stubs → Causes reflections due to impedance mismatch

- Vias are back-drilled → reduced stub

- Backdrill hole can be filled with non-conductive epoxy



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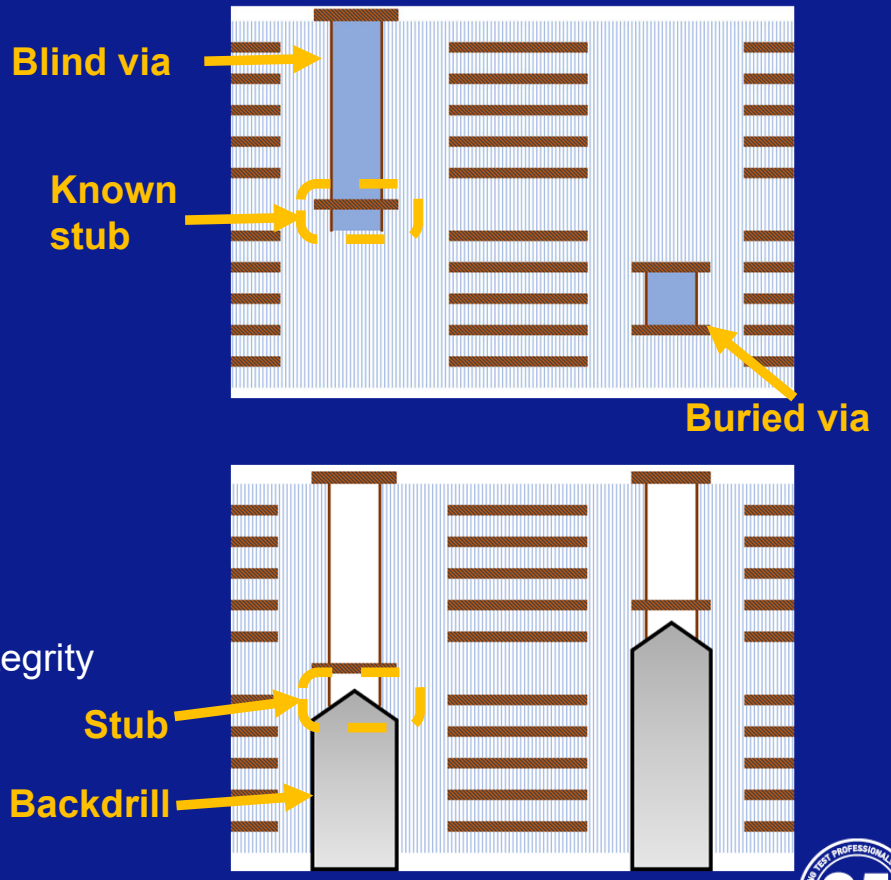
Traditional Via Strategies for HS Lines

Blind/Buried vias

- Pros:
  - Known minimum stub
  - Reduces via density for better power delivery
- Cons:
  - longer lead times
  - high cost
  - Not suitable for high channel count

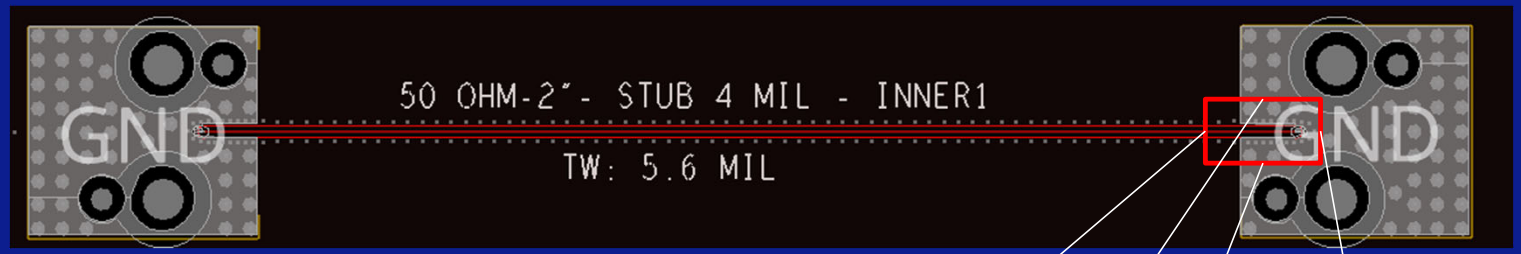
Through-vias with back-drills

- Pros:
  - Shorter lead times
  - Good cost-effective solution to support signal integrity
  - Can be used in conjunction with blind vias
- Cons:
  - Stub variation impacts signal integrity



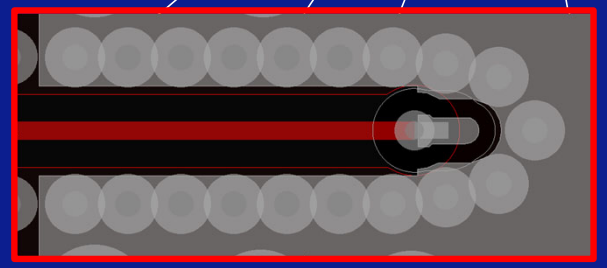
Test Vehicle Design

Measurement Structures



– 3 structures per routing layer
  - 12 mils stub
  - 8 mils stub
  - 4 mils stub

– Repeatability: Tested 2x boards



Engineering Evaluation for Stub Analysis

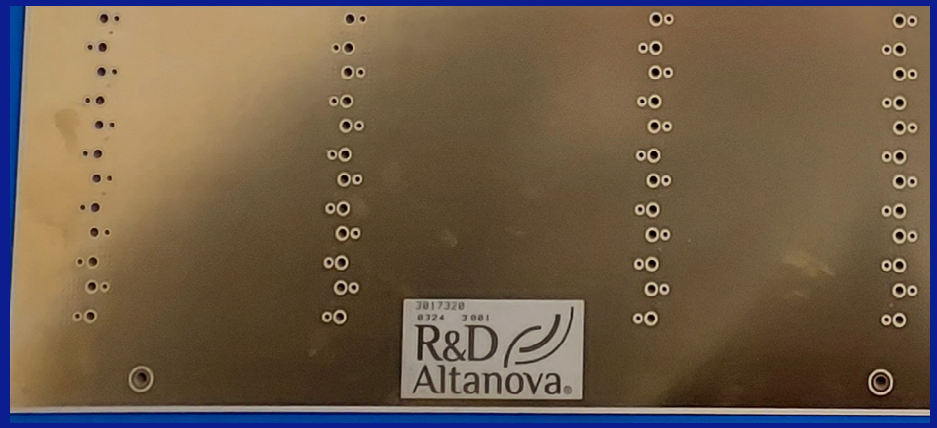
Qs: What stub length is acceptable for my design?

- Test Vehicle Design Considerations:
  - Board Material : Meteorwave4000
  - Trace Impedance: +/- 5%
  - Stack-up:
  - Board thickness: 188mils [4.77 mm]
    - 32 Layers
    - VLP Copper [Ra 4.5 microns]
  - Other Consideration:
    - Strip-line features: 2” long x 0.0056” wide
    - Design constraint: Compression mount connectors, 50 Ohms transmission lines and vias

Validation Setup

Setup

- Anritsu 70GHz Vector Network Analyzer [VNA]
- Calibrated up to 1.85mm VNA cables
- Connector P/N: 08K80F-40ML5 [1.85mm]
- Test Vehicle Board



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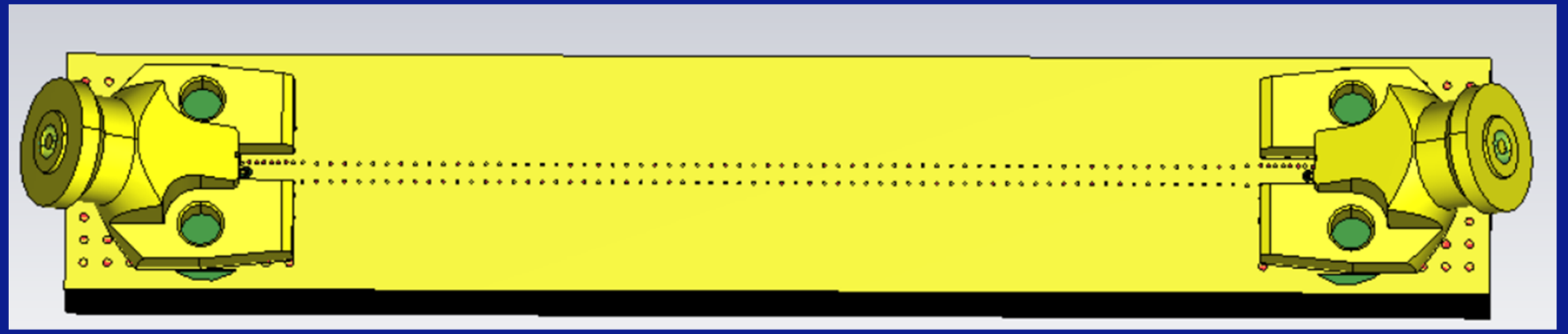
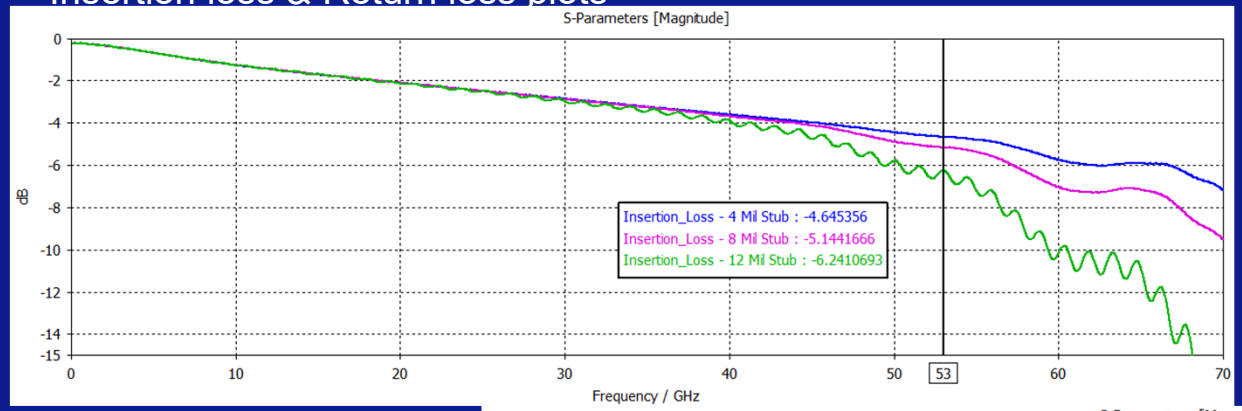
Modeling Setup

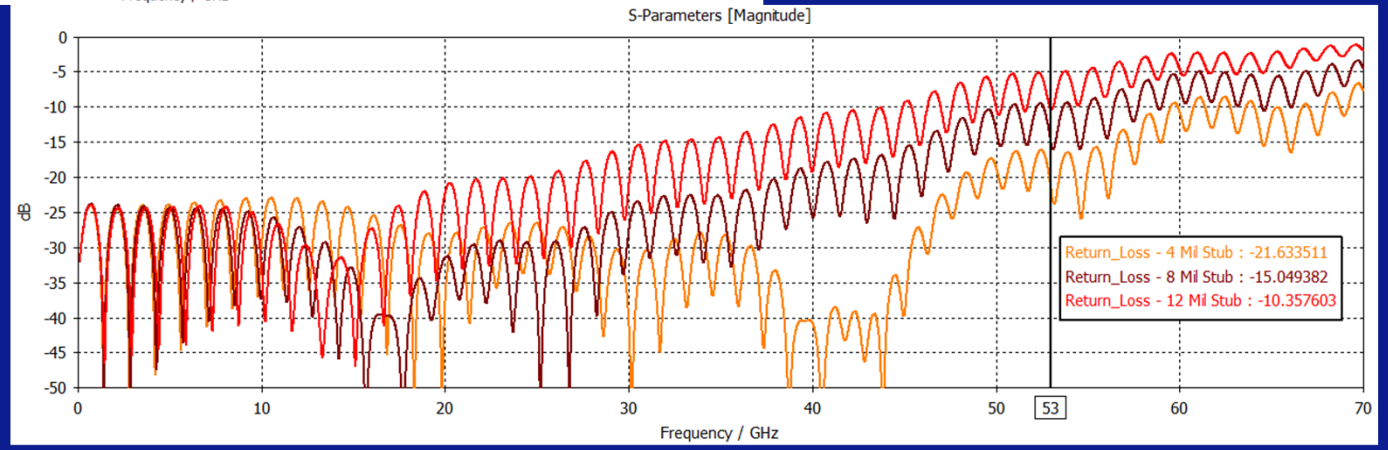
- Modeled with a Full 3D solver [Microwave Studios]
- 4, 8 and 12 mils stub up to 70GHz sweep
- Invisible Vias!
- Copper roughness accounted



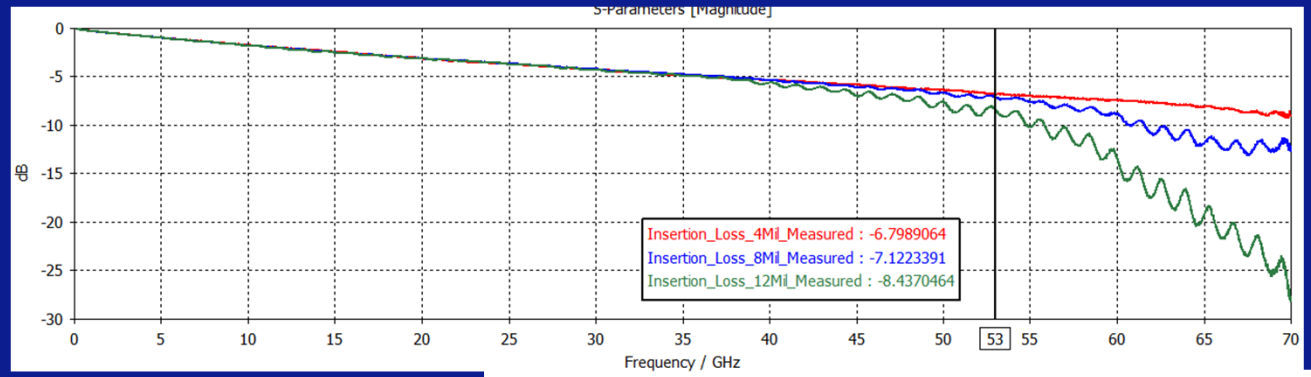
Simulation Results

Insertion loss & Return loss plots

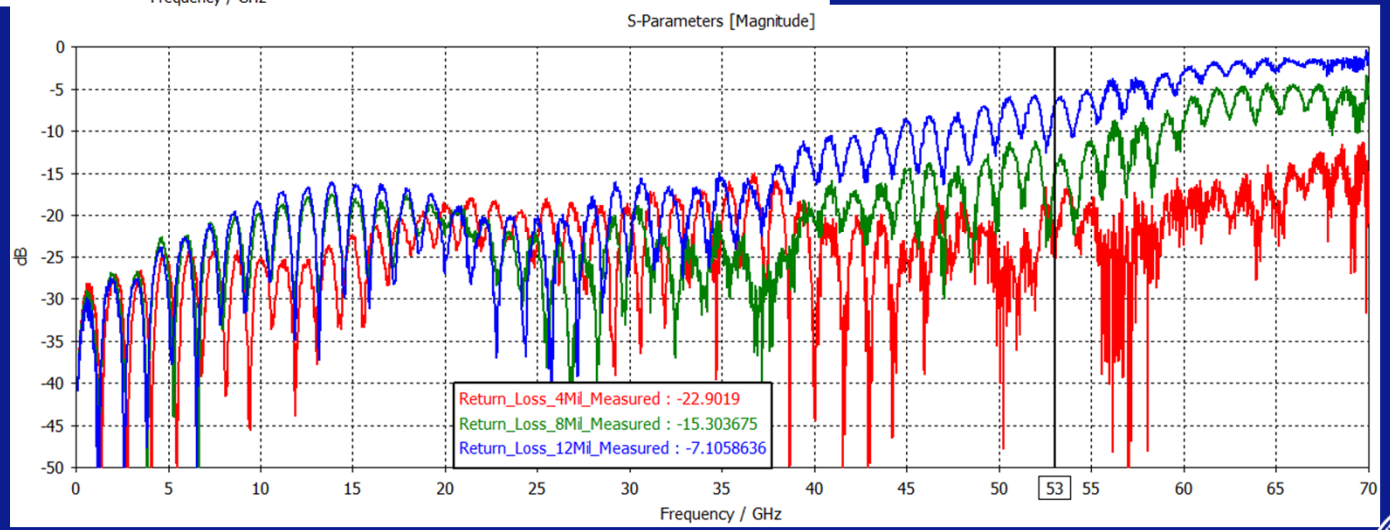




Measurements



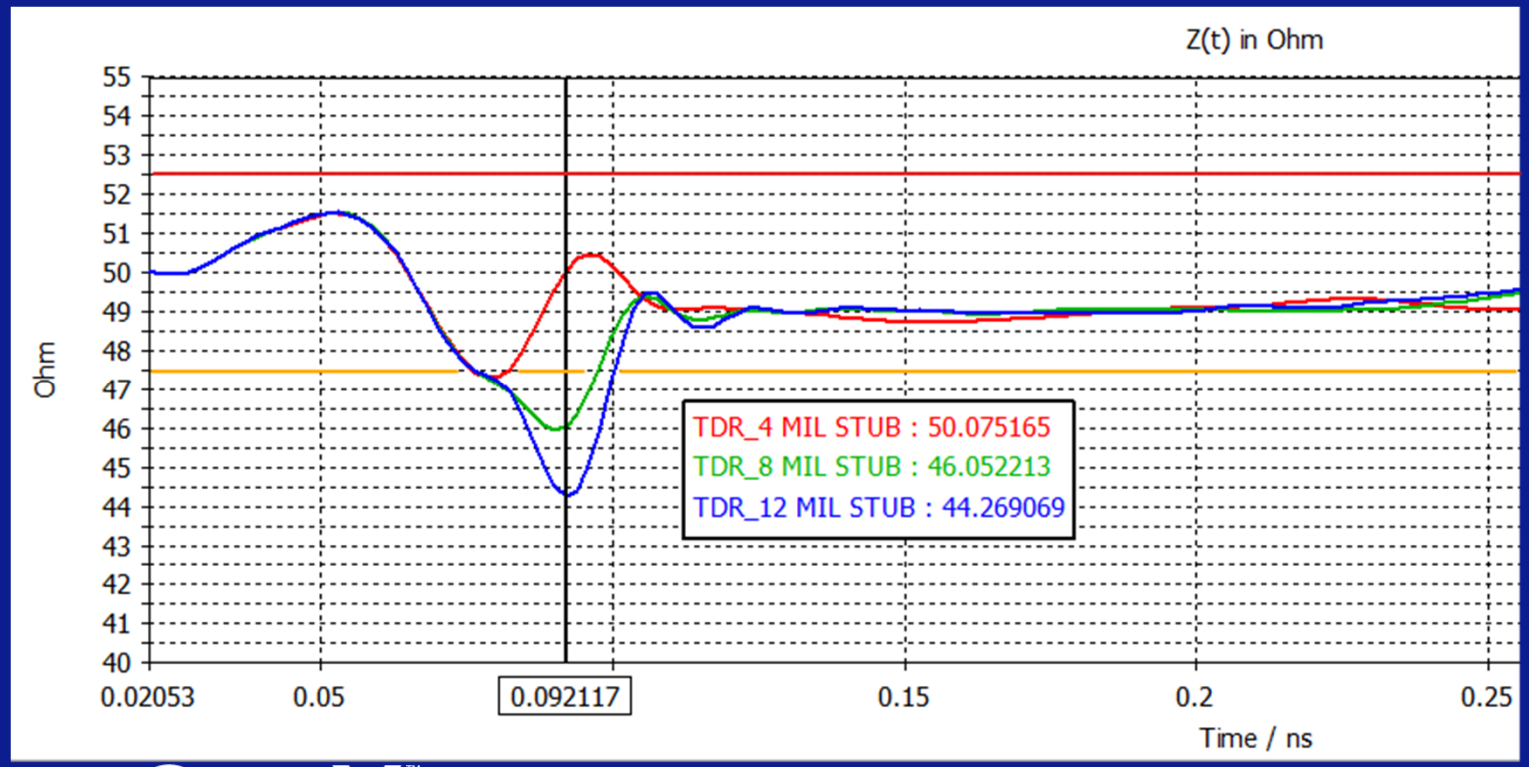
Insertion & Return Loss



Measurements

TDR

Clear Impedance variation is observed when looking at the TDR



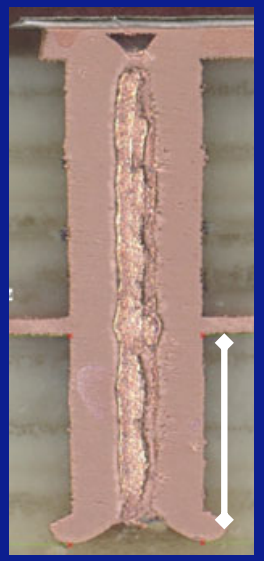
Back-Drill Validation

- Boards were cross-sectioned to validate stub length. Measured structures are within manufacturing limits:

4-mil stub

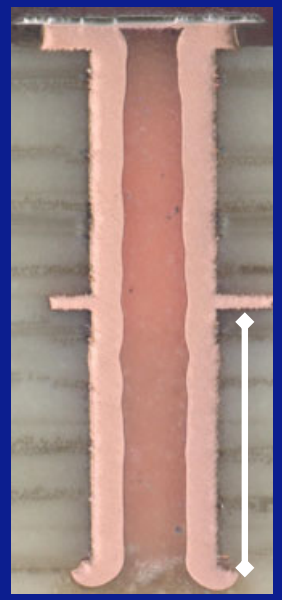
4.56mils

8-mil stub



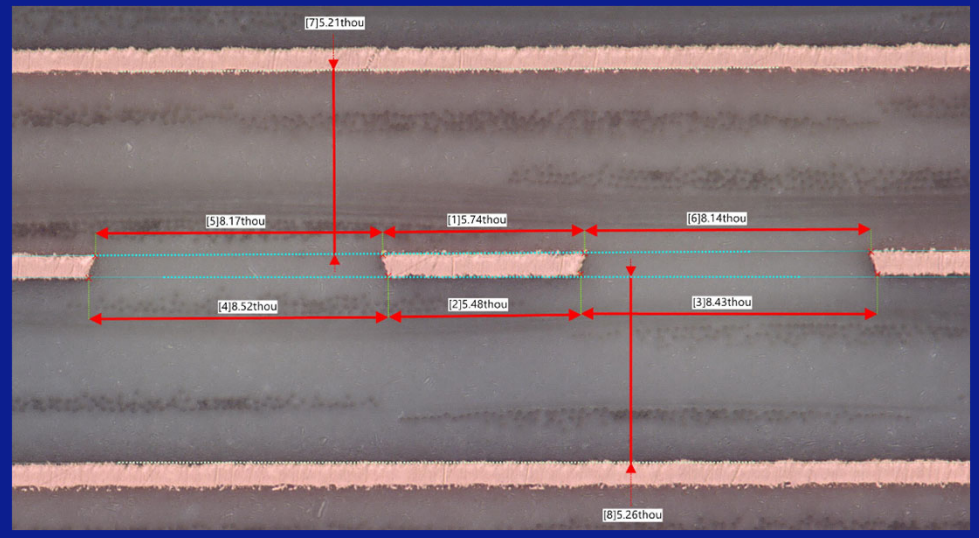
8.36mils

12-mil stub



12.35mils

Trace Cross-Section



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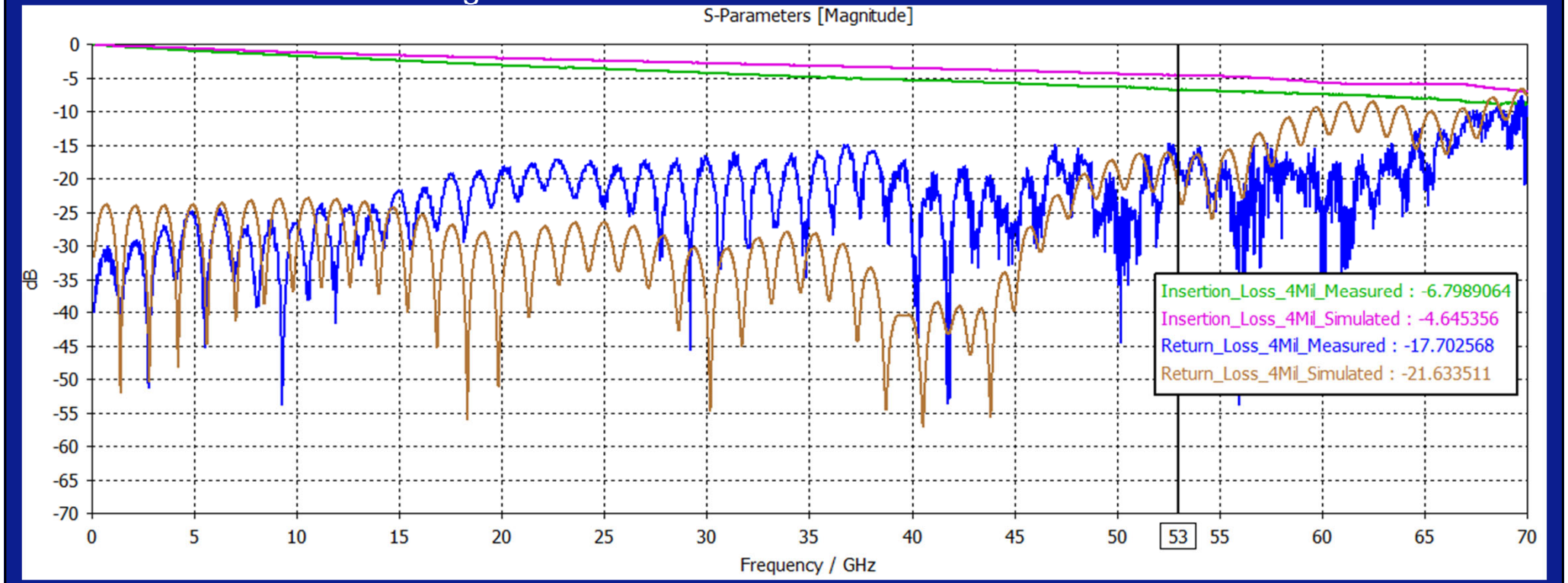
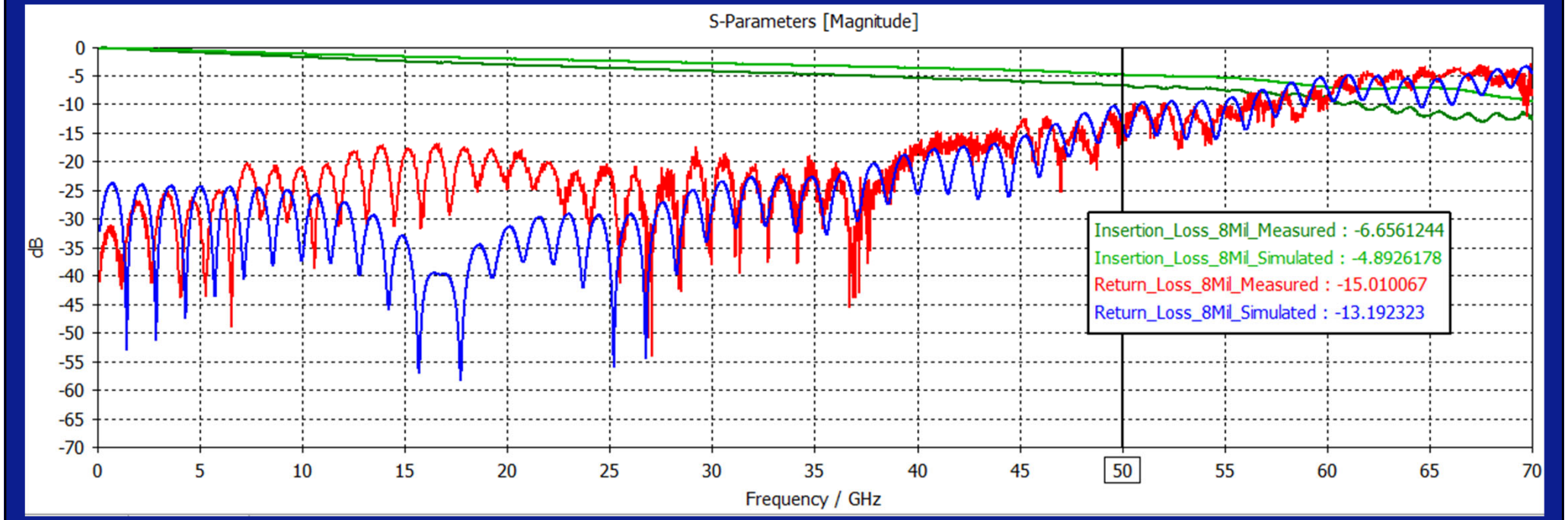
Measurement Correlation [4 Mil Stub]

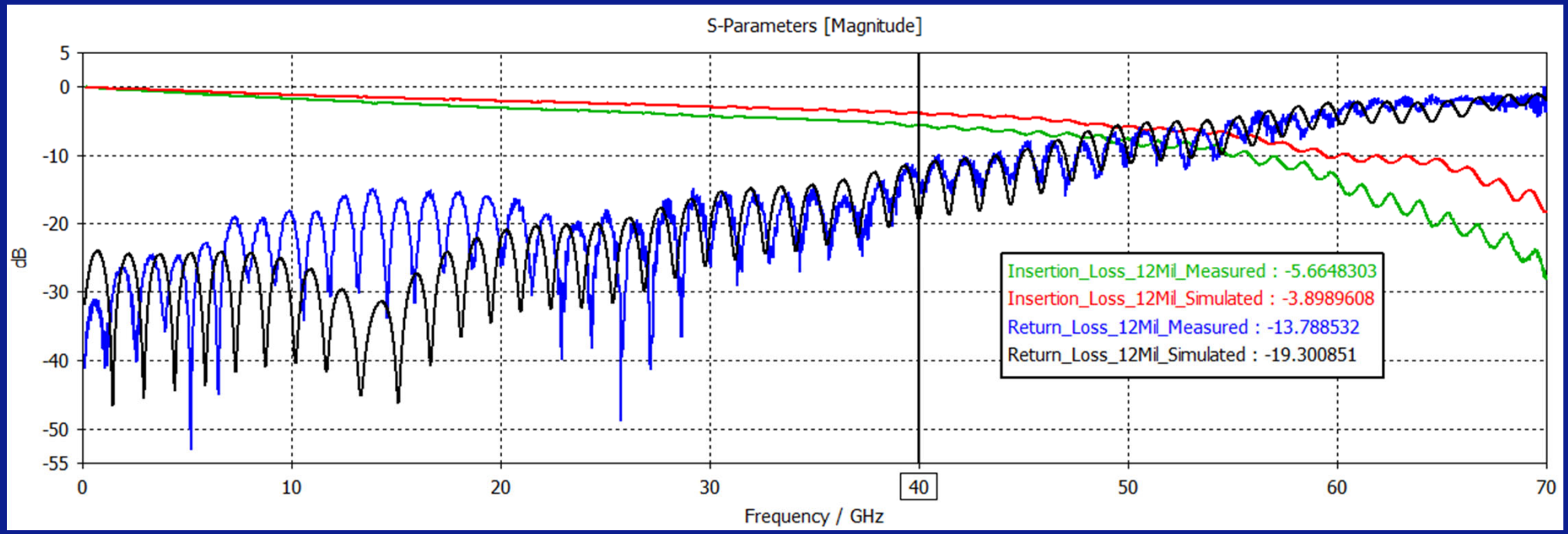
- Measurements shows good correlation with simulated data



Measurement Correlation [8 Mil Stub]

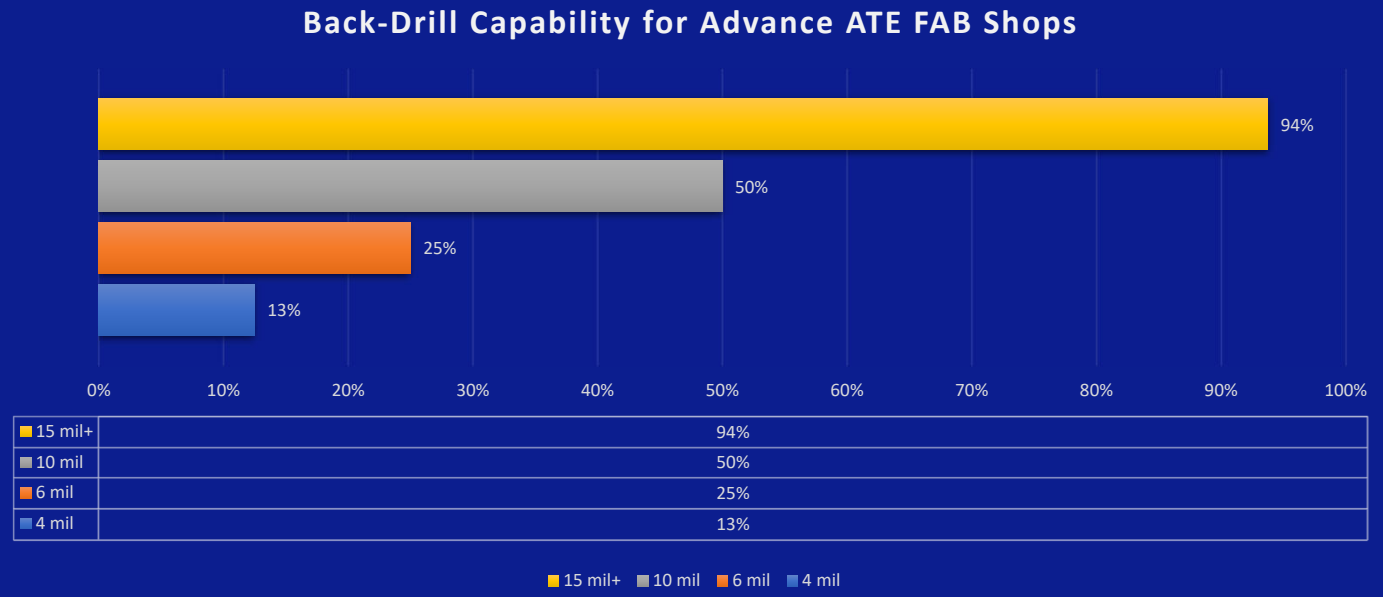


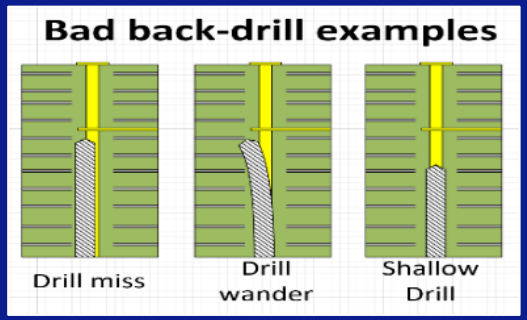
Measurement Correlation [12 Mil Stub]



Capability Matrix for Advance Back-Drilling

- Estimated market breakdown for Advance ATE FAB back-drilling capability





- 4 mil back-drills is critical for 200G+ PAM4 speeds
- Make sure your board vendor has 4 mil back-drill technology

Summary and Results

- Back-drills; unlike growing perception is still highly effecting technique for stub removal
- With proper back-drill stub control, 70+ GHz performance can be achieved on PCBs
- With manufacturing tolerances accounted, conservatively; 12 mil or better Back-drills can be used for up to 35 GHz design and 8 mils or better up to 50GHz. For 50GHz+_Design a premium back-drill under 6 mil is advised.
- Make sure to account for PCB manufacturing tolerances when selecting back-drills. Manufacturing tolerance can account for +/-5% to +/-10%
- Other critical parameters as material selection, impedance control, via optimization, etch control, plating features etc. are equally important considerations

Speed/Modulation	Nyquist	PCB Material	Stub (Simulations)	PCB Impedance Tolerance [Max]
28Gbps NRZ / PAM2	14GHz	METWAVE2K	12 mil	+/-10%
56Gbps PAM4		METWAVE2K	12 mil	+/-10%
PCIE Gen5	16GHz	METWAVE2K	12 mil	+/-10%
56Gbps NRZ / PAM2	28GHz	METWAVE4K	10 mil	+/-5%
112Gb PAM4		METWAVE4K	10 mil	+/-5%
212G PAM4	53GHz	MW4K / MW8K/TACHYON 100G	6 mil	+/-5%
224G PAM4	56GHz	MW4K / MW8K/TACHYON 100G	6 mil	+/-5%
260G PAM4	65GHz	METWAVE8K/TACHYON 100G	4 mil	+/-5%
280G PAM4	70GHz	METWAVE8K/TACHYON 100G	4 mil	+/-5%

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Honorable Mentions

RDA performance validation team:

- Henry Lai
- Jacob Neely

& RDA Front End Engineering:

- Pravin Alurkar
- Syed Raza Ali Rizvi
- Irfan Khalid

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