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Virtual Event

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High resolution SAR ADC testing on ETS364

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SAR ADC introduction

Successive approximation register(SAR) ADC

➢ Consist of a sample-hold circuit, a comparator, a DAC, SAR register, and a logic control unit. Sample-hold circuit and DAC are integrated in the capacitance matrix. The capacitance matrix named sample and hold capacitor (Csh)

➢ A typical SAR conversion cycle has two phases, a sampling phase (acquisition phase) and a conversion phase.

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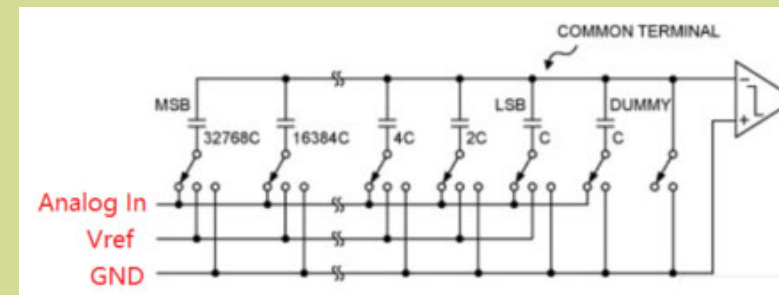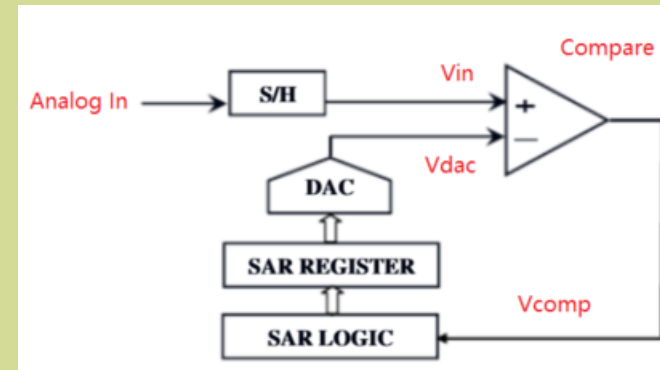
High resolution SAR ADC feature

➢ **SAR ADC resolution and throughput**

      8bit~24bit, 1MSPS~20MSPS

➢ **SAR ADC AC performance**

      SNR, THD,SINAD

➢ **SAR ADC DC performance**

      INL, DNL, Gain error

➢ **SAR ADC input type**

      Single ended inputs, pseudo differential inputs and differential input

➢ **SAR ADC application**

      Battery-operated systems, remote data acquisition and industrial controls

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Typical SAR ADC tests

Two important tests for ADC test

➢ **Dynamic test:** calculate SNR, SINAD, THD, Harmonic

➢ **Linearity test:** calculate DNL, INL, Gain error

 • **Histogram method**

Input a voltage ramp, capture output code and count the number of each code in histogram to calculate DNL/INL

 • **Servo loop method**

Select some codes to test, use servo loop to find input voltage on code's left edge or on code's right edge. INL/DNL is calculated by input voltage.

The difference between the two methods is that the QPLU servo loop method is input voltage's statistics while the histogram method is output codes' statistics.

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SAR ADC filter design

➤ For optimum performance, SAR ADC require the correct frond-end RC filter
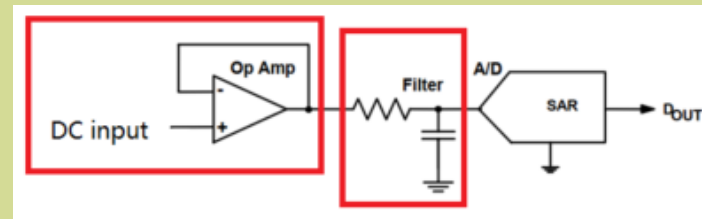
➤ A Multiple negative feedback bandpass filter is inserted to improve waveform performance before the input buffer for dynamic test

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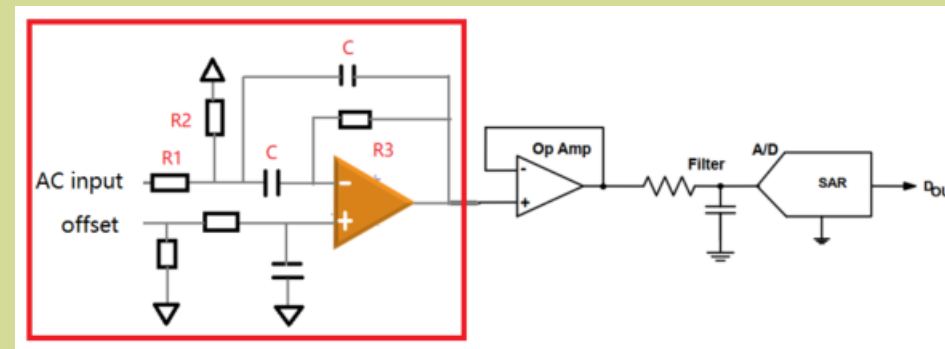
Front-end RC filter design

The front-end RC filter is to provide a path for charging and discharging, and to do some minimal isolation of op amp output to these transients.

➢ Cf serves two purposes, one is to store energy to charge ADC internal sampling capacitor (Csh), another is to provides a place for Csh to discharge. Cf's type is critical to the harmonic distortion and the value ensures ADC can have enough charge for each conversion.

➢ Rf ensures op amp output is stable.

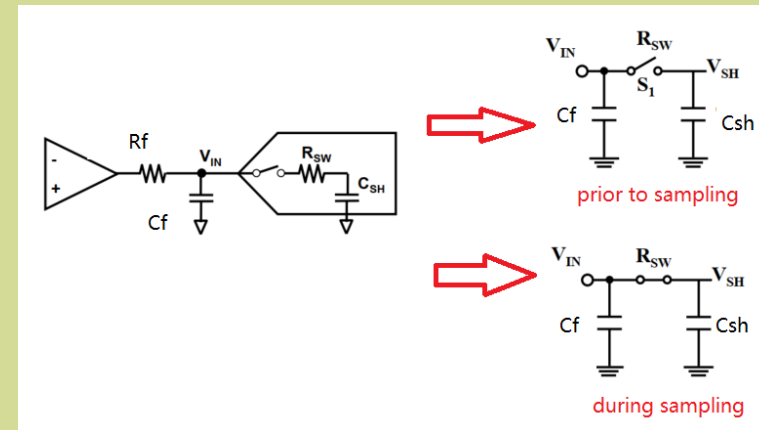High resolution SAR ADC testing on ETS364

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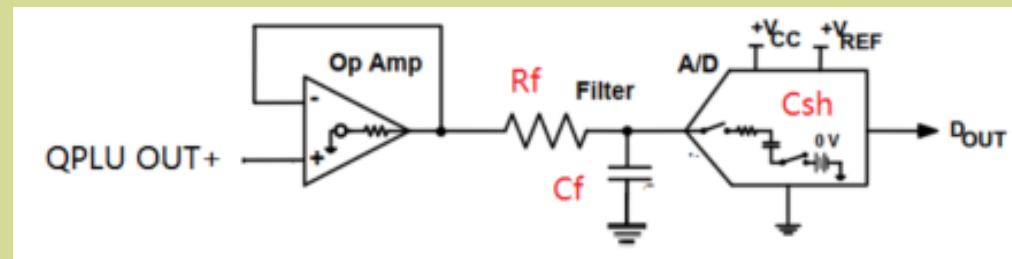
Define Cf

To define Cf's value, should know Csh and Vfsr, Vfsr is the full scale range of the converter. Cs=24pF, Vfsr=5V. For 16bit ADC, 1lsb=Vfs/2^16.

➤ Change transfer equation: Q=C*V

For Csh Worst case, Vsh=0V, Qsh=Csh*Vfsr

For Cf Worst case, droop 0.5 lsb on Cf, Qf=Cf*Vfsr/2^17

Qsh=Qf, Cf=Csh/2^17=3.15uF

The value is too large, Op Amp couldn't drive it.

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Define Cf

Then suppose, Cf has 5% droop of Vfsr because the amplifier provides some of the current to charge the Cf.

Qf=Cf*5%*Vfsr, Cf = Qf/(5%*Vfsr)=480pF, choose 470pF as a close.

**Conclusion:**

➢ As the rule of thumb, Cf ≥ 20*Csh

➢ To decrease the harmonic distortion, ceramic COG type capacitor is the best choice.

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Define Rf

To define Rf's value, should know Tsmpl, k(the time constant multiplier) and Cf

k is the number of time constants which required to settle to within a half LSB to a given number of bits. For 16-bit, k =12.

➢ Tsmpl≥ k*Rf*Cf, Tsmpl= 1.04us, Rf≤Tsmpl/(k*Cf)=184ohm

➢ Consider Op Amp output load and transient signal settling Time, Design in a margin of 40%.

0.60*Tsmpl≤ k*Rf*Cf, Rf≥0.60*Tsmpl/(k*Cf)=110.4ohm

➢ Finally choose Rf=110ohm

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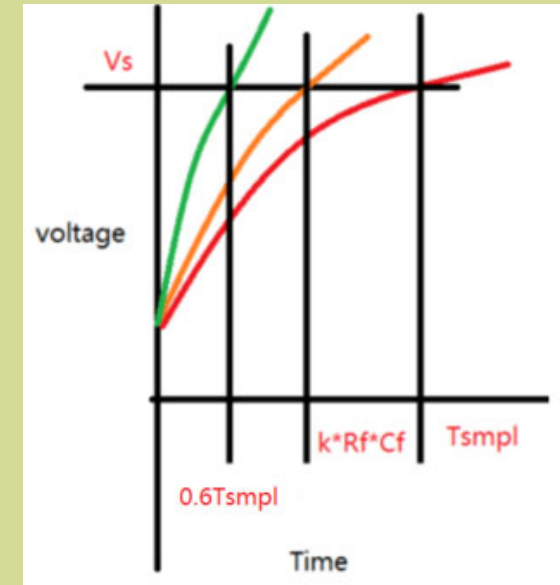
Multiple negative feedback bandpass filter design

The multiple negative feedback band pass filter's center frequency(f), voltage gain(A) and quality factor(Q) are determined by R1, R2, R3 and C.
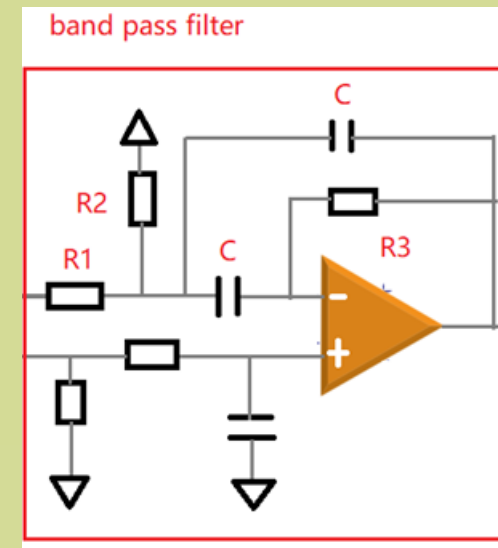
F = sqrt(1/(R3*C^2)*(R1+R2)/(R1*R2))/(2*π)
A = R3/2R1 = 0.3
Q = sqrt(R3(1/R1+1/R2))/2 = 3.28

R1 = 57.6kohm, R2 = 820ohm, R3 = 34.8kohm,
π =3.14,   C = 15nF
F = 2kHz, A = 0.3, Q = 3.28

band pass filter

By adjusting resistance value and capacitance value to obtain the wanted f, A and Q.

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Dynamic test condition

Input 2khz sinewave, offset and amplitude are 2.5V.

Here use SPU audio mode to force sinewave, apu12 force offset.

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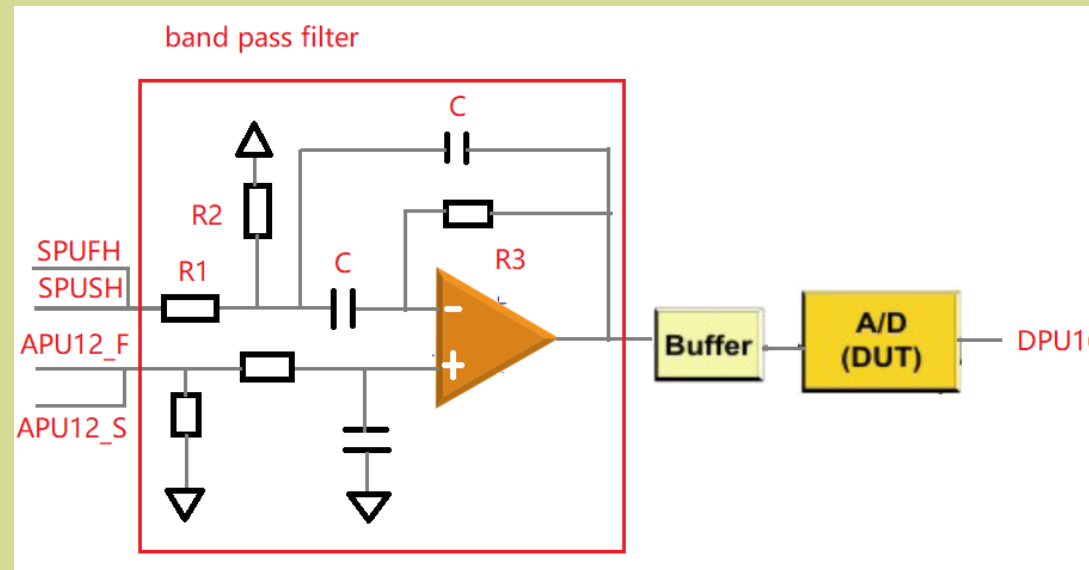
How to select analog components' type for band pass filter

Analog electronics are slightly nonlinear, which creates harmonic distortion.

➤ Resistors, thin film or metal resistors could be necessary in high performance signal chain

➤ Capacitors, Polystyrene and NPO/COG capacitors are good alternative to improve THD.

The right is frequency spectrum. Blue is the one with X7R capacitor, Green is the one using COG capacitor. The harmonics obviously decrease after COG capacitor is used, and SNR, SINAD and THD all increase about 40dB.

Frequency spectrum(dB)
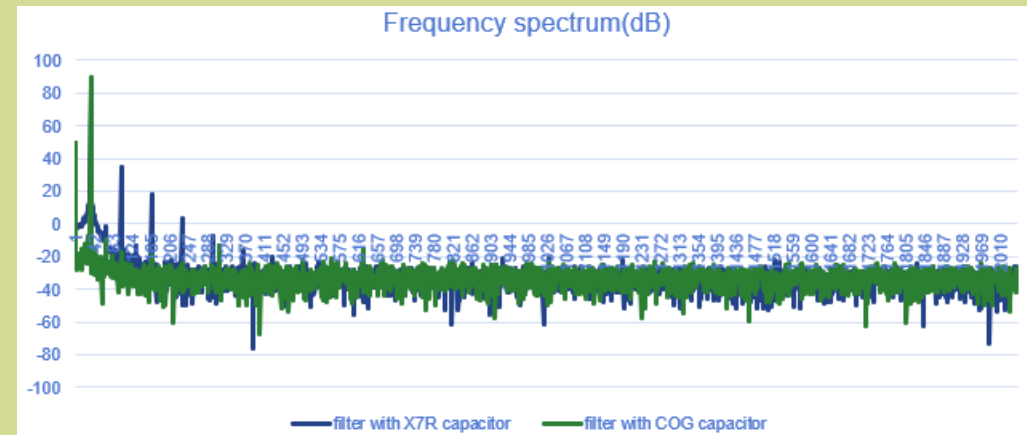
unit dB	SNR	SINAD	THD	SFDR	2ndHarm	3rdHarm
filter with COG capacitor	84.945	84.836	-100.902	95.126	-103.297	-106.736
filter with X7R capacitor	56.396	48.858	-49.7	49.796	-86.32	-49.796

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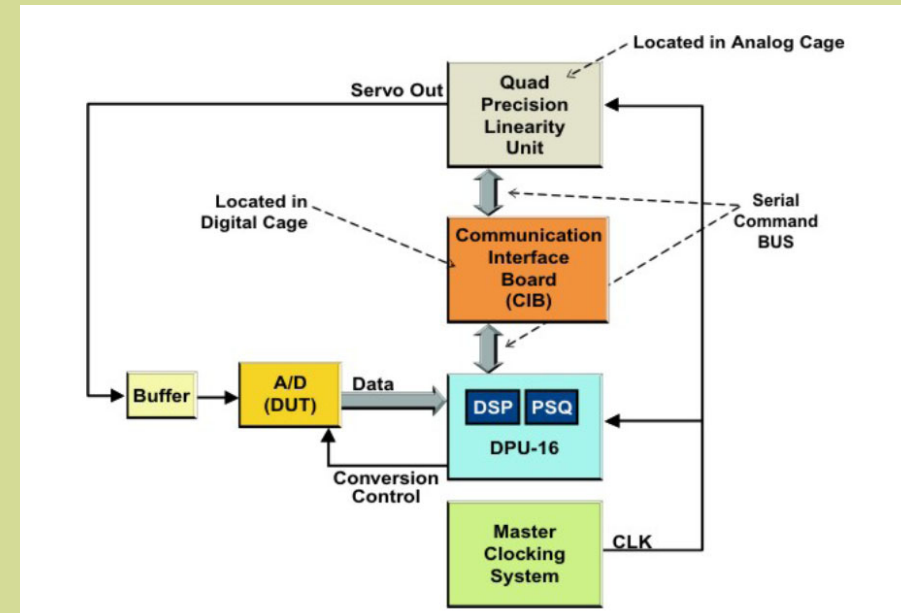
QPLU introduction

Quad Precision Linearity Unit(QPLU)

➢ Each PLU has two REF DACS(16bit)

➢ The SERVO loop consists of pedestal DAC, Dither DAC, PGA, and 16bit ADC.

➢ The Servo output has fixed mode and differential mode. The ADC we tested selects fixed mode, and only IN+ is connected to the Servo output.

➢ PLU also includes GND Force and GND Sense.

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QPLU setup for ADC test

The QPLU setup requires a communication interface board (CIB), DPU-16, a QPLU and HP 3458A meter.

➢ CIB used to communicate between the QPLU and DPU-16 DSP
➢ DPU-16 capture DUT output code and process data based on DSP board
➢ HP 3458A meter calibrates the pedestal voltage QPLU forced and input buffer error.

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QPLU rapid dither algorithm for linearity test

Rapid dither is a servo loop algorithm that searches the input voltage of the code left edge or right edge and takes hundreds or thousands of DUT code samples to find the code of interest. It consists of three stages.

- Transition Intercept (TI): quickly find code's input voltage , binary search, initial step size is large (100lsb or 200lsb), next step size is half of previous step size, during the search process, input using QPLU force pedestal voltage, output using DPU16 capture code for several samples, the average code will return to QPLU. After multiple QPLU searches, find the code of interest.
- Fast Dither (FD): fixed step size, typical is smaller than 1LSB, search results more accurate.
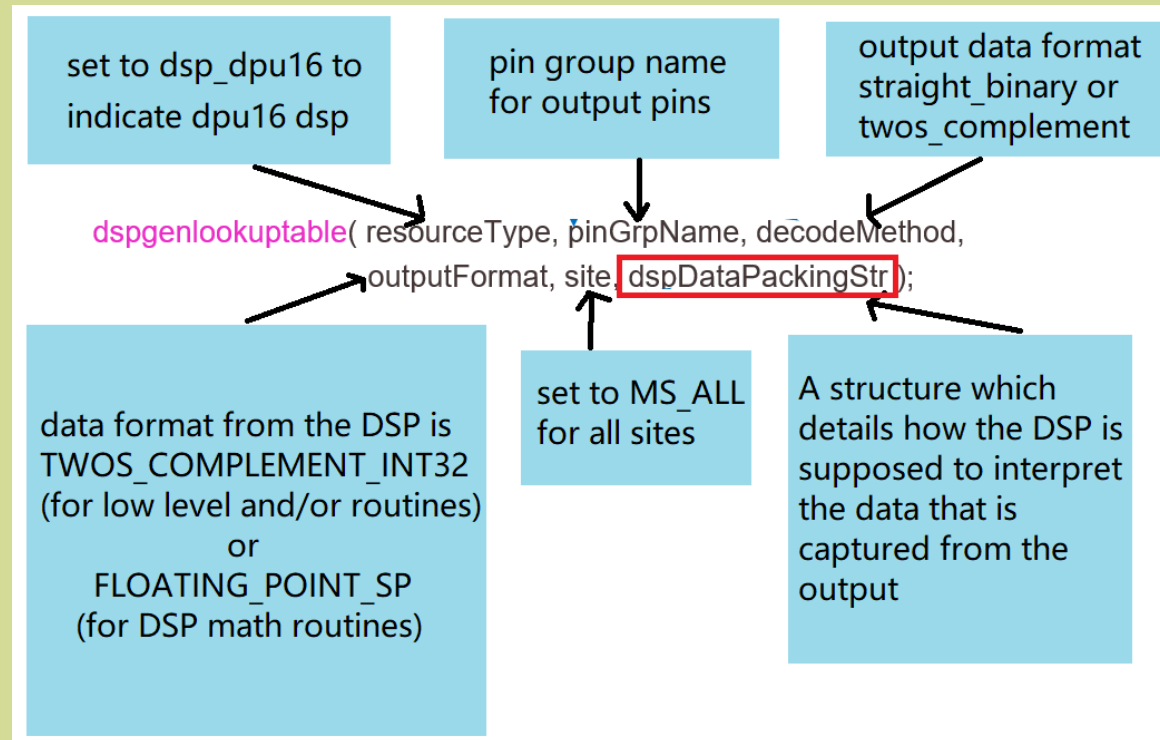- Slow Dither (SD): smallest step size, typical 0.1LSB, take stable values' average as the code's input voltage

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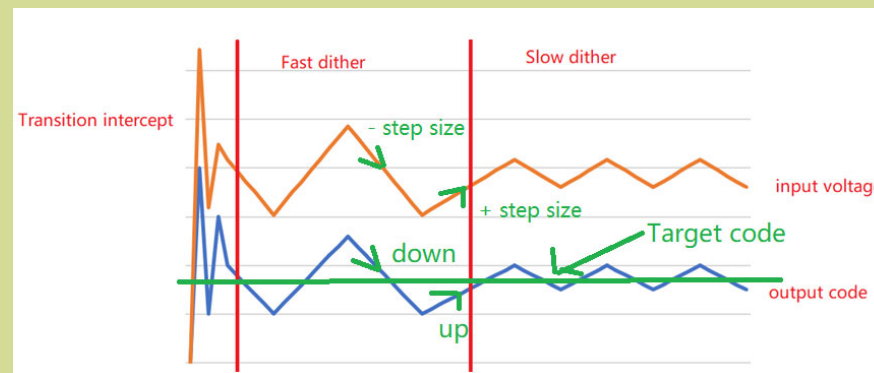
How to set various output data format

For ADC output data processing, the following factors will increase the complexity with multisite testing.

➢ Output type: serial or parallel
➢ Output data format: straight binary or twos complement

Here will use dspgenlookuptable() function, it can match various DUT output data formatting and data packing schemes.

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Dspgenlookuptable() function

set to dsp_dpu16 to indicate dpu16 dsp

pin group name for output pins

output data format straight_binary or twos_complement

dspgenlookuptable(resourceType, pinGrpName, decodeMethod, outputFormat, site, dspDataPackingStr);

data format from the DSP is TWOS_COMPLEMENT_INT32 (for low level and/or routines) or FLOATING_POINT_SP (for DSP math routines)

set to MS_ALL for all sites

A structure which details how the DSP is supposed to interpret the data that is captured from the output

dspDataPackingStr includes output data width, output type serial or parallel, if serial, set MSB

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Change ADC output code format by hardware

If want to change ADC output code format by hardware, can add a XOR gate for output pin. Below is the example how to change twos complement format to straight binary format.

➢ Add a XOR gate for Dout, allocate two DPU channels to XOR inputs and one DPU channel to XOR output.
➢ Reverse the 16th bit by XOR gate control to obtain straight binary output code.

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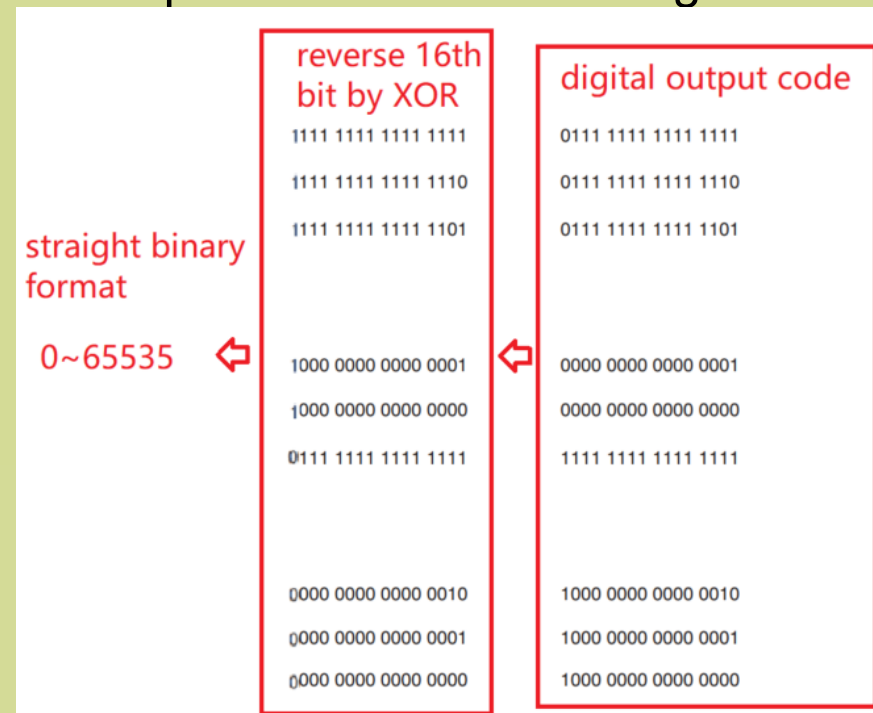
QPLU rapid dither algorithm programing

➢CUT loop: Code under test(CUT) table size

➢TI loop, FD loop and SD loop

➢Decision loop and Conversion loop

Multiple conversions per decision(MCPD) means average multiple DUT conversions without changing the servo loop voltage for one decision. The average value defines the direction of moving Dither DAC

Decision loop times decide how many times to change the direction
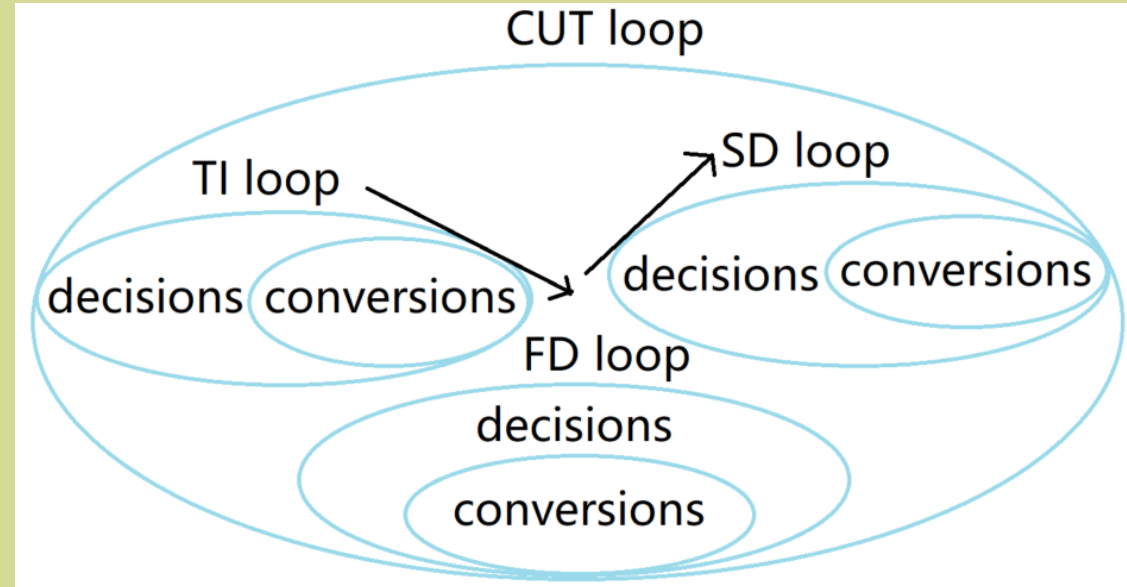
Qpluinterceptmode/qpludithermode use vector labels as input parameters

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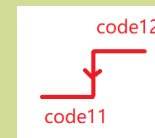
QPLU rapid dither MCPD setting

MCPD reduces the noise band and the likelihood of incorrect decisions. For example, find code 12 left edge

MCPD equal to 2 in TI, FD and SD loop
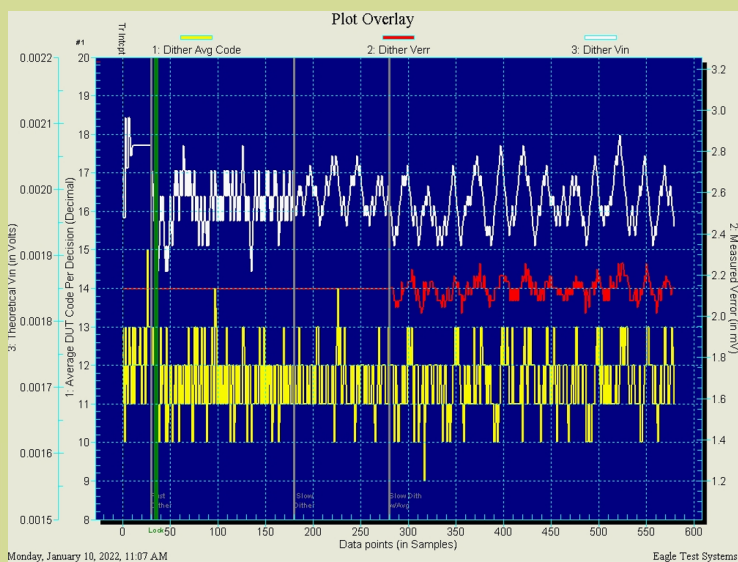
MCPD equal to 20 in TI, FD and SD loop
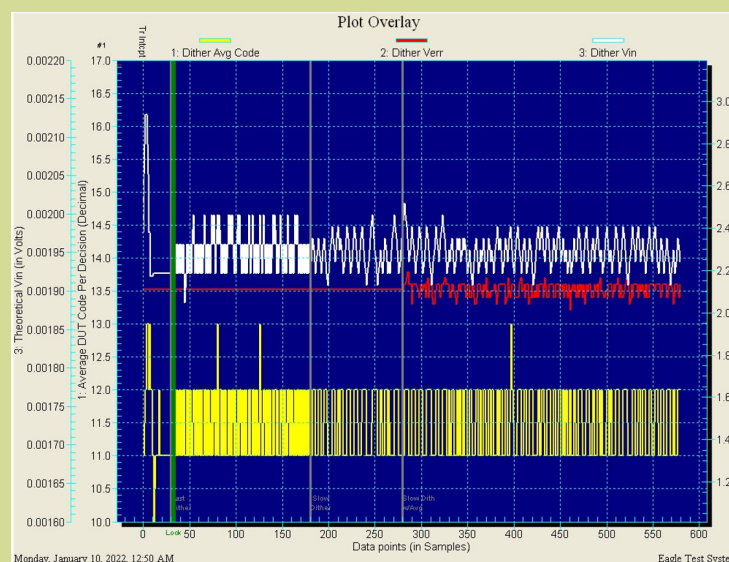
MCPD setting is based on Dither Avg code and Dither vin, most Dither Avg code should be target code and its edge code, Dither vin should be stable.

Note: in SD loop, 1lsb=76.29uV

MCPD	max code	min code	max Vin	min Vin	delta Vin	LSB
2	13	9	2.082mV	1.914mV	167.59uV	2.197lsb
20	13	11	2.014mV	1.908mV	106.64uV	1.398lsb

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How to check SAR ADC noise

Below two methods to check SAR ADC noise:

➢ Force a DC value, capture DUT output code many times and check if code fluctuate within normal range. In datasheet, code fluctuation is around 4.

➢ Force a pedestal value, use a small step size, increase step by step on the basis of the pedestal voltage, and capture each step's output code, see if the output code length is in 1lsb. PedestalDAC provides pedestal voltage, ditherDAC provides step size. This method is called DC sweep method.

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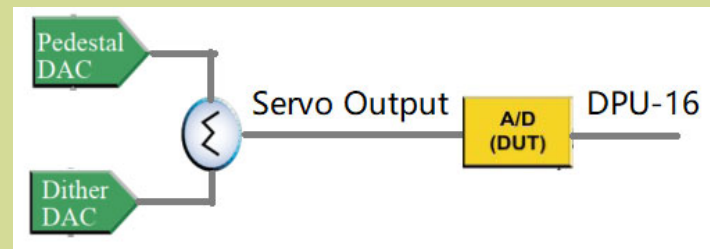
Summary

➢ To optimize ADC performance to design front-end filter and band pass filter

➢ QPLU rapid dither method based on a servo loop algorithm is fast and accurate for 16-bit SAR ADC linearity testing.

➢ Provide DC sweep method based on QPLU dither DAC to display SAR ADC transition noise.

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