Power Integrity in Load Boards from the GND Up

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TestConX™
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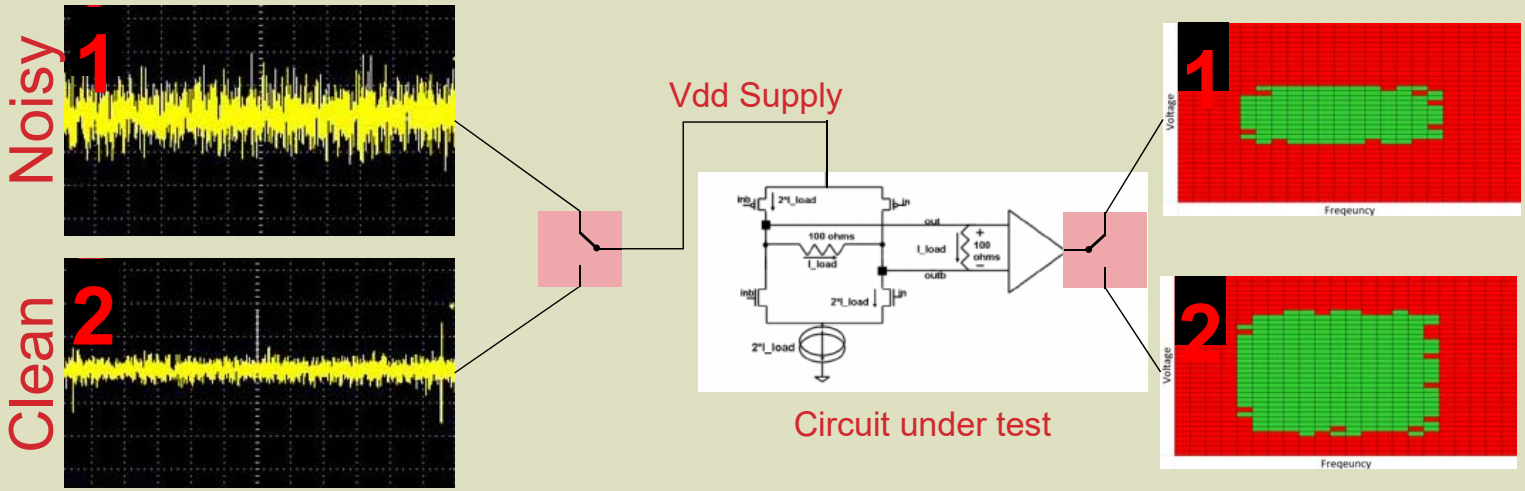
What is Power Integrity?

- Power Integrity (PI) is the behavior of your Power Distribution Network (PDN) as it relates to frequency
- Closely related is IR drop analysis, which is the behavior of your device at DC
  - IR drop analysis is relatively intuitive and deals with resistance and thermal concerns with in the board. *This is not addressed in this paper.*
- Power Integrity is typically represented as an Impedance. *(That's another way of saying "resistance as it relates to frequency"!)*

Why Do We Care About Power Integrity?

- PI relates to how the power supply ripples under load. (Both Vdd and GND!)
- As your power supply ripples, your ability to test your part will be reduced. Ripple on your supply will lead to a yield hit and you may not even be aware of it!



Yesterday's Model of PI: Rules of Thumbs

To Start:

- Capacitor scheme comes from device app notes for a soldered down device on a thin board

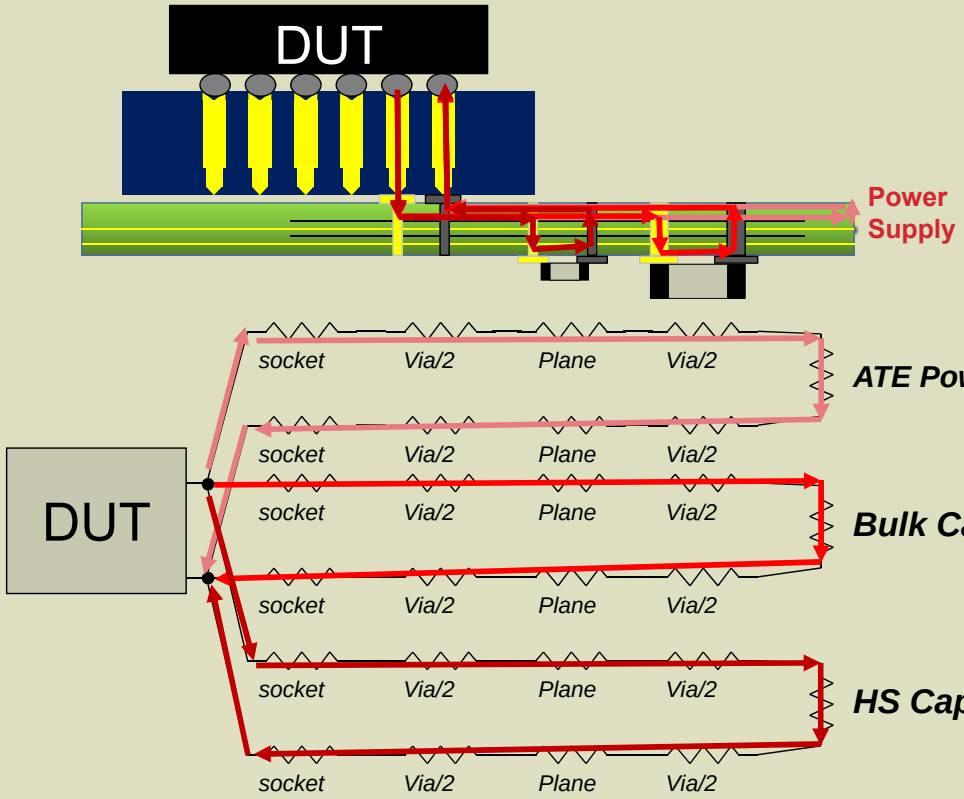
Apply Rules:

- Big caps can be placed anywhere on the board, but should be closer to DUT
- Small capacitors must be placed on back side of DUT
- Power and ground planes should be close together
- Shorter is better

And if it fails:

- Add more capacitors!
- Hold meetings and come up with wild guesses at what may be causing the problem!

Board Impedance from the DUT (Frequency Domain View)



- At DC, path of least resistance is to the power supply
- At medium frequencies, the path of least resistance is to the bulk or mid sized caps
- At High Frequencies, the path of least resistance is to the high speed caps

0 Hz to ~ 10 kHz

~10 kHz to ~ 1 MHz

~1 MHz to ~ 50 MHz

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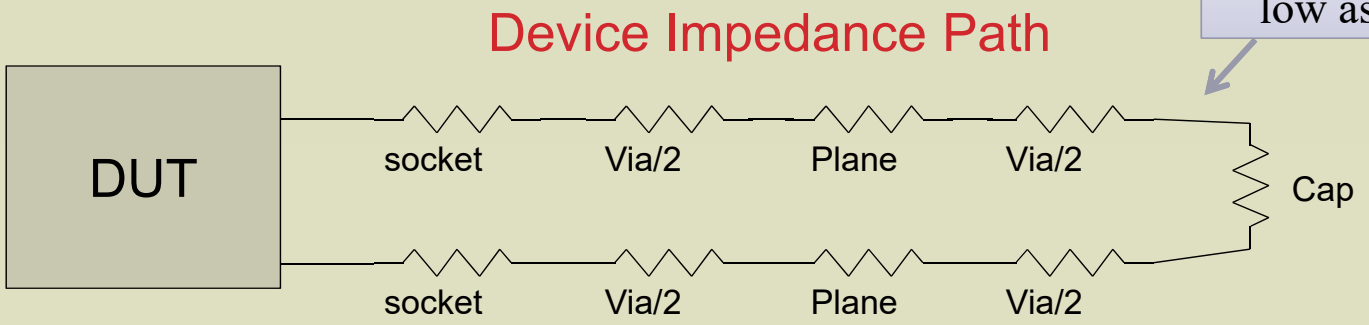
A Closer Look…

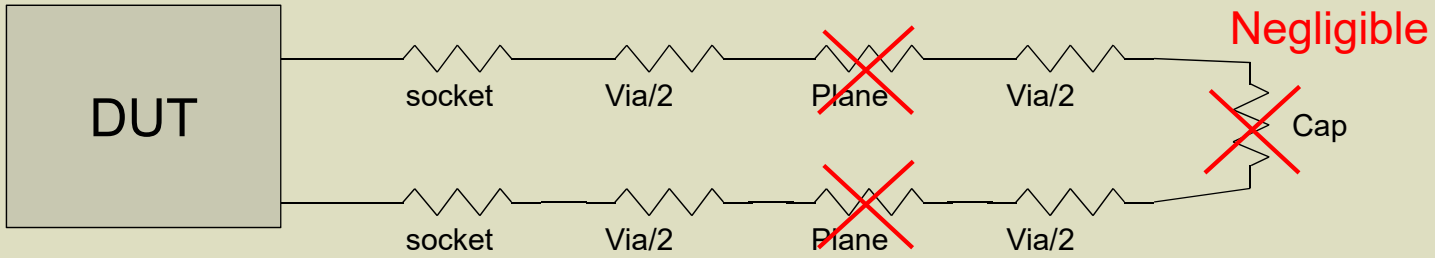
- Path impedance is a measure of how well the by-pass caps can get rid of HF energy
- This determines the capacitor's ability to "help" the DUT with PI

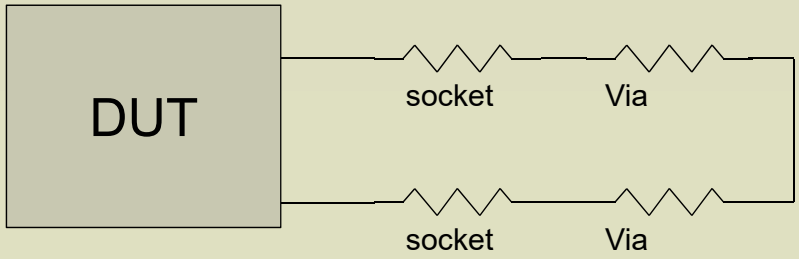
- Inductors and capacitors look like resistance at a fixed frequency (Remember phasors!)
- The higher the path inductance, the higher the resistance at frequency

We want this path resistance to be as low as possible!



HF DUT Impedance Path Example

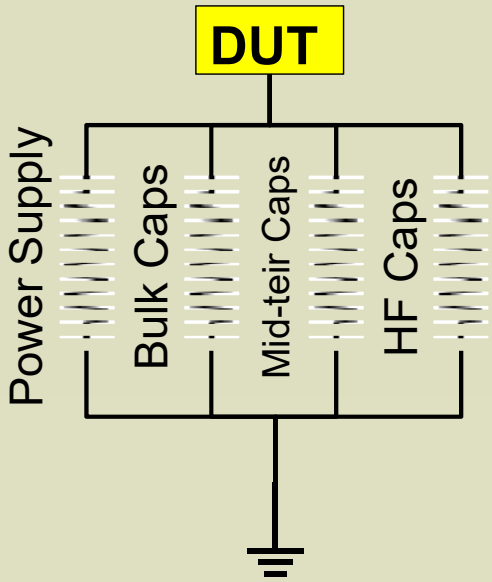


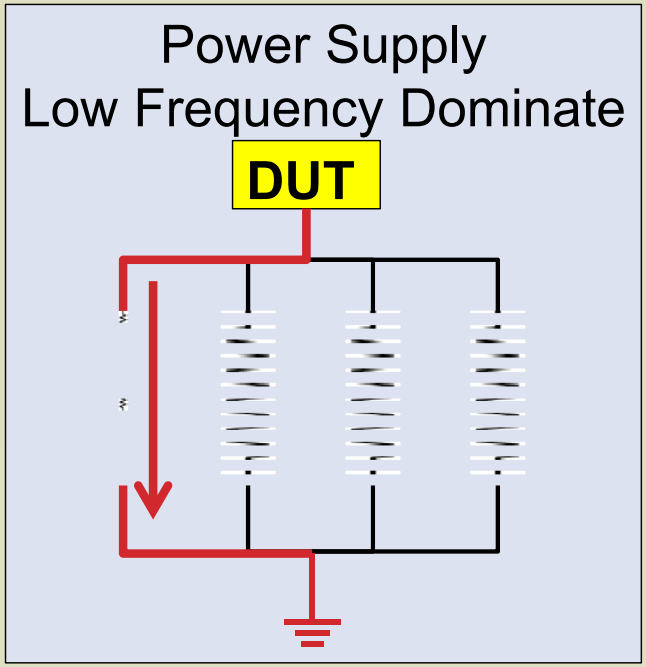


- Via and Socket Inductance often dominate the high frequency response
- Reducing the inductance of these two pieces will dramatically improve high frequency PI performance!
- Your DUT socket is also a critical piece of the PI puzzle

Impedance in Parallel

- The system will look like resistors in parallel and will find the lowest impedance path



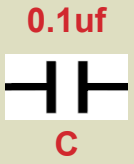


At different frequency bands, alternate paths will provide the "path of least resistance"

Capacitor Modeling

Modeling Tradeoff Example: MLC Capacitor

Ideal Model



Model w/Parasitics

$$Z = \frac{1}{(S)C} \quad \text{or} \quad \frac{1}{(j\omega)C}$$

$$Z = \frac{S^2 + S\left(\frac{R}{L}\right) + \frac{1}{LC}}{\frac{S}{L}}$$

$$Z(j\omega) = j\omega^2 - \frac{j}{LC} + \frac{\omega R}{L}$$

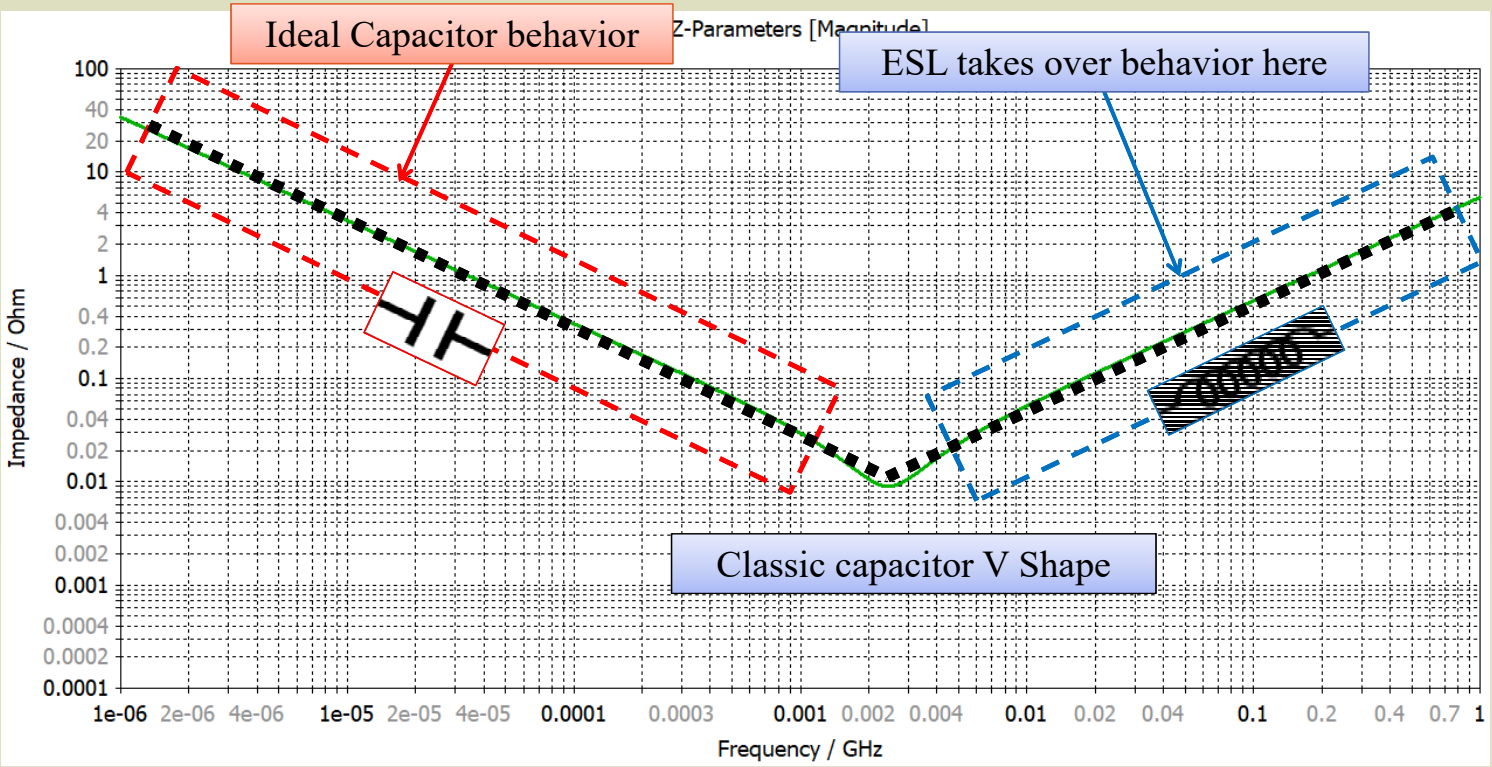
Generic Capacitor Model

1210

4.7uF

ESR: 9mΩ

ESL: 0.9nH



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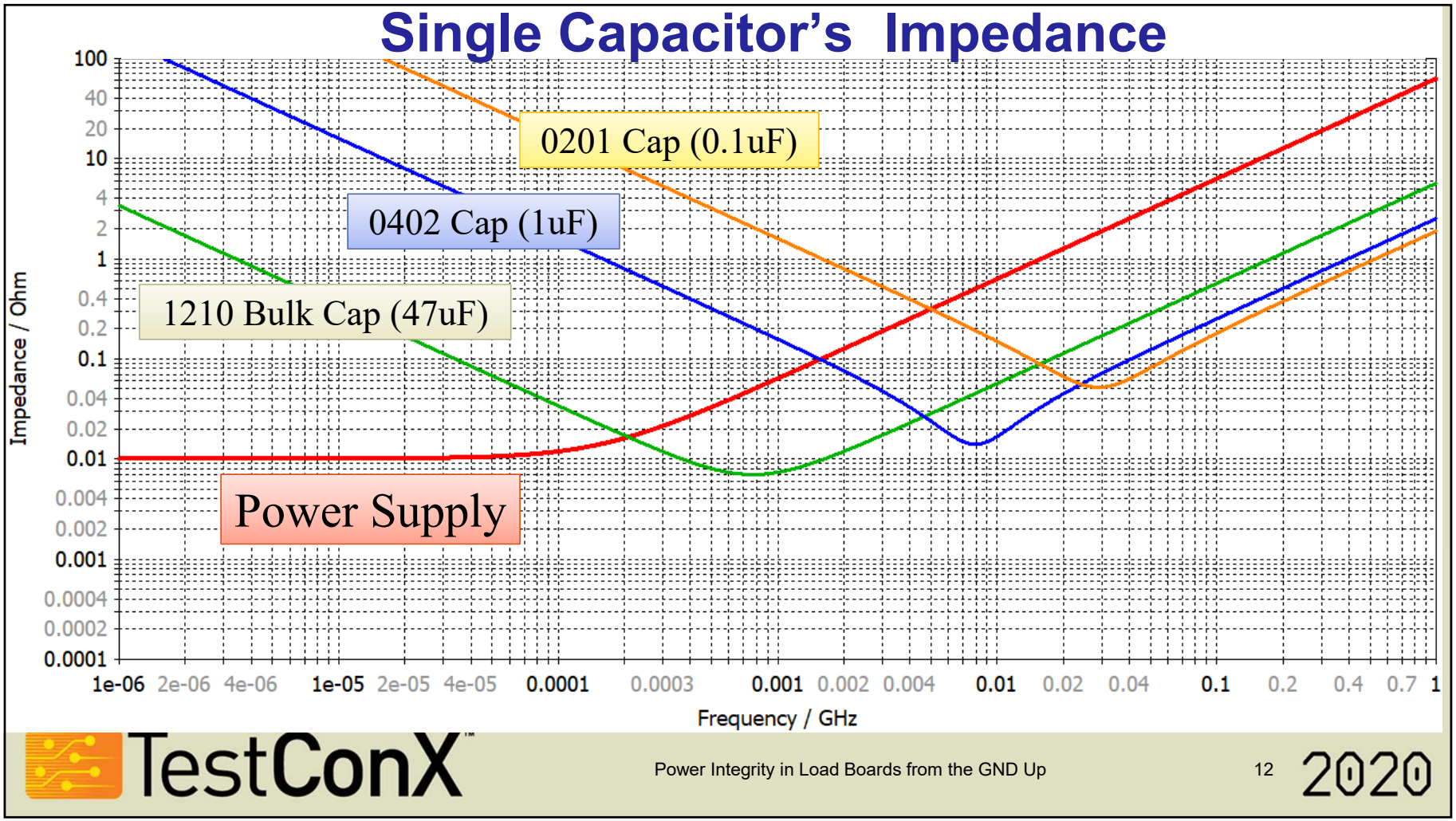
Impedance Plots in Detail

- Single Capacitor Impedance
- Parallel Capacitor Impedance
- Complete Power Net Impedance
- Typical Board Simulation Results
- Including Sockets

We will step through the plots to help understand in detail


Single Capacitor's Impedance
0201 Cap (0.1uF)
0402 Cap (1uF)
1210 Bulk Cap (47uF)
Power Supply
Impedance / Ohm
100
40
20
10
4
2
1
0.4
0.2
0.1
0.04
0.02
0.01
0.004
0.002
0.001
0.0004
0.0002
0.0001
1e-06 2e-06 4e-06 1e-05 2e-05 4e-05 0.0001 0.0003 0.001 0.002 0.004 0.01 0.02 0.04 0.1 0.2 0.4 0.7 1
Frequency / GHz
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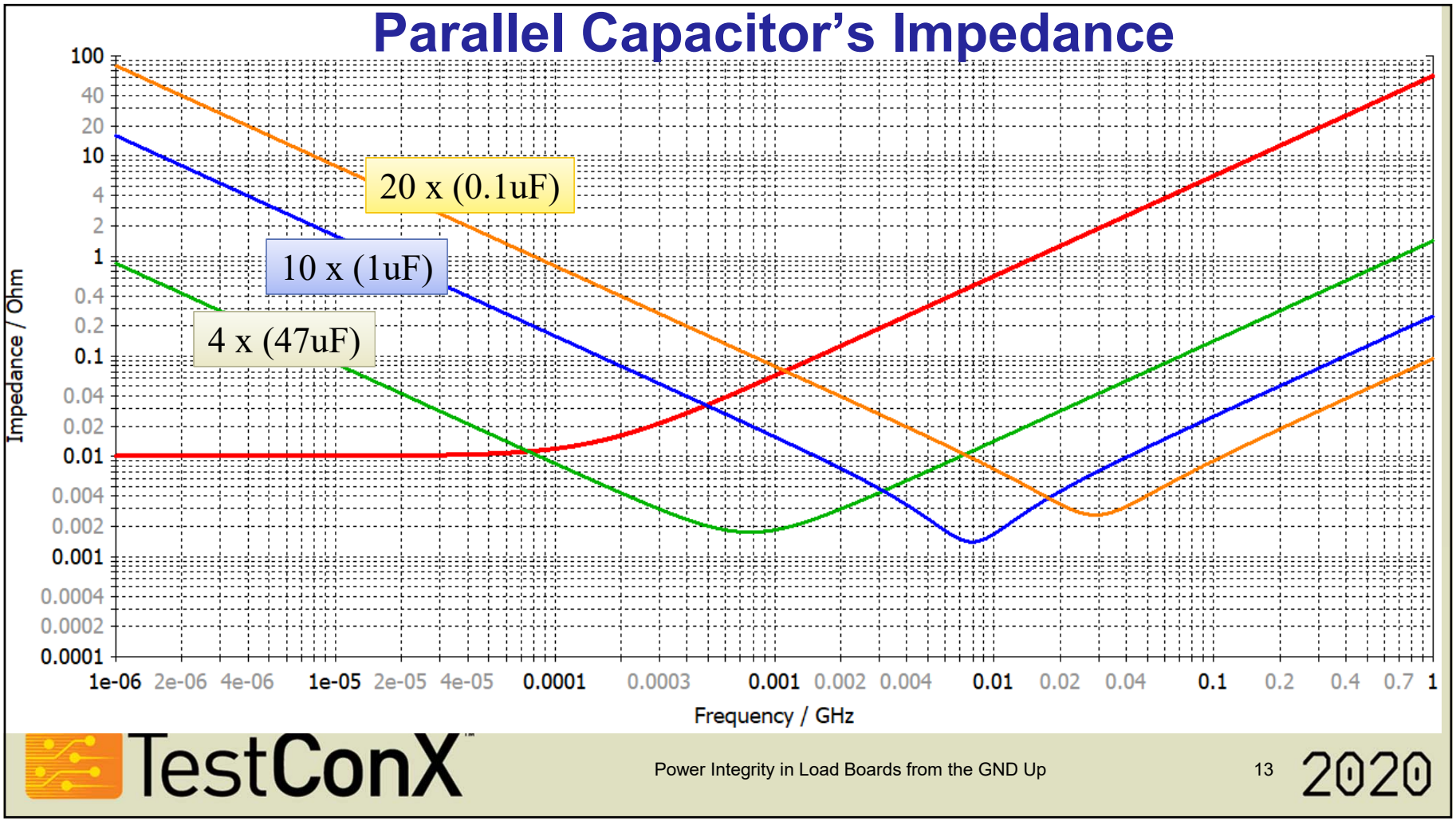
Parallel Capacitor's Impedance
20 x (0.1uF)
10 x (1uF)
4 x (47uF)
Impedance / Ohm
100
40
20
10
4
2
1
0.4
0.2
0.1
0.04
0.02
0.01
0.004
0.002
0.001
0.0004
0.0002
0.0001
1e-06 2e-06 4e-06 1e-05 2e-05 4e-05 0.0001 0.0003 0.001 0.002 0.004 0.01 0.02 0.04 0.1 0.2 0.4 0.7 1
Frequency / GHz
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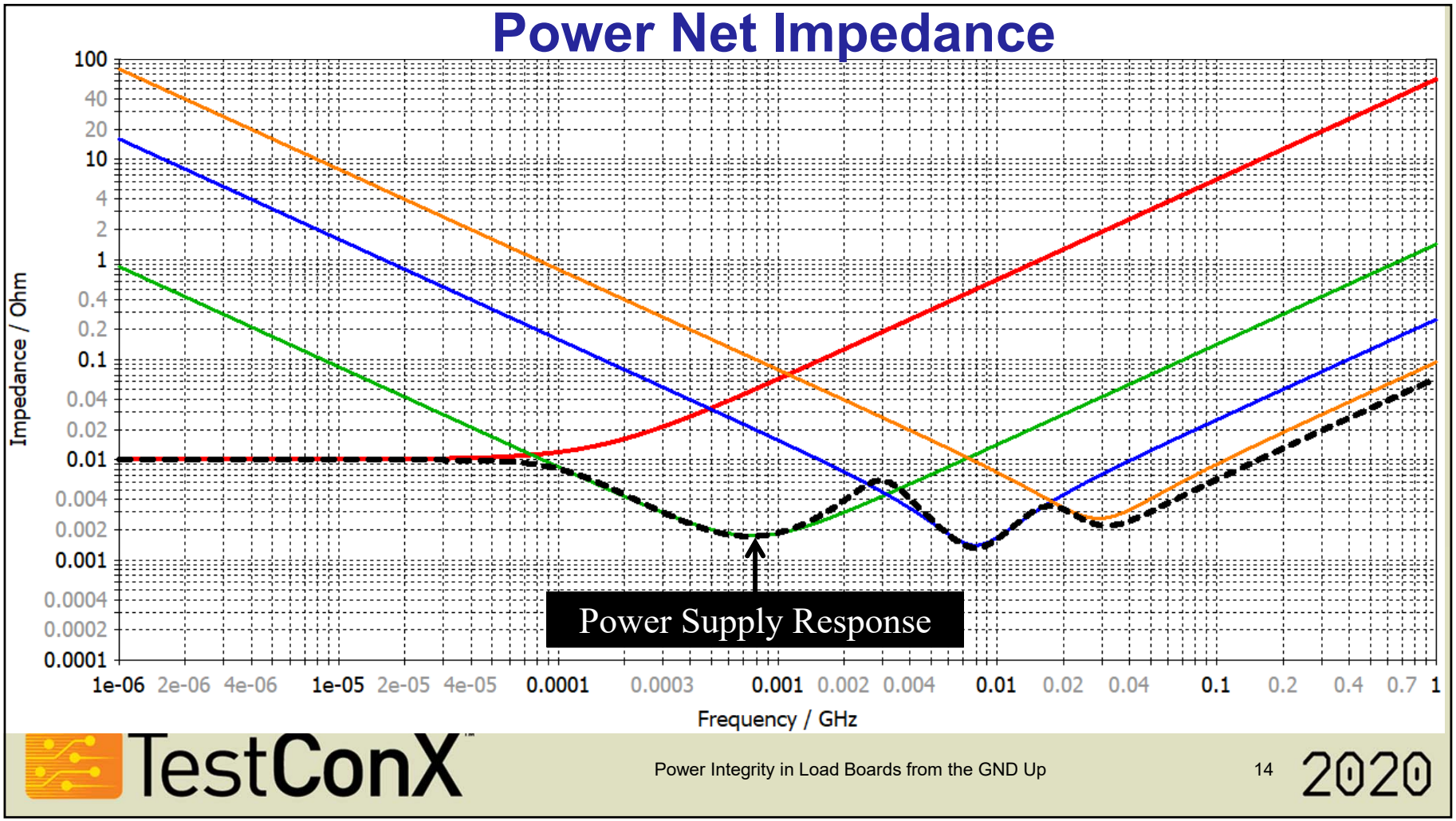
Power Net Impedance
Impedance / Ohm
100
40
20
10
4
2
1
0.4
0.2
0.1
0.04
0.02
0.01
0.004
0.002
0.001
0.0004
0.0002
0.0001
1e-06 2e-06 4e-06 1e-05 2e-05 4e-05 0.0001 0.0003 0.001 0.002 0.004 0.01 0.02 0.04 0.1 0.2 0.4 0.7 1
Frequency / GHz
Power Supply Response
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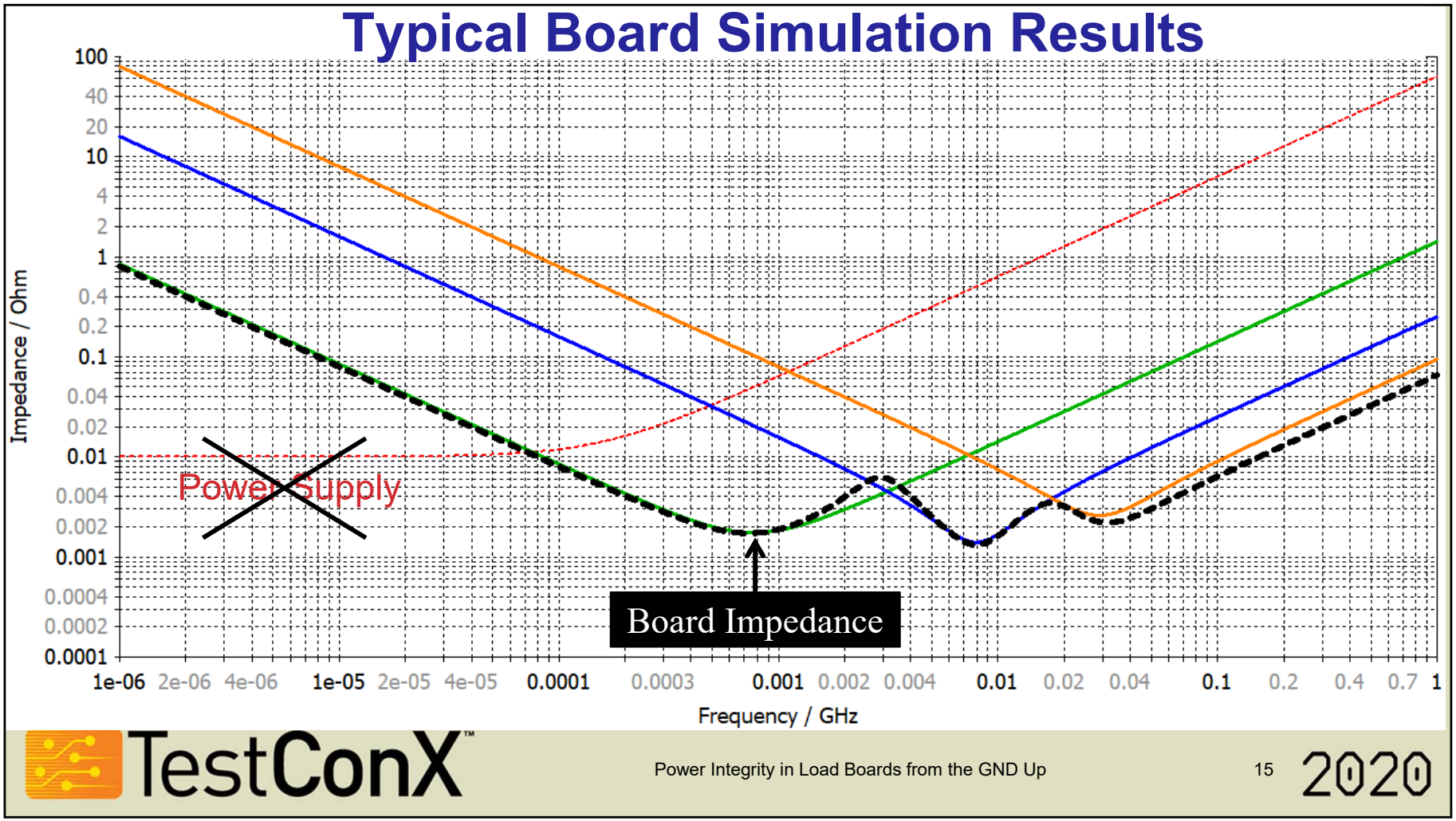
Typical Board Simulation Results
Impedance / Ohm
100
40
20
10
4
2
1
0.4
0.2
0.1
0.04
0.02
0.01
0.004
0.002
0.001
0.0004
0.0002
0.0001
Power Supply
Board Impedance
1e-06 2e-06 4e-06 1e-05 2e-05 4e-05 0.0001 0.0003 0.001 0.002 0.004 0.01 0.02 0.04 0.1 0.2 0.4 0.7 1
Frequency / GHz
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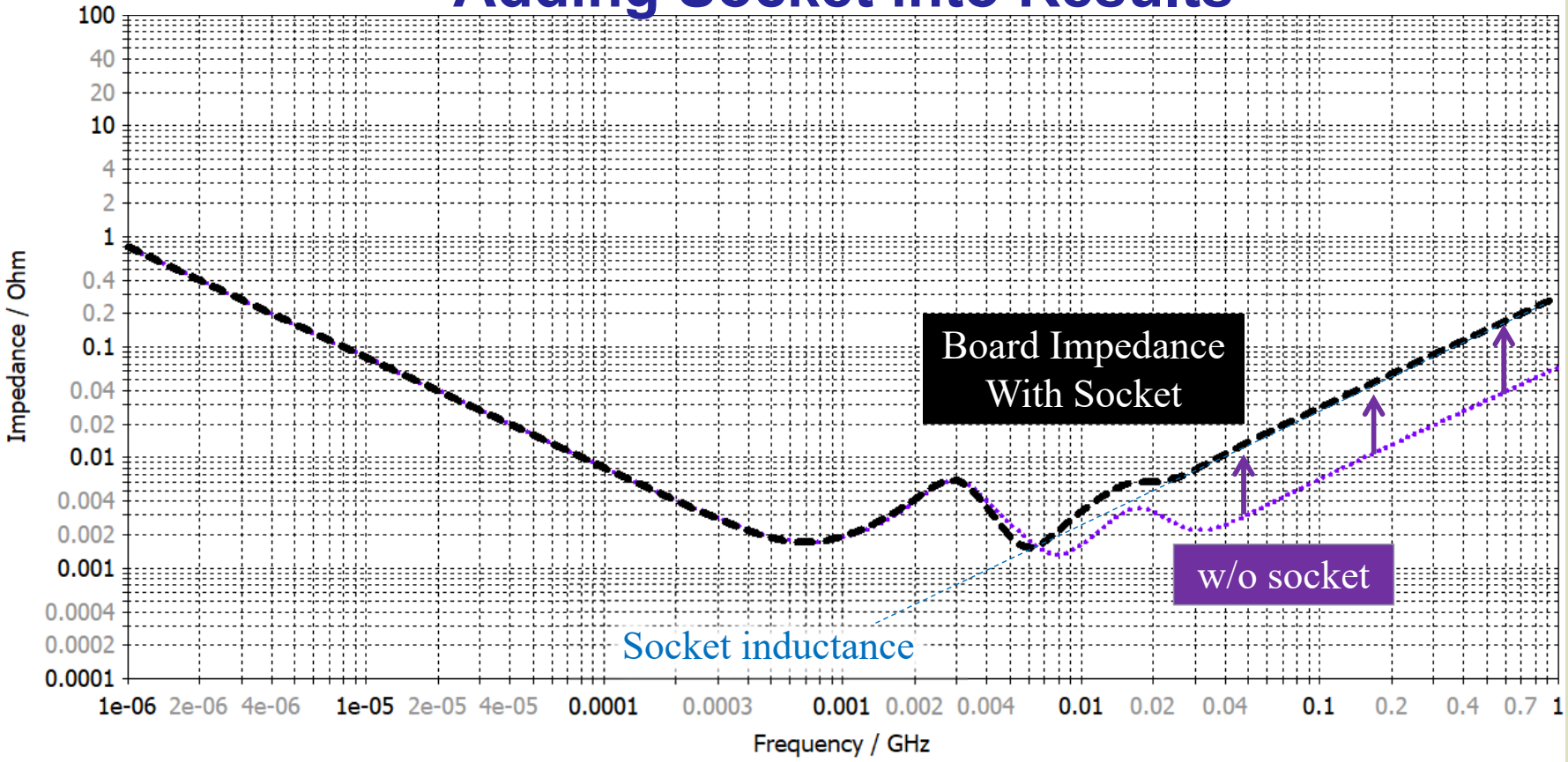
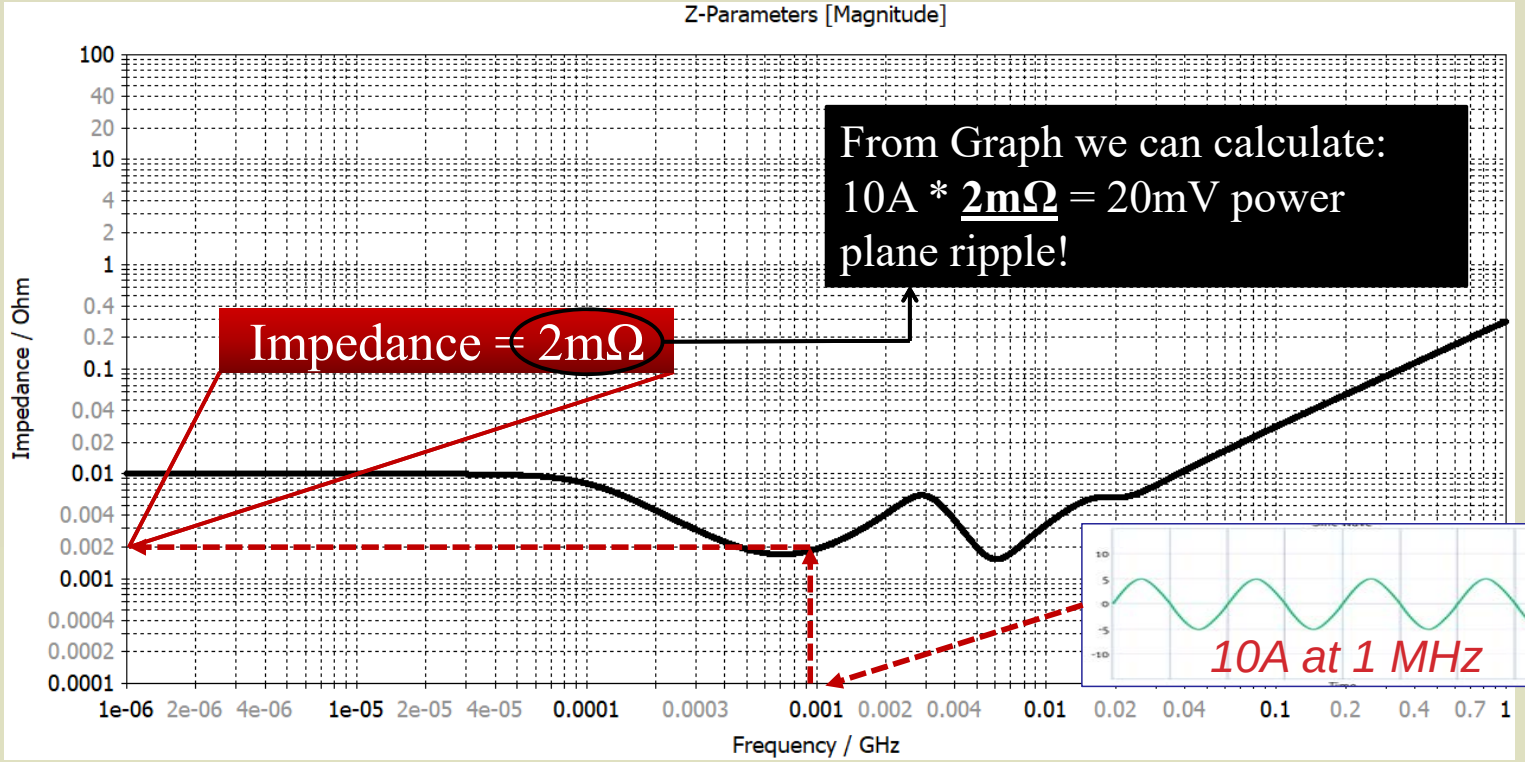
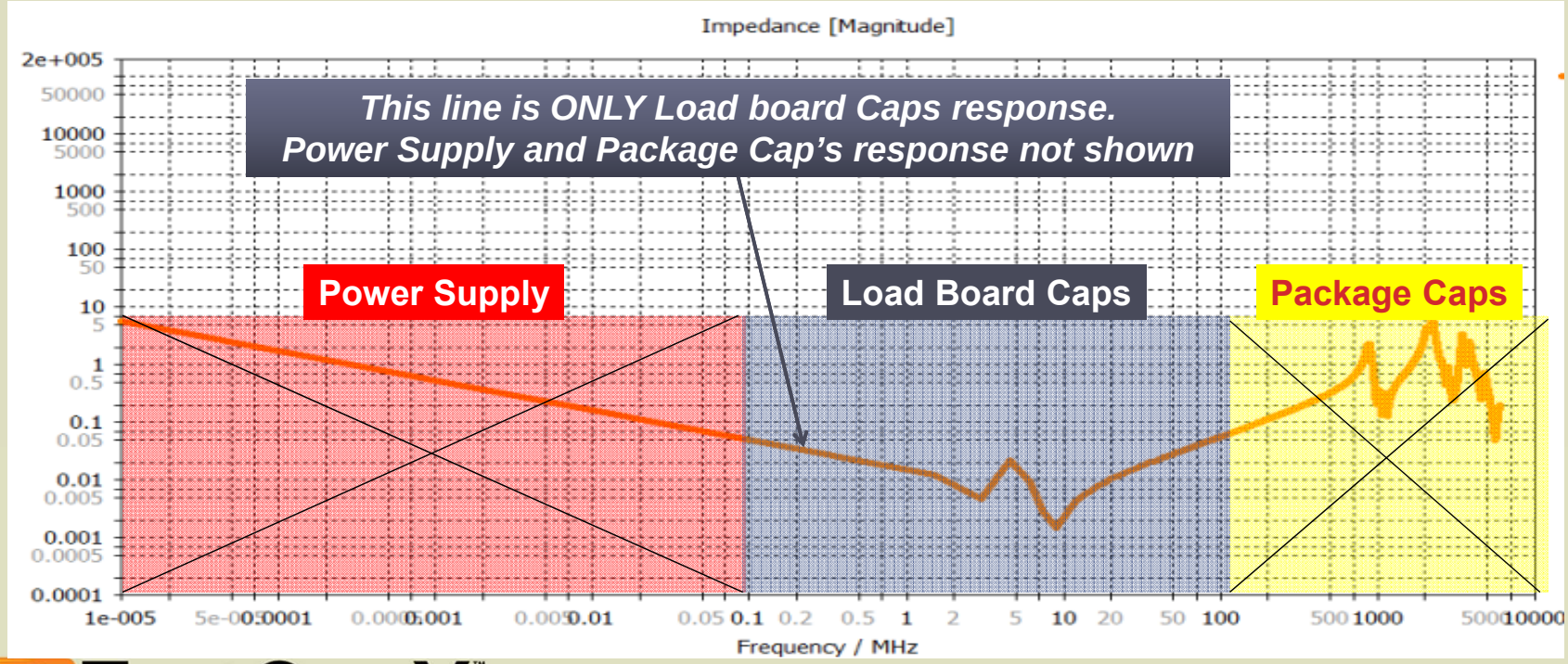
Adding Socket into Results



How Do I Use an Impedance Chart?



Different Response Regions for ATE Board



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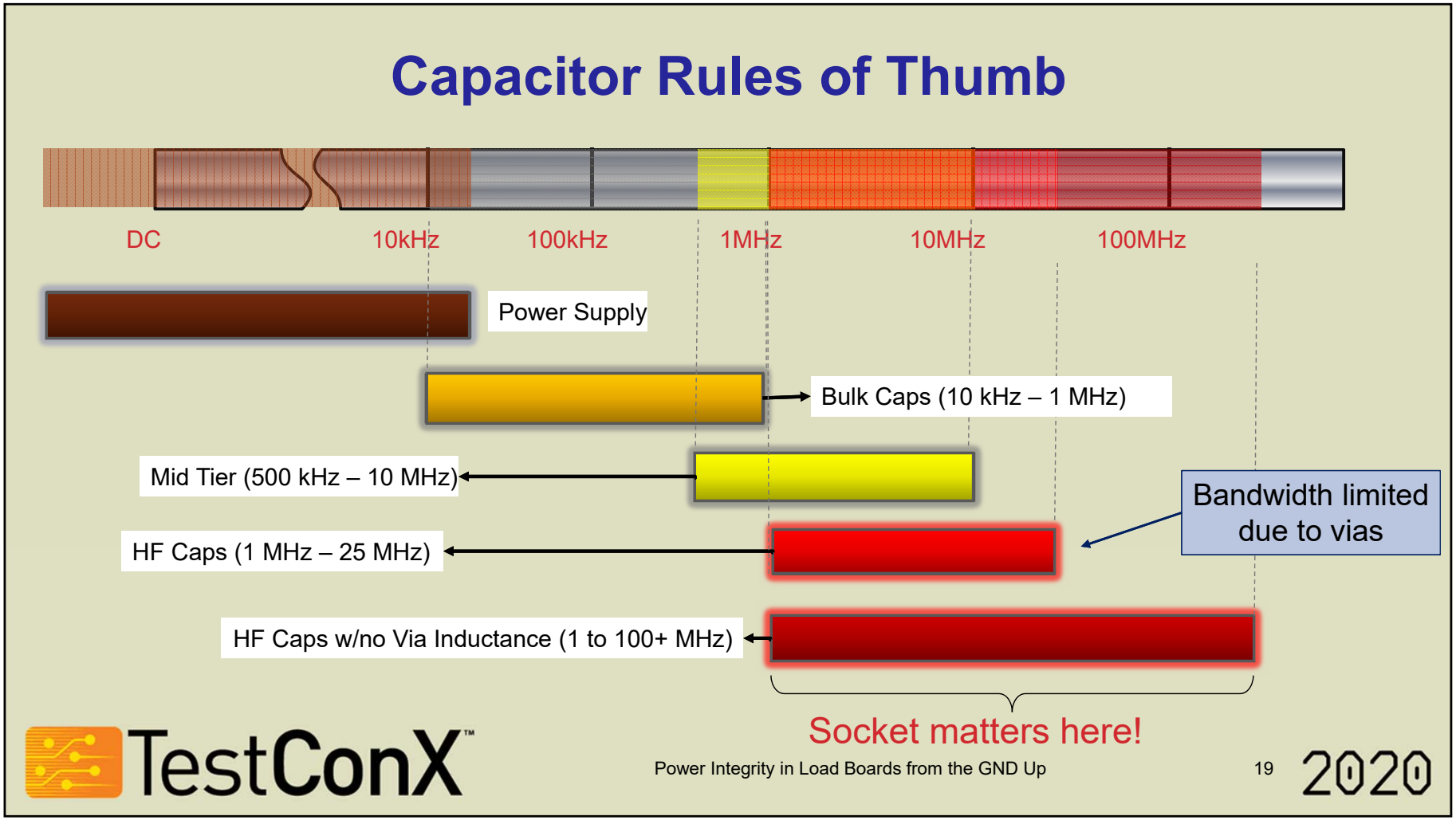
Capacitor Rules of Thumb
DC
10kHz
100kHz
1MHz
10MHz
100MHz
Power Supply
Bulk Caps (10 kHz – 1 MHz)
Mid Tier (500 kHz – 10 MHz)
HF Caps (1 MHz – 25 MHz)
Bandwidth limited due to vias
HF Caps w/no Via Inductance (1 to 100+ MHz)
Socket matters here!
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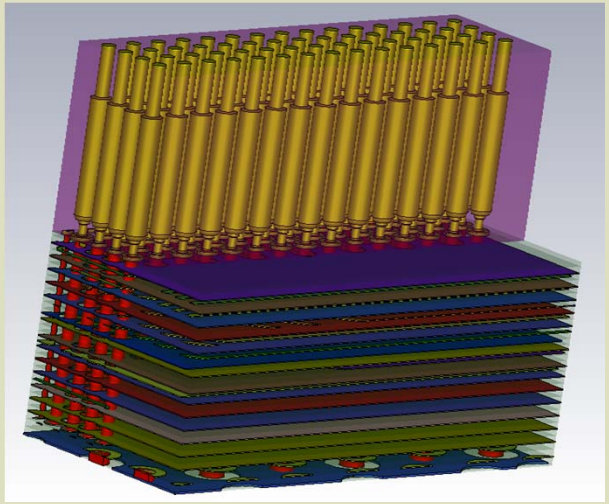
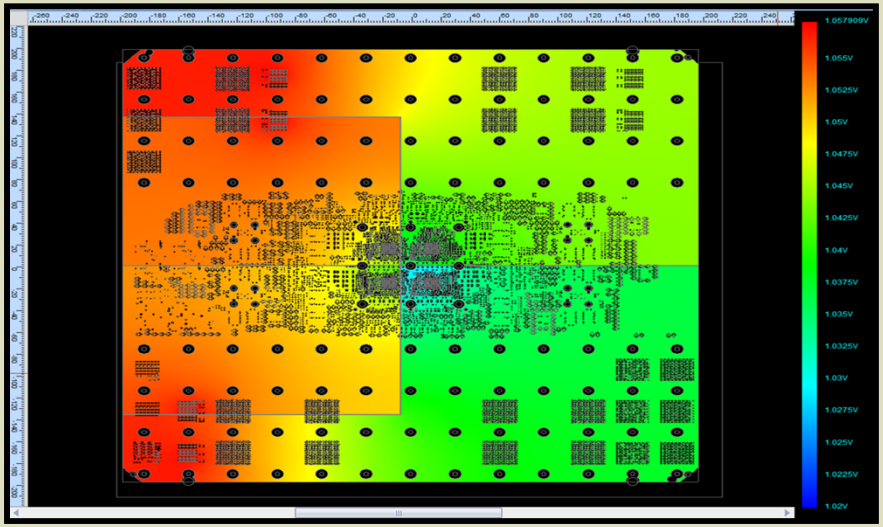
Load Board Power-Integrity Analysis





Simulation should take into account all aspects of the board design, including capacitor models, power planes routing, and socket performance
95% of PI modeling in ATE does not include the socket

PI Strategy

Initial Pre-Layout Simulations

- Use previous design results and pre-modeled results to estimate performance before layout
  - This is very useful for quick “what if” analysis. (What if you add more bulk caps? What if you add more high speed caps? What if you add EC? Etc.)
  - We have seen good correlation between spice and Full Board Simulations
  - Simulation time is minutes

Final Post-Layout Full Board Simulations

- Import finished design into simulation tool and model entire board PI
  - These simulations are full board simulations and include power plane effects
  - Socket is not included and if possible should be added after completion
  - Simulation time can be 10-20 hours

PI: The Ideal Full System Analysis

- Power Integrity can be done as either
  - board only
  - board + socket
  - board + socket + package & test program model
- Time domain results can only be calculated only with all of the above sections
- *More chip makers should implement a full system PI analysis!*

Example PI Impedance Result Summary

No	Power Rail Name	Criteria			Result	
		PCB Target Impedance			PI Impedance Analysis	
		Value (mΩ)	Minimum Frequency	Maximum Frequency	SITE0 PCB Maximum Impedance (mΩ)	SITE1 PCB Maximum Impedance (mΩ)
1	VDD_I	17	100kHz	20MHz	10.53	10.67
2	HVCC	18	100kHz	20MHz	16.23	14.58
3	LVCC	18	100kHz	20MHz	12.01	11.74

Spec

PI is typically listed at specific frequency points to make defining targets easier

Simulation Results

Socket Power Integrity

"Standard"

- The baseline performance

Coax

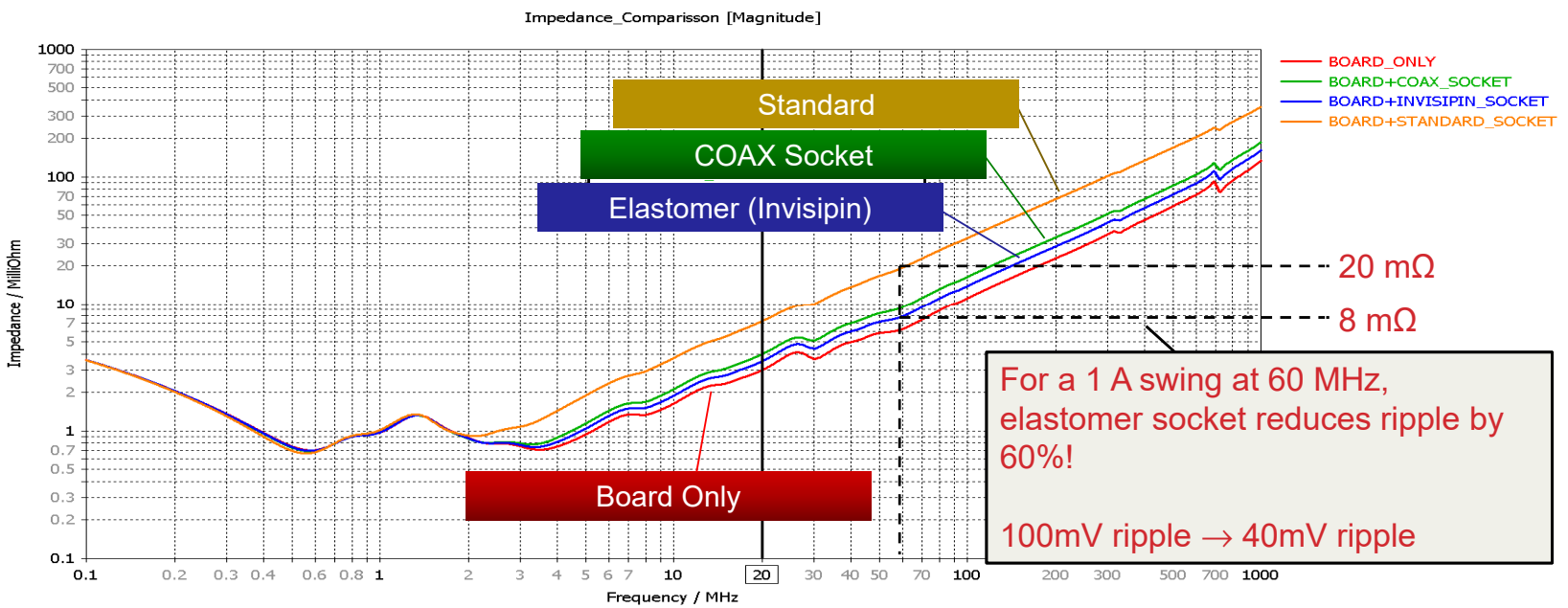
- Power pins specifically designed for low inductance. *(This will not be true for all coax sockets!)*

Elastomer

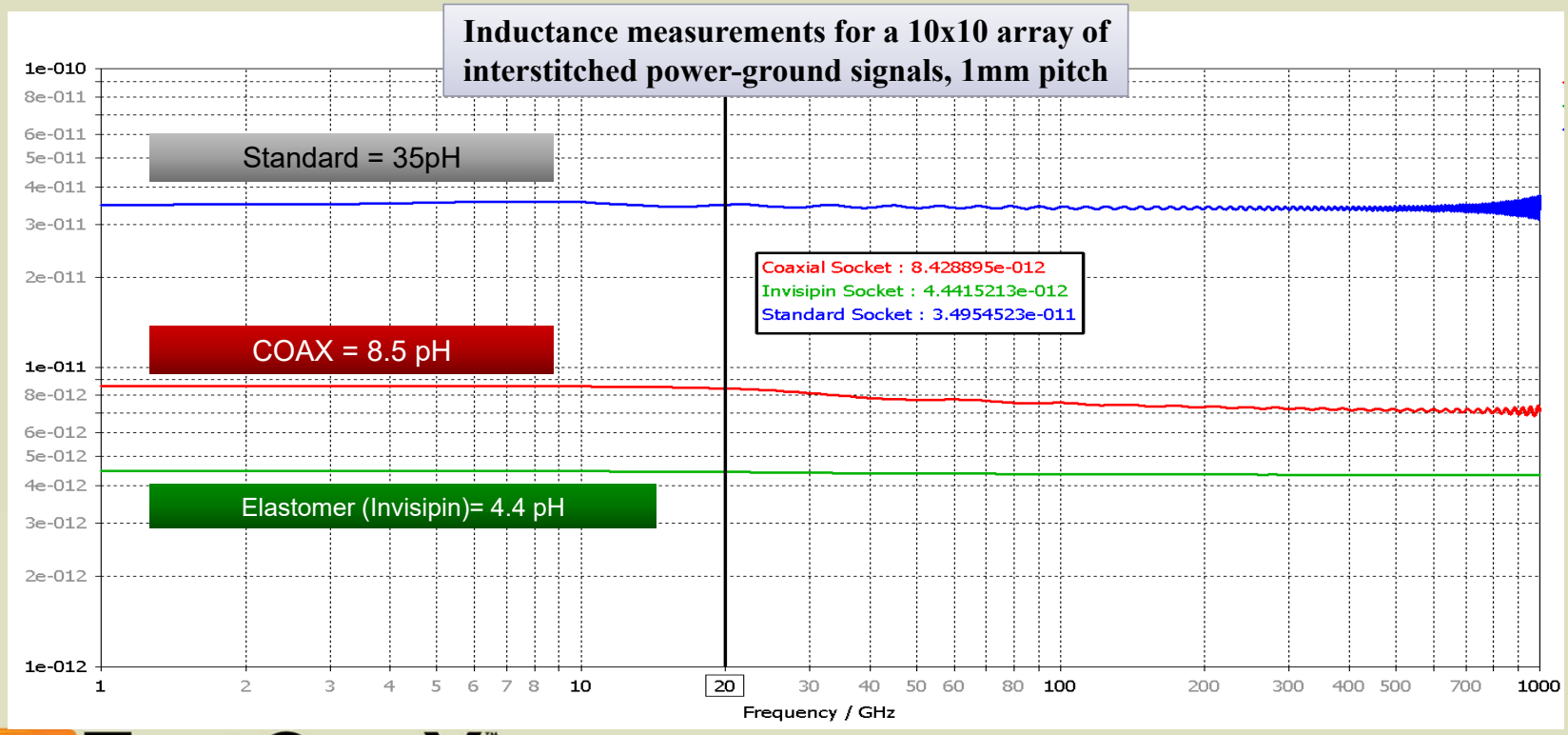
- Inductance is proportional to length, so the ultra short height of elastomers makes this solution have very low inductance

Adding Sockets To a simulated Power Net

(This is a standard board with no “tricks” to reduce via impedance)



Socket Inductance Values



Conclusion

- As an industry we need to do better on power integrity and use the tools available
- Impedance plots are valuable and straight forward method of analyzing your power net response
- Sockets are a critical part of the PI of the system

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