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-1 dB insertion loss to 90 GHz ?

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BiTS Workshop
March 4 - 7, 2018



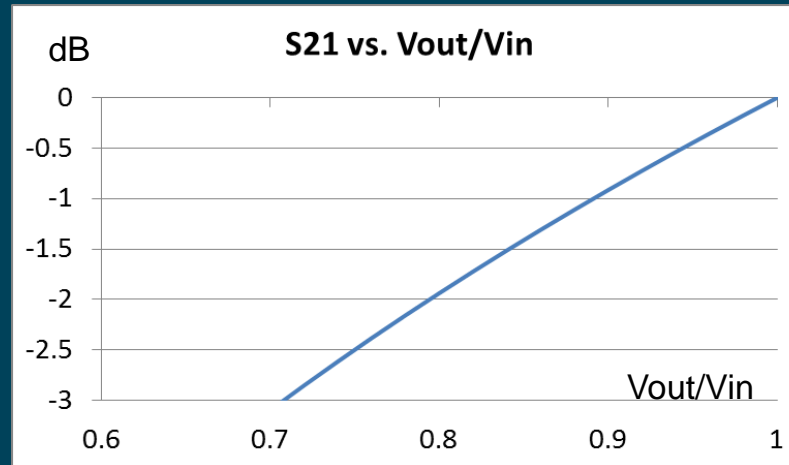
Objective

- Examine contact characteristics at elevated frequencies
- Identify key parameters for best performance
- Illuminate significance of these parameters
- Offer some insight why expectations are not always met

Approach

- Present existing -1 dB data
- Design experiments to identify insertion loss contributions
- Set up and run simulations that exemplify significance of individual contributors

- 1dB ?



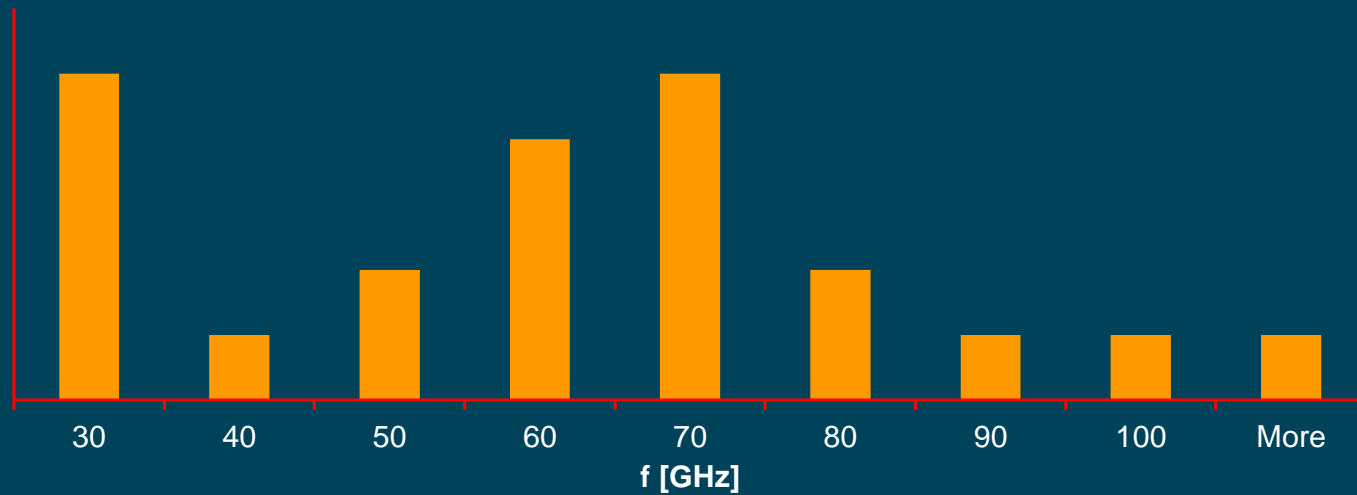
Insertion loss S21 is defined by ratio of output signal level at port 2 vs. input signal level at port 1 of an interconnect/socket

$$S21 = 10 * \log(P_{out}/P_{in}) = 20 * \log(V_{out}/V_{in})$$

Measured -1 dB frequencies

(sockets for potential automotive radar applications – tested at GWN)

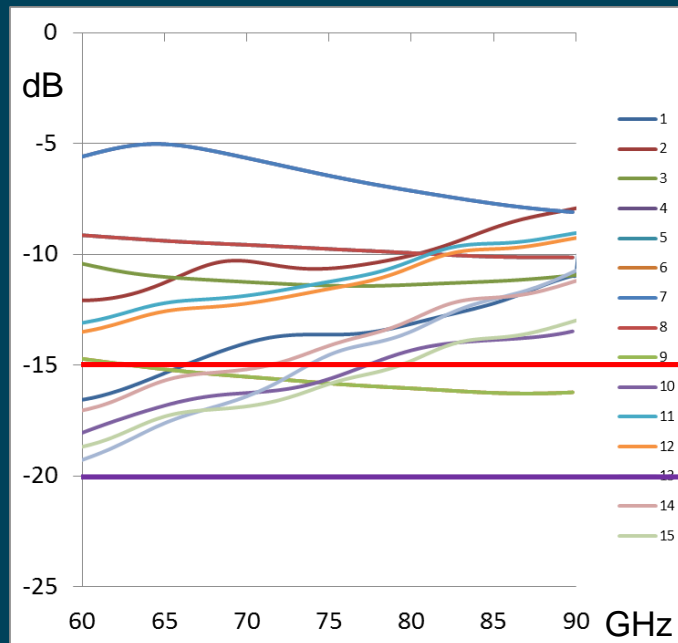
Histogram



A collection of -1dB insertion loss points

Return loss examples

Return loss defined by ratio of source signal level vs. reflected amplitude level at port 1 (S11) or port 2 (S22)



-15 dB may be more suitable above 60 GHz

-20 dB is an often used metric at "lower" frequencies

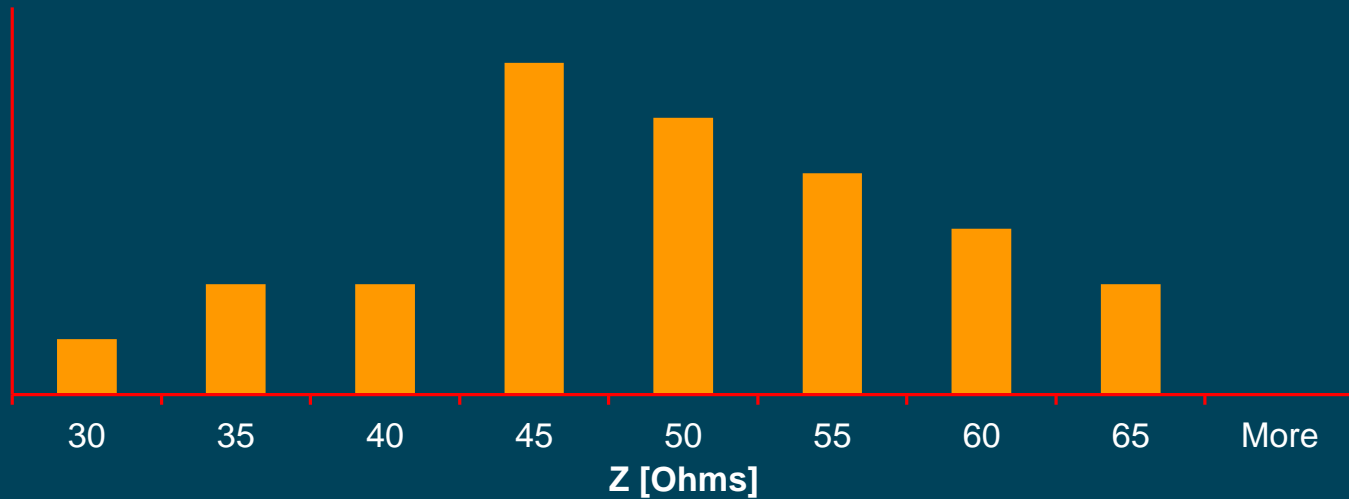
From measurements - modified to make the actual response unidentifiable

-1 dB insertion loss to 90 GHz ?

Measured impedance levels

(sockets for potential automotive radar applications – tested at GWN)

Histogram

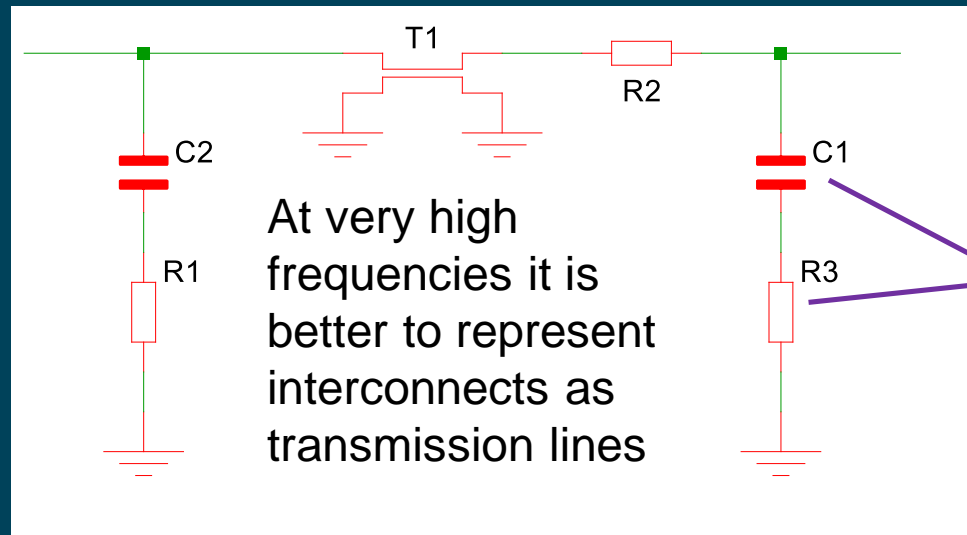


Characteristic impedance

Parameters to be examined

- Impedance
- Pitch
- Contact length
- Contact materials, plating
- Surface roughness
- Dielectric materials / loss tangent

Line impedance impact

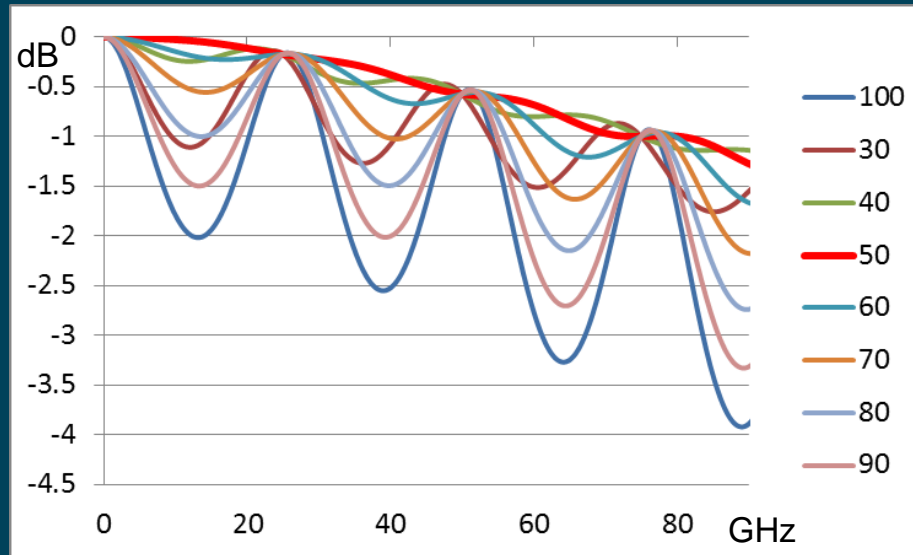


At very high frequencies it is better to represent interconnects as transmission lines

Parasitics (to model loss and fixture contributions)

Simulation circuit (SPICE simulation for simplicity)

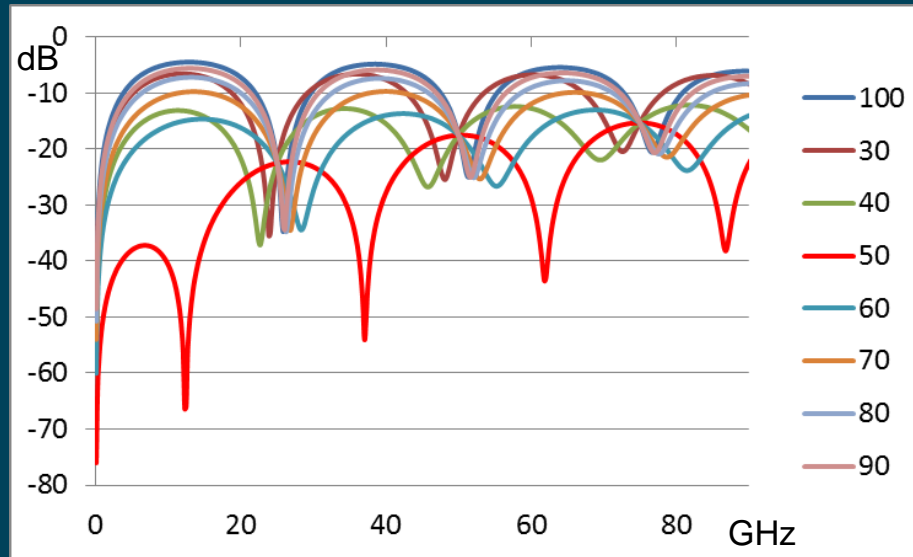
Line impedance impact



* Line length was fixed at 20 ps

Insertion loss for different line impedance levels

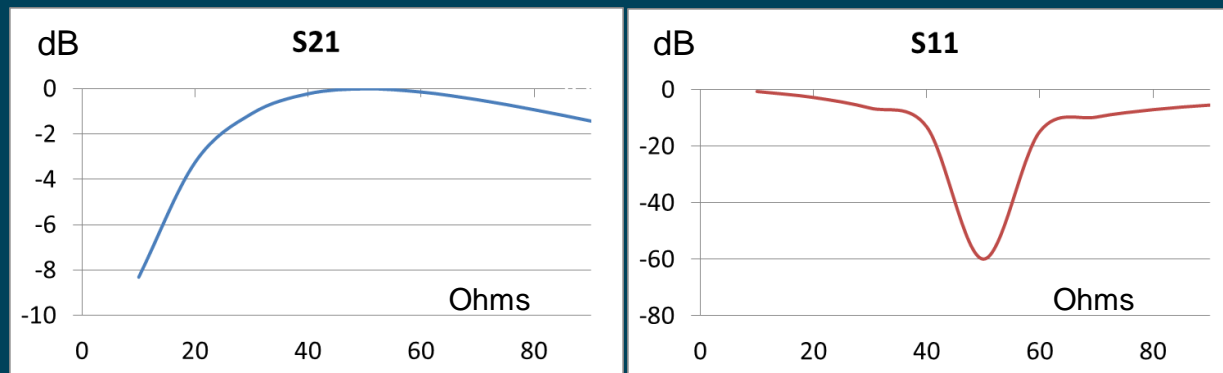
Line impedance impact



Optimal results are achieved for a near 50 Ohm design

Return loss

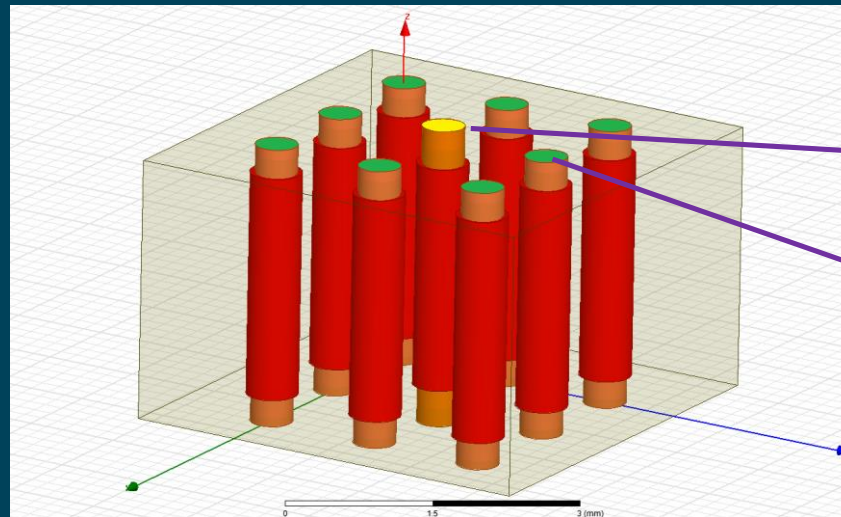
Line impedance impact



Peak insertion and return loss values as a function of line impedance

Basic simulation setup (3D HFSS models)

A 'field' configuration with grounded unused pins is chosen since that resembles applications



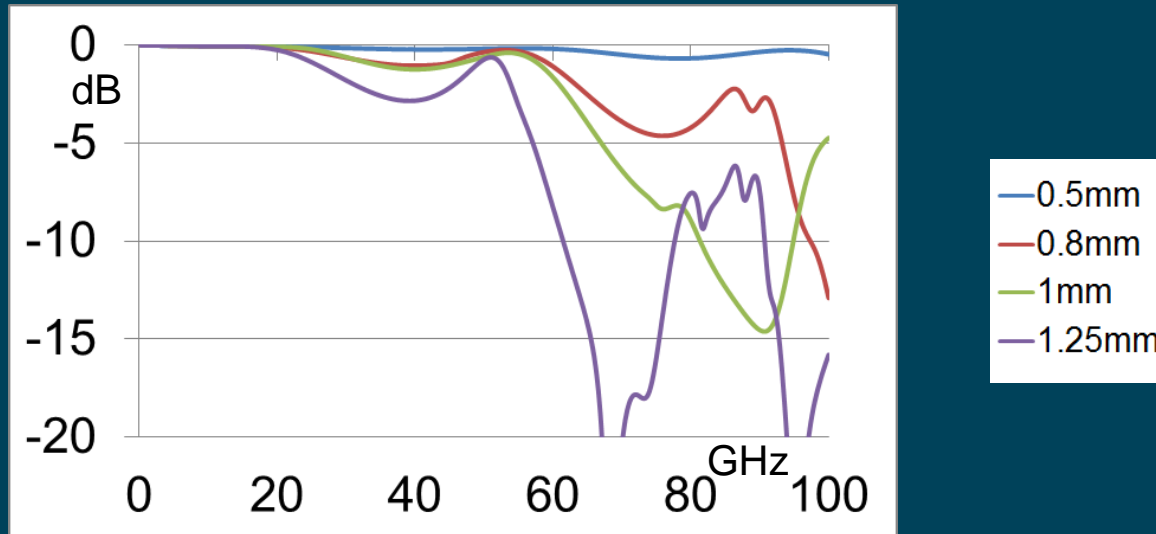
signal

ground

Simulation parameters and configurations oriented toward 'real-life'

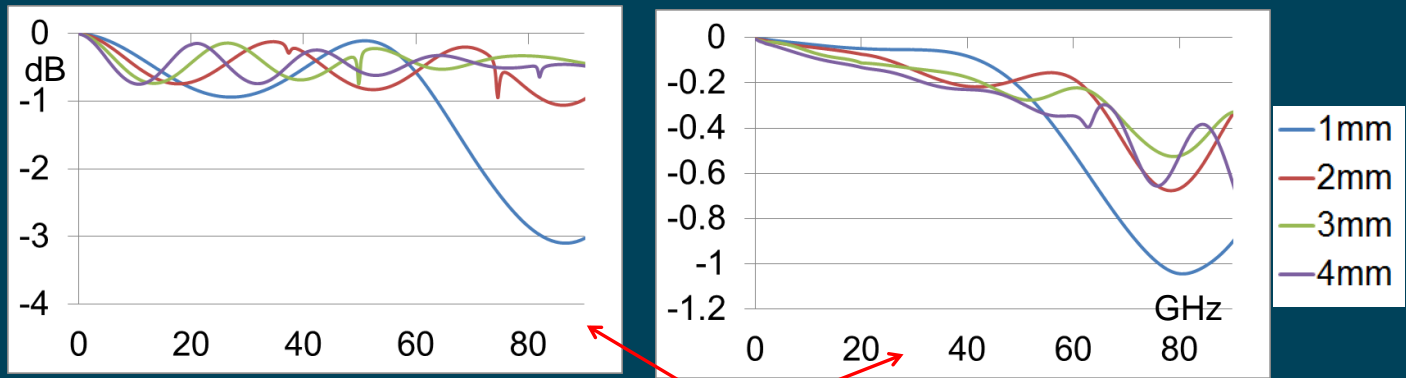
Pitch

A near 50 Ohm design was used in all cases



Insertion loss for different pitch arrangements

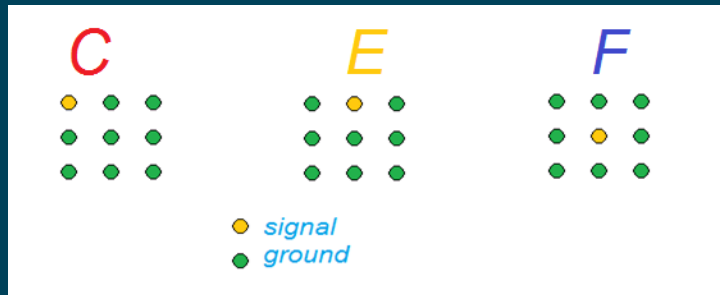
Line length impact



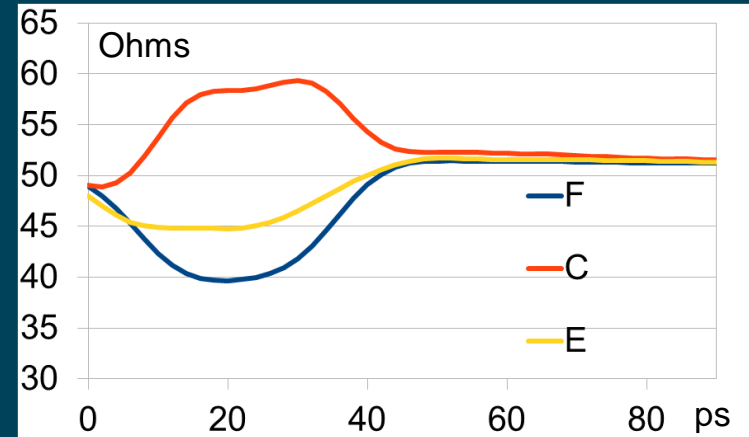
Line impedance was fixed at 35 and 48 Ohms

Insertion loss for different line lengths and impedance levels

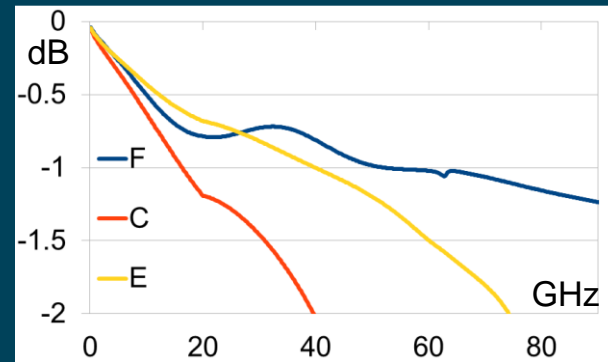
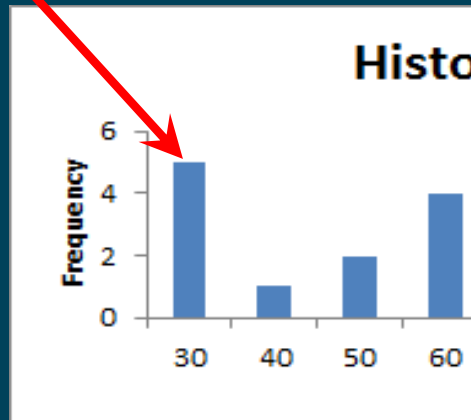
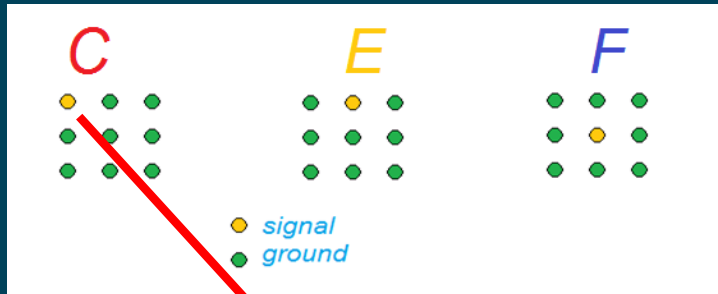
Signal and ground arrangement



Setup impact depends on which configuration gives closest Z to 50 Ohms



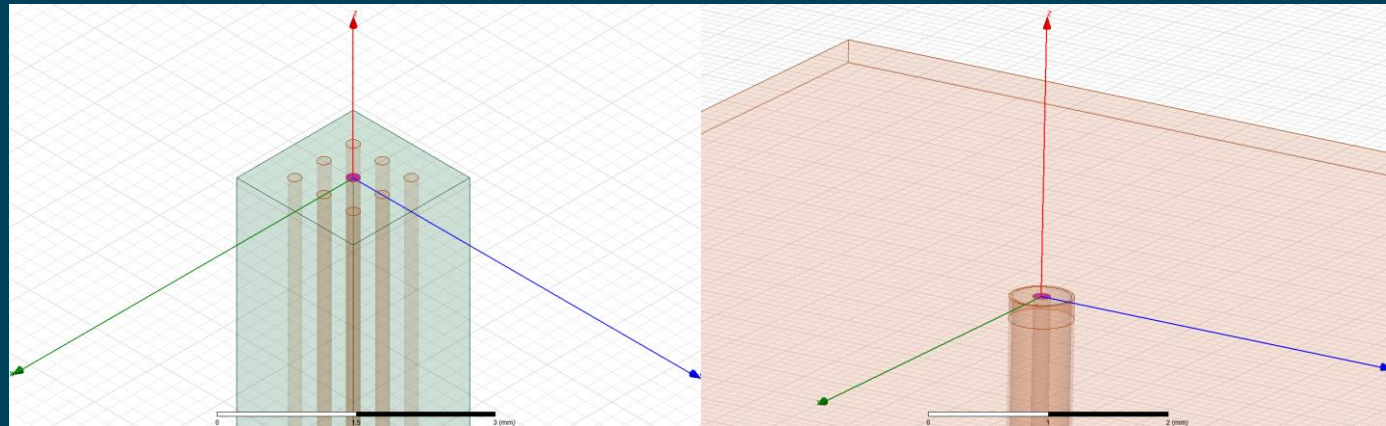
Signal and ground arrangement



Corner configuration often has lowest -1dB point

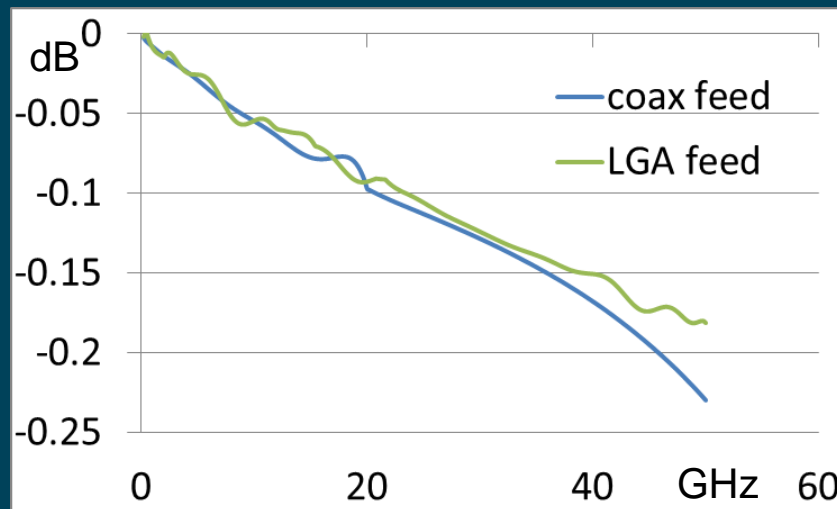
-1 dB insertion loss to 90 GHz ?

Models for different test configurations



LGA type feed will result in slightly different field configuration than coaxial feed

Test configuration

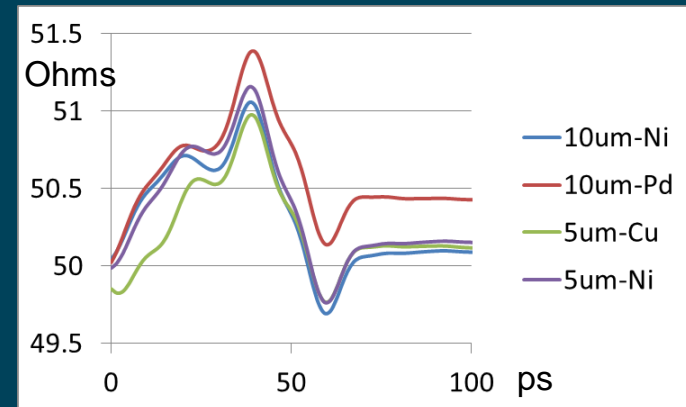
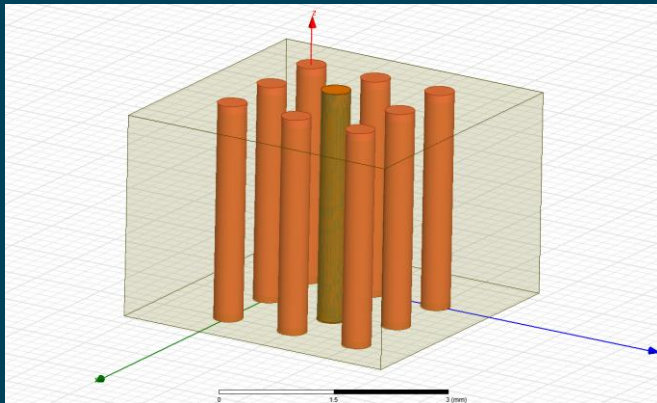


In this example there is relatively little difference in test results up to 40 GHz. This is not always the case.

Insertion loss difference example

Plating

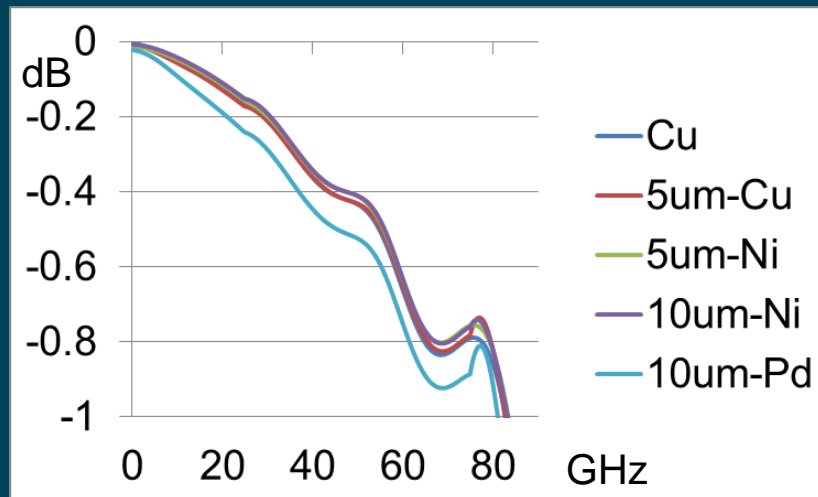
Simulation Setup:



Impedance as a function of time (i.e. distance)

Plating

Au was not included since it is generally very thin and thus somewhat "transparent"

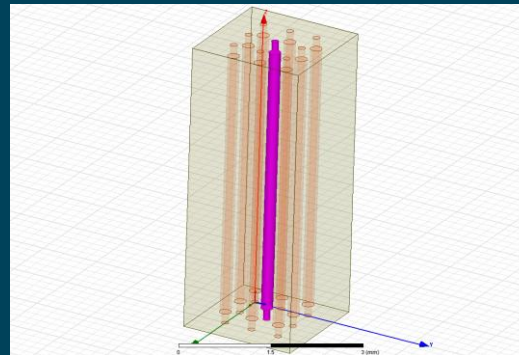


For this near 50 Ohm design plating does not contribute significantly to loss.

Insertion loss

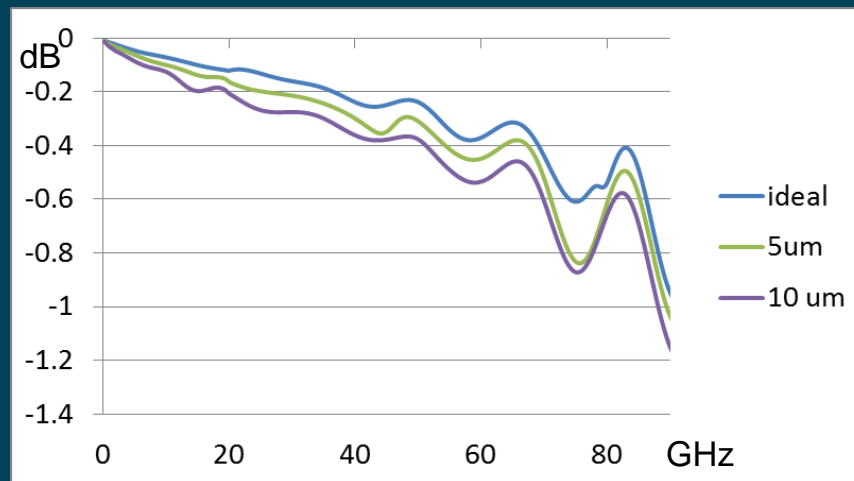
Roughness simulation

- Signal surrounded by ground assumed
- Only large diameter portion of pin was assigned a roughness



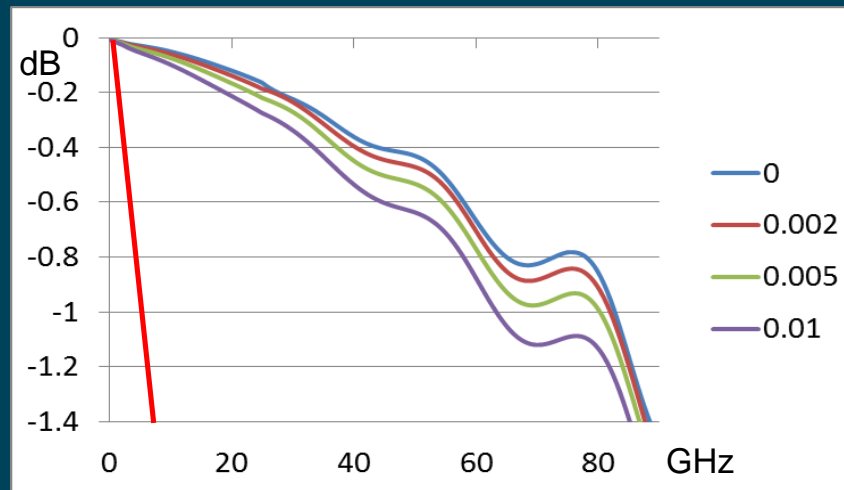
-1 dB insertion loss to 90 GHz ?

Roughness



Insertion loss as a function of frequency

Tangent Delta



Insertion loss as a function of loss tangent

Sensitivity of parameters

- Characteristic impedance is a major contributor to performance
- Pitch should be below 0.8 mm
- Line length can shift -1 dB point in frequency
- Roughness is not a major factor for short connections except for large variations
- Dielectric materials generally have only a small influence on performance
- Configuration for test and in application is important

Conclusion

- Socket design should place a focus on interconnect impedance
- End user needs to consider signal/ground configuration
- Materials selection can contribute to loss
- Dielectric materials need to be properly characterized for simulations