

BiTS 2017

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Reality Check - Validation & MEMS Test

Session 3

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 4:30 pm

Reality Check

"Augmenting form factor designs with validation and debug capability"

John Kelbert - Intel Corporation

"New Possiblity with Coax Via Risers"

Matthew Priolo, Adrian Rodriquez, Christopher Kinney, Adewale Oladeinde – Intel

"Processes for Validating and Maintaining Electrical DUT Interfaces"

Martin Gao, Carolina Lock - Texas Instruments



New Possibility with Coax Via Risers

Matthew Priolo, Christopher Kinney, Adewale Oladeinde, Adrian Rodriguez Intel Corporation



BiTS Workshop March 5 - 8, 2017



Session 3 Presentation 2

Contents

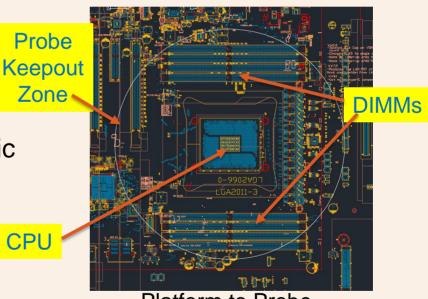
- Problem Statement
- Solution Space
- Proposed Strategy
- Simulation Results
 - Stacking Effect
 - SI / Power Impact
- Actual Solution

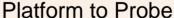


Problem Statement

- Enable Silicon Debug Team to probe the die.
 - The Probe Tools require 12" Diameter keepout (Cooling plate) which conflicts with components that are 35 mm tall.

- Previous Strategy
 - Special Skew Platform
 - More Resource / Logistic
 - Started After Power On







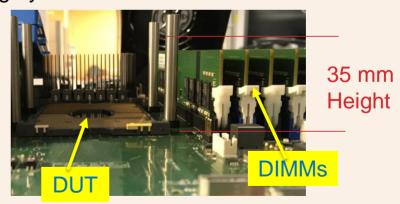
New Possibility With Coax Via Risers

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Reality Check - Validation & MEMS Test

Solution Space

- Requirement
 - Height > 35 mm
 - Withstand Thermal Cycling
 - Mechanical Rigid/Stable
 - Operate at Full Speed
 - Low Impact on Power Delivery
 - IR Drop
 - Low Impact on Signal Integrity
 - Controlled Impedance
 - Low Coupling





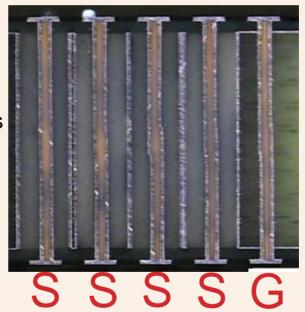
New Possibility With Coax Via Risers

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Reality Check - Validation & MEMS Test

Solution Strategy: Coax Via PCB Riser

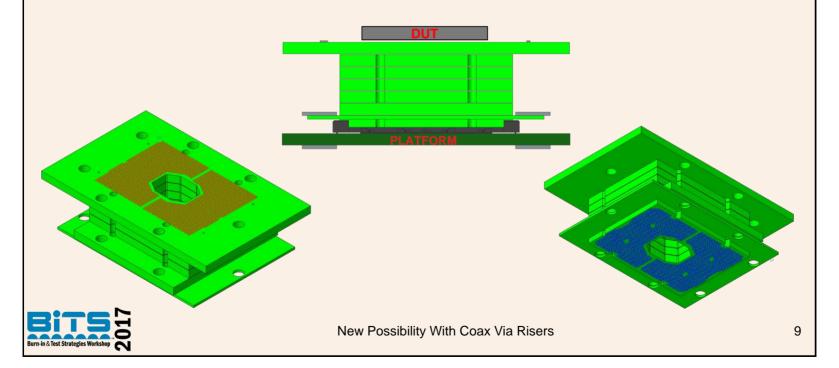
- Riser
 - PCB with Top and Bottom footprint map 1:1
 - Height Limitation related to aspect ratio
- Coax: Drill within a Drill
 - Buried Outer Via
 - Shorted to GND Plane / GND Pins
 - Inner Drill
 - Signal, Through hole



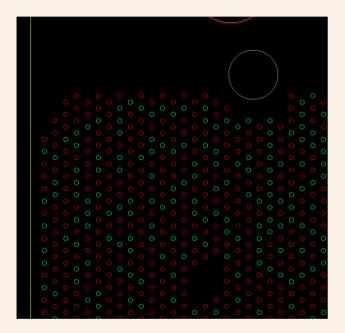


Proposed Solution

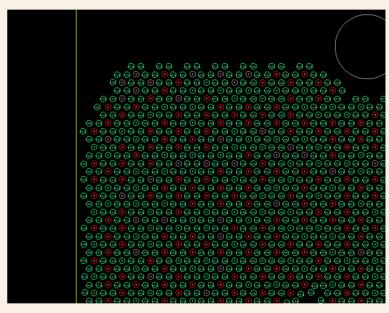
- (7) 5mm Stacked Coax Risers
- GND Grid Solder Ball Attached
- Additional Decoupling Capacitor on Top Riser



Proposed Solution: Ground Grid Solder Ball



DUT PINS



DUT PINS w/ Added Gnd Pads

(Connected to GND Layer by laser)



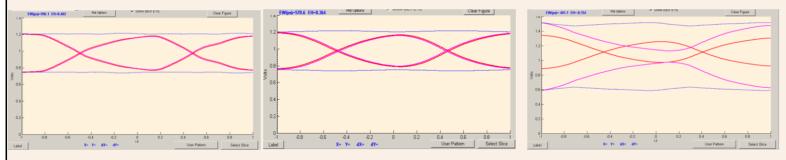
New Possibility With Coax Via Risers

Simulation: GND Grid Solderball Simulation of Grid Impact Signal Vias Interconnect 1-2 Ground Solder Balls Interconnect 2-3 XV Plot 5 0.00 Interconnect 3-4 NO GND SHIELDING -10.00 -20.00 GND SHIELDING 晉-30.00 ₩-40.00 Lower Value = Less Coupling -50.00 Coax Signal **GND Walls** -60.00 -70.00 0.00 2.50 10.00 Freq [GHz] 12.50 17.50 5.00 15.00 New Possibility With Coax Via Risers 11

Simulation: DDR@1600MTs

Results

| | No Riser | 35 mm Riser | 35 mm Riser (No Shielding) |
|----------------|----------|-------------|-----------------------------|
| EyeWidth (pS) | 596.1 | 570.6 | -401.1 |
| EyeHeight (mV) | 402 | 364 | -154 |



No Riser (Nominal) 35 mm Coax Riser 35 mm NonCoax Riser

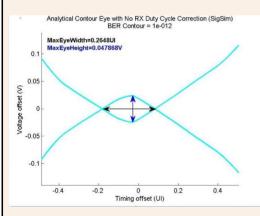


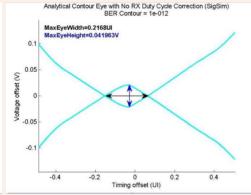
New Possibility With Coax Via Risers

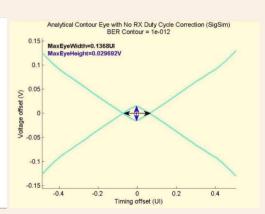
Simulation: PCle Gen3

Results

| | No Riser | 35 mm Riser | 35 mm Riser (No Shielding) |
|----------------|----------|-------------|-----------------------------|
| EyeWidth (UI) | 0.2648 | 0.2168 | 0.1368 |
| EyeHeight (mV) | 0.047868 | 0.041963 | 0.029692 |







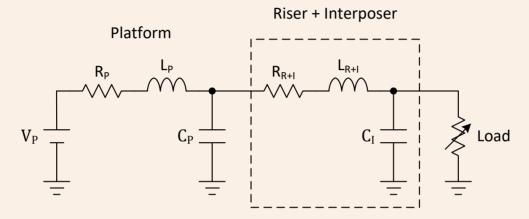
No Riser (Nominal) 35 mm Coax Riser 35 mm NonCoax Riser



New Possibility With Coax Via Risers

Simulation: Power Integrity

Basic Power Delivery Model



| Effect | Riser and interposer (R+I) add additional parasitic resistance and inductance |
|----------|---|
| Result | Reduces platform power delivery bandwidth. Impedance Profile will be higher (Z vs F). |
| Solution | Interposer load side capacitors (C _I) mitigate bandwidth degradation |



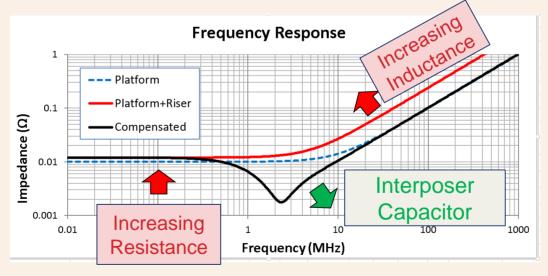
Simulation: Power Integrity

Inductance will increase, impacting Higher frequency response

$$L_{via} = 5.08h[\ln\frac{4h}{d} + 1]$$

$$L_{\text{COAX}} \approx \mu_o \mu_r / (2\pi) \, * \, \text{In(D/d)*} \, \, L$$

- Resistance will increase. Resistance = Resistivity*Length/Area
 - Inductance/Resistance is function of # of Pin Associated to power Rail.

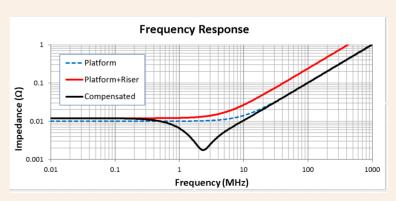




New Possibility With Coax Via Risers

Simulation: Power Integrity

- Higher Frequency
 - Primarily impacted by the Increased Inductance
 - Localized decoupling
 - 4 of capacitors on platform seemed to be a good starting point
- Lower Frequencies
 - Primarily impacted by the Increased Resistance
 - Bulk Capacitors
 - Remote Sensing





New Possibility With Coax Via Risers

Final Solution: Views

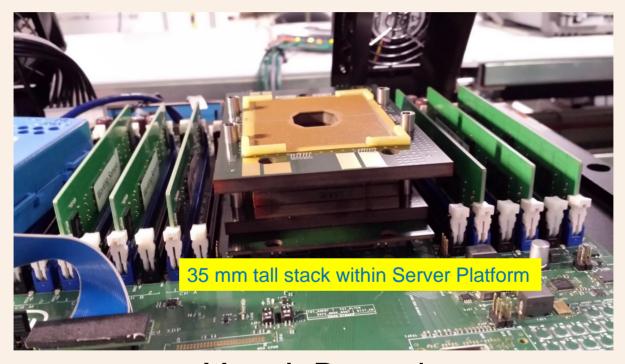






New Possibility With Coax Via Risers

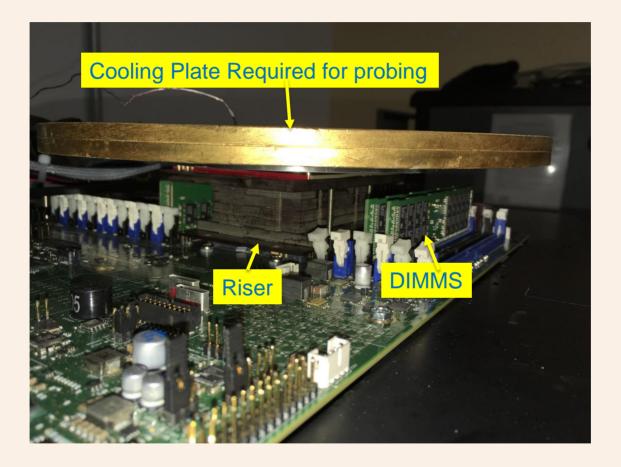
Final Solution: Platform



Yes, It Booted



Final Solution: Platform





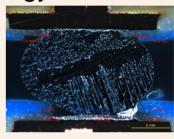
Final Solution: Testing

- Signal Integrity
 - Boots & all interfaces are functional
 - DDR Evaluated at 2666 MTs
 - Riser Impact of 66pS/70 mV (biggest single bit difference)
- Power Integrity
 - Testing Adding and Removing caps
 - Inconclusive, we have a feeling something else might be impacting behavior (BIOS / Training)



Final Solution: Challenges Faced

- Assembly Testability
 - Short / Open / Continuity Testing Methodology
 - SM Issues Too thick



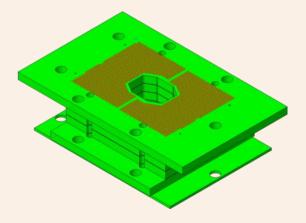
- Fab
 - Had Early Delamination Material Change
 - Coax Shorting Fab process change





Summary

- The Proposed Solution
 - Reduced the need for a special platform skew
 - Minimized the Z axis coupling
 - Created a controlled impedance environment
 - Provided necessary Z height to rise above keepout zones





New Possibility With Coax Via Risers

Session 3 Presentation 2

Summary

- Coax Risers Enables
 - New Test / Observation Strategies
 - Move Coverage
 - Platform Configuration
 - "Any Platform" Debug
 - Available at Power On
 - "Sky's the Limits" Solution ©
- Complements BiTS2017 Presentation
 - "Augmenting Form Factor Designs with Validation and Debug Capability"
 - Interposers will become more robust

