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## Design method to endure the stress by high spring pin counts on the wafer test

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### Introduction

#### BACKGROUND

- Probe Card connects physically and electrically between Automatic Test Equipment (ATE) and Device Under Test (DUT) in wafer test.
- High parallelism probe card as low cost test solution [1-2]
  - about 1,536 parallelism for one touch down test per wafer
  - up to about 100,000 probe pins & about 50,000 pogo pins
- High risk of the crack or break in ceramic due to the increased stress by the huge number of probe/pogo pins
- In this work, we present the endurable ceramic design which is strong against the compression stress and the thermal deformation.

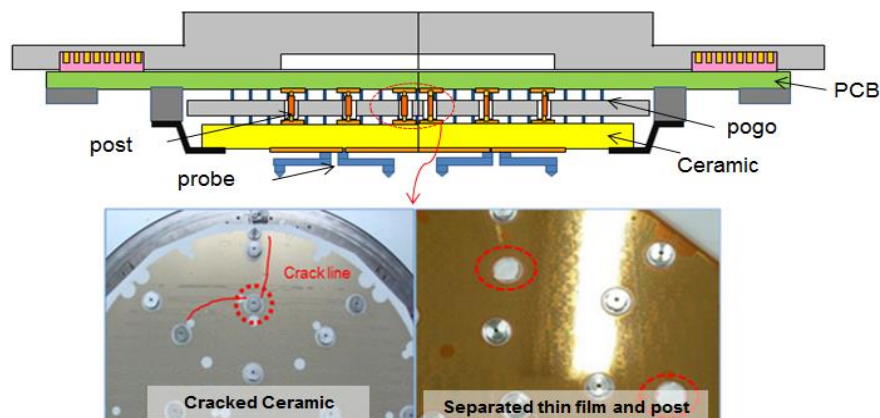


Fig. 1. Structure of Probe Card and Ceramic damage

## Endurable Ceramic Designs

### Design I. Low force solutions for ceramic crack.

- Compression stress to ceramic
  - Top side by pogo pins & overdrive
  - Bottom side by probe pins & overdrive

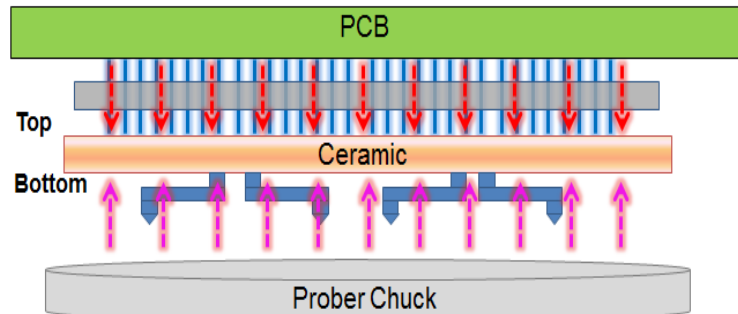


Fig. 2. Stress to ceramic of high parallelism probe card

- Low force pogo pins and probes to decrease the compression stress

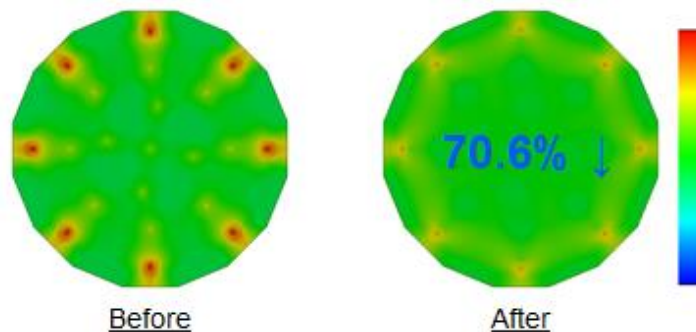


Fig. 3. Stress simulation by low force probe (40% less, normalized)

### Design II. CTE mismatch between ceramic and ceramic post

- Ceramic post for probe card assembly with PCB.
- Thermal stress due to CTE mismatch between ceramic and ceramic post during hot (+95°C) and cold (-40°C) wafer test
- Proper material selection for CTE of ceramic post against CTE of ceramic.

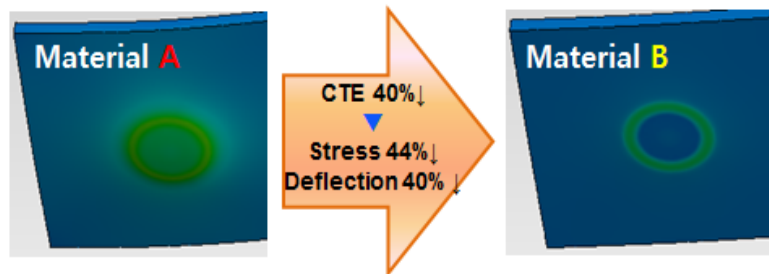


Fig. 4. Simulation of the materials of ceramic post of probe card

## Conclusion

- High parallelism probe card → Higher stress to ceramic
- Two design factors for enduring ceramic against stress
  - Low force pogo pins and probes for ceramic crack failures
  - Improvement CTE mismatches for ceramic post break failures
- Ceramic damage dramatically decreased through the proposed enduring ceramic design.

### Count of Ceramic damage

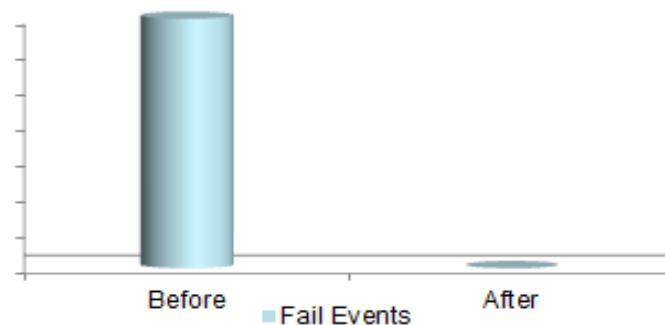


Fig. 5. Count of ceramic damage: Before vs. After

## References

- [1] The International Technology Roadmap for Semiconductors: Test and Test Equipment Section.
- [2] G. Kim, W. Nah, "NAC Measurement Technique on High Parallelism Probe card with Protection Resistors", *Journal of Semiconductor Technology and Science*, vol.16, no.5, 2016