

AWARD WINNING PERFORMANCE

High performance devices call for high performance test and burn-in solutions and require participation by the entire test ecosystem including contactors, sockets, the DUT board, along with the environment that testing takes place in and the methodology applied. This session provides insight to each step beginning with the development of a statistical model to identify the optimized bandwidth for spring probes. Next up is a look at environmental factors that can readily impact socket performance and thus indirectly test yield. The third presentation verifies test methodology to troubleshoot a device that is having issues in a very high performance test contactor to determine the cause of the issues and affect changes to prevent them from reoccurring. Lastly, we'll hear about the unique challenges to create an optimized test methodology for 25 to 40 GHz RF amplifiers, mixers, and down converters in LFCSP (QFN) and WLCSP packages, considering connectivity issues between DUT board and sockets.

Design of Experiments Using Spring Probe Parameters for Optimized Socket Bandwidth

Mike Fedde, Ila Pal—Ironwood Electronics, Inc.

Socket Performance vs. Environmental Conditions

Gert Hohenwarter—GateWave Northern, Inc.

Troubleshooting Test Oscillation Problems

Jeff Sherry—Johnstech International Corporation

Optimization of Package, Socket and PC Board for 25 to 40GHz RF Devices

Carol McCuen, Phil Warwick—R&D Circuits, Inc.



This Paper

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Optimization of Package, Socket and PC Board for 25 to 40GHz RF Devices

Carol McCuen and Phil Warwick
R & D Circuits



2013 BiTS Workshop
March 3 - 6, 2013



Using simulation to understand and improve Socket and PCB performance

- HFSS, the 3D full-wave electromagnetic field simulator is used to predict performance and learn the effect of changes.
- ADS, EDA software for RF, Microwave and High speed digital application is used to create equivalent circuit to match the measurement data, .s2p file. Also, eye diagrams and deembedding can be done with ADS.

Case study- QFN20 Elastech socket 25 GHz application

- Measured QFN20 Elastech socket, 650 um pitch, mounted on customer circuit board using VNA, swept to 30 GHz.
- IC side was probed using Cascade Microtech FPC probe with test insert and the other port was coaxial.
- There was an unexpected increase in the Insertion Loss at 25 GHz, to -10 dB. Return Loss was bad as well, -5 dB.
- Want to have good performance to 30 GHz.
- The steps taken to find and fix the problem follow.

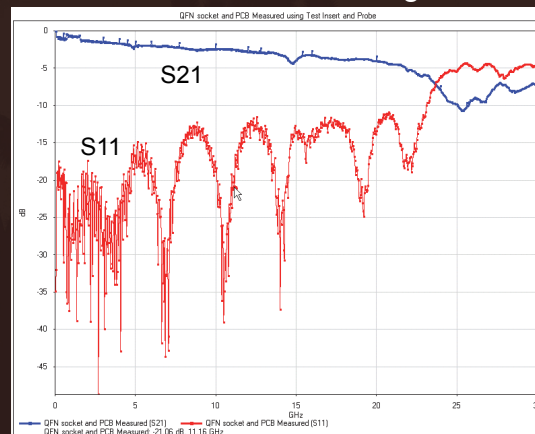
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Measurement results

QFN socket and PCB measurement using Test Insert and Probe



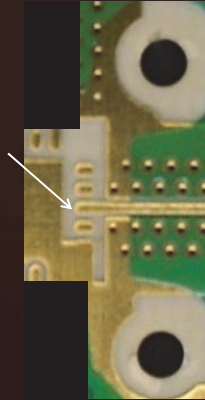
S21 – Blue
S11 – Red

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Customer Circuit Board Improvements



- Notice the lack of grounding around the high frequency pin on the IC.
- Top circuit pattern ground fill could be increased.
- This ground fill would connect the two adjacent Ground pins on the IC and the Ground plate on the bottom side of the IC.

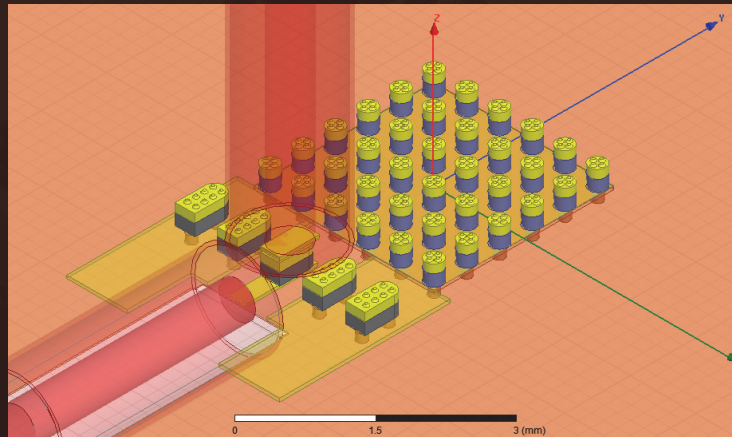
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Socket Model and PCB with more top layer ground fill

Perfect coax was used for input and output ports



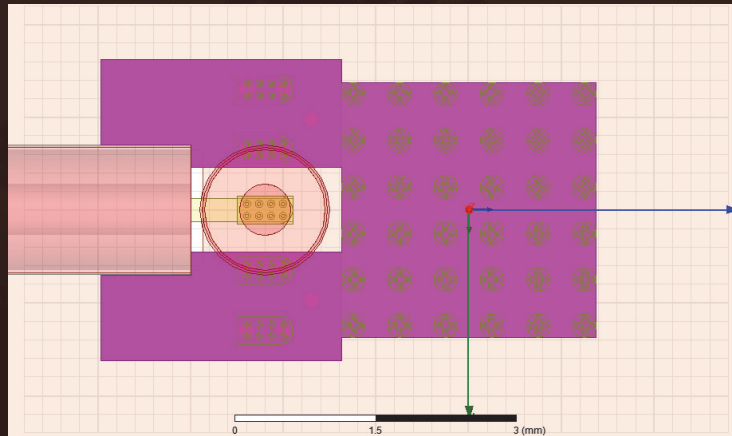
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Model of PCB with more top layer ground fill

Pink highlight is on the top layer



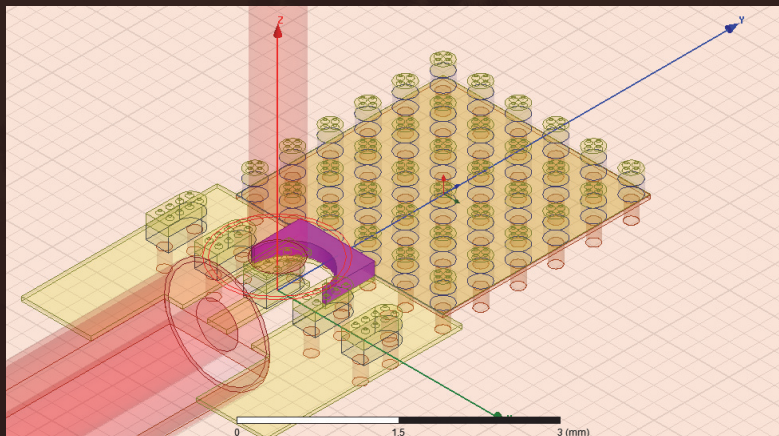
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Add ground wrap for additional analysis

- Flexibility in designing the shape of the elastomer contact,
- Join two ground pins in the GSG pattern together with an arch shaped elastomer to improve the horizontal to vertical transition.



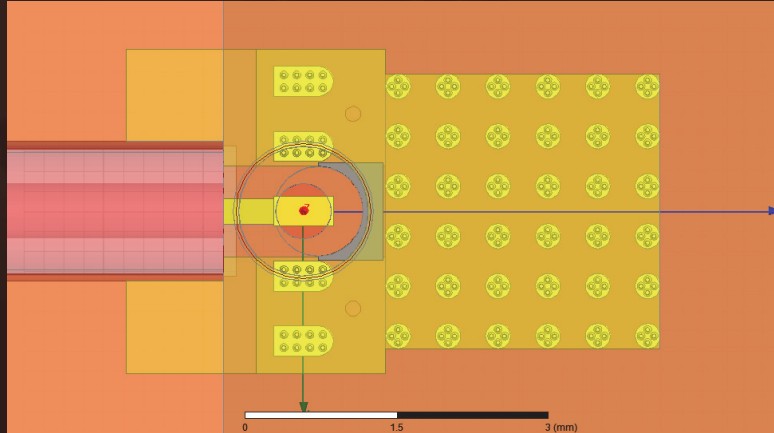
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Top View of model with ground wrap (blue).

- The inner edge of the elastomer is lined up with edge of ground fill.
- Two contacts on either side of signal contact are grounded.



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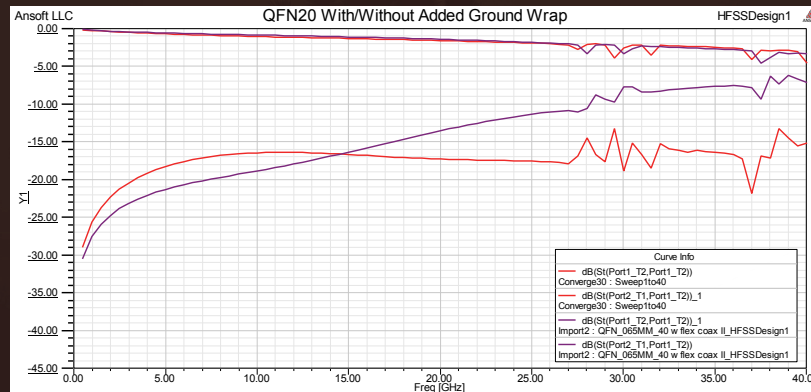
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Results for adding more ground plane top layer

Red Traces, S11 and S21 - More grounding Plus added Ground Wrap.

Blue Traces, S11 and S21 - More grounding top layer circuit



The problem at 25 GHz is nearly gone.
 High Frequency Improvement in S11 with ground wrap.

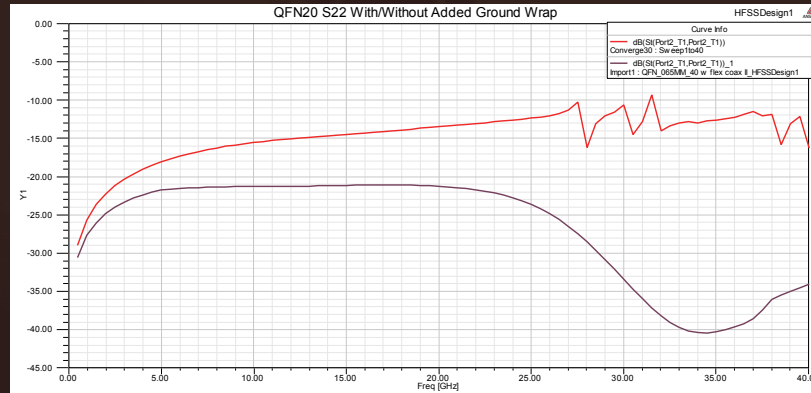
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Surprising results on Port 2, vertical coax.

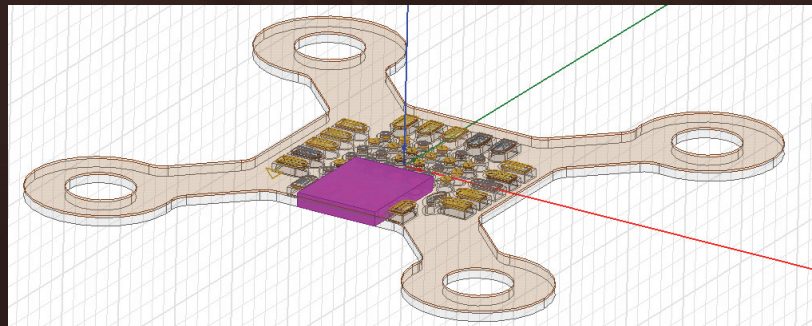
Red Traces, S22 - More grounding and added Ground Wrap.
 Blue Traces, S22 - More grounding top layer circuit



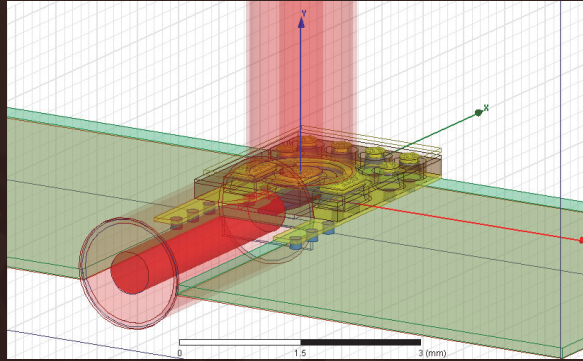
S22 is made worse with the addition of the Ground Wrap.

**Further Design Validation
 Mechanical Designer creates Solid Works model.**

A section around RF_IN pin of the IC was cut out of the Interposer section of the Elastomer socket to be used in the HFSS Simulation.



New HFSS design with mechanical model, note the higher level of detail.



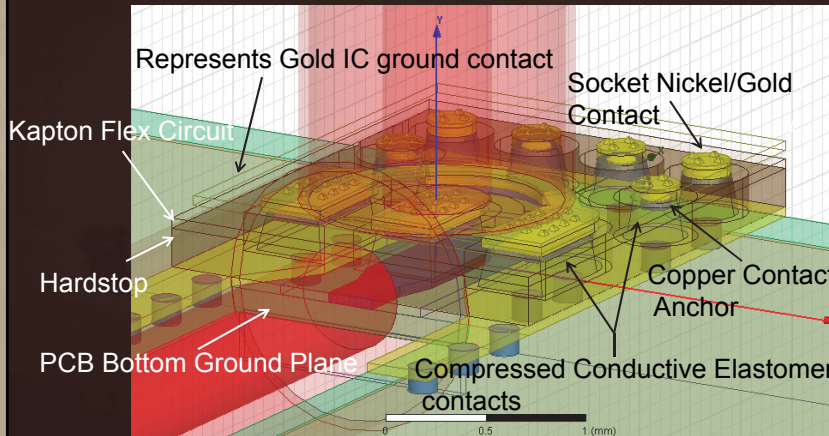
- Perfect 50 Ohm coaxes for waveports in driven terminal design.
- A Rogers RO4003 PCB with just two circuit layers:
 1. the top was gold around the elastomer and connecting to the Port1 coax (horizontal),
 2. the bottom was copper from edge to edge.

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New HFSS design with mechanical model
 Interposer details



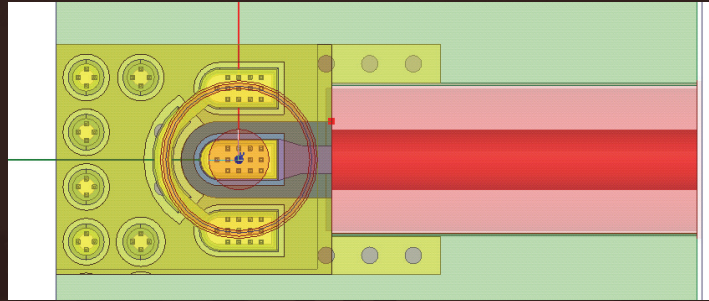
The greater complexity in the model will increase the simulation time.

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Top view of the 0.35 mm radius Ground Wrap design.



- top ground layer cut away 0.7 mm wide.
- same procedure for each radius design.
- The circle centered on the signal contact in the center is the outer conductor of the Port 2 coax (vertical).
- The grey vias connect the ground portion of top layer to the bottom layer copper. There are vias that can't be seen below the round elastomer contacts

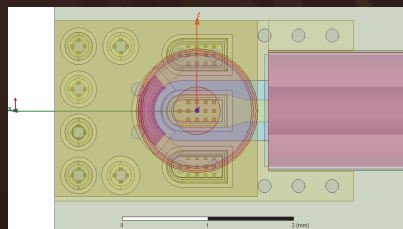
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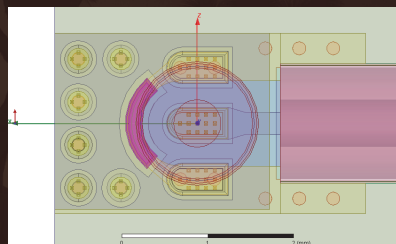
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Models for various radii
 created and simulated

Ground Wraps were
 350 um to 550 um



350 um radius



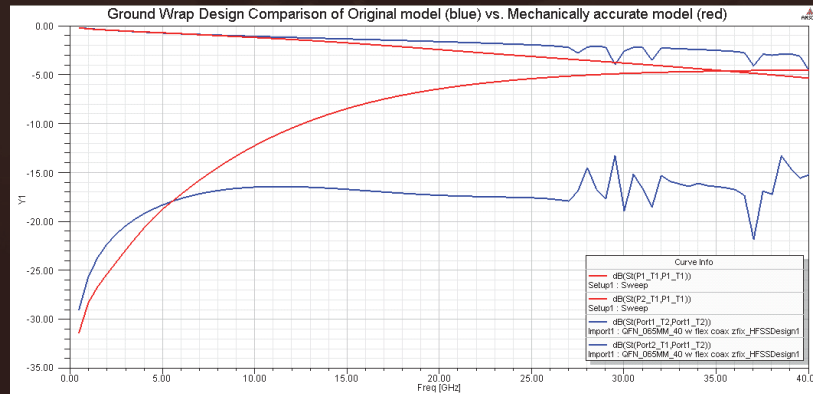
500 um radius

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Ground Wrap design Comparison-
 The results from the 350 um radius new model did
 NOT match the improvement we got in last model.
 WHY? Different size ground wrap & more complex interposer
 model.

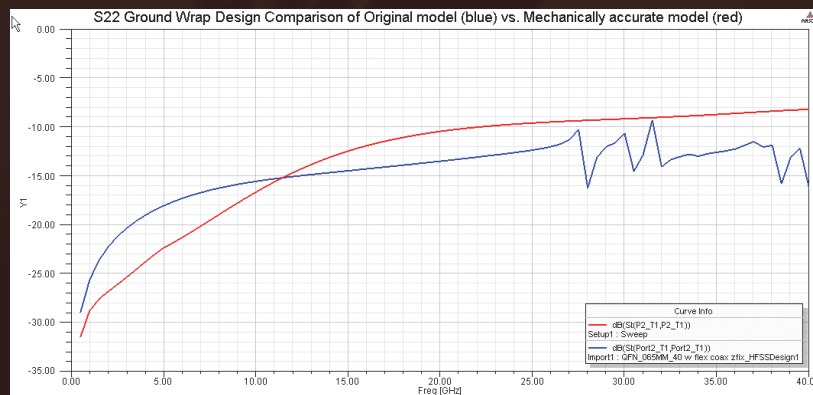


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Additionally, the S22 results for the 350 um radius
 new mechanical model improved only below
 11 GHz over the original model.
 Output Return Loss (S22)



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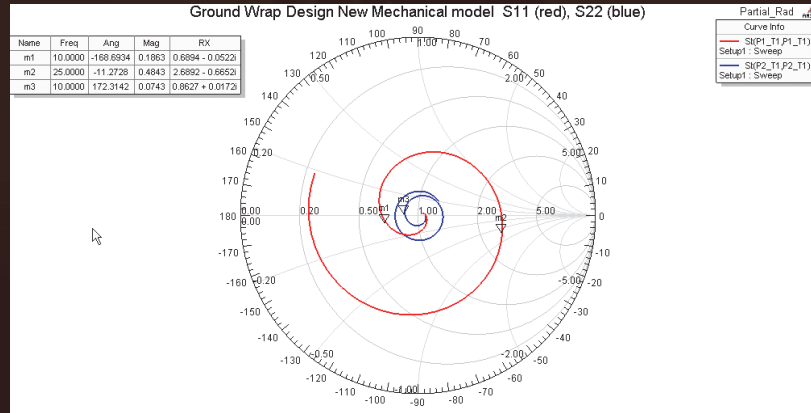
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The Smith Chart plot of the input and output return loss.

What can we do to improve the input Return Loss?

Use Lumped Circuit modeling.



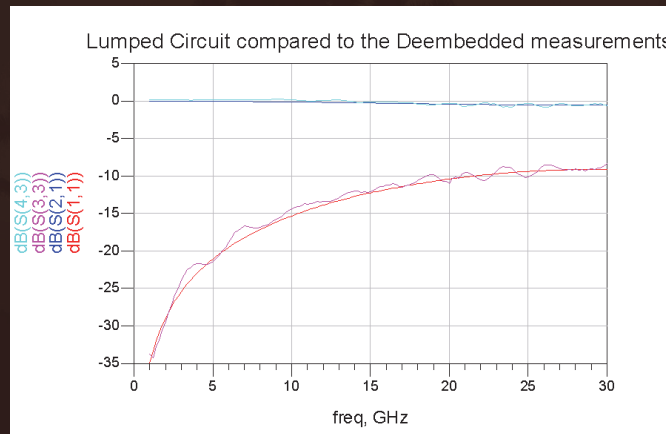
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Conductive Elastomer Characterization Circuit

Curve-fit lumped circuit to Deembedded measurement



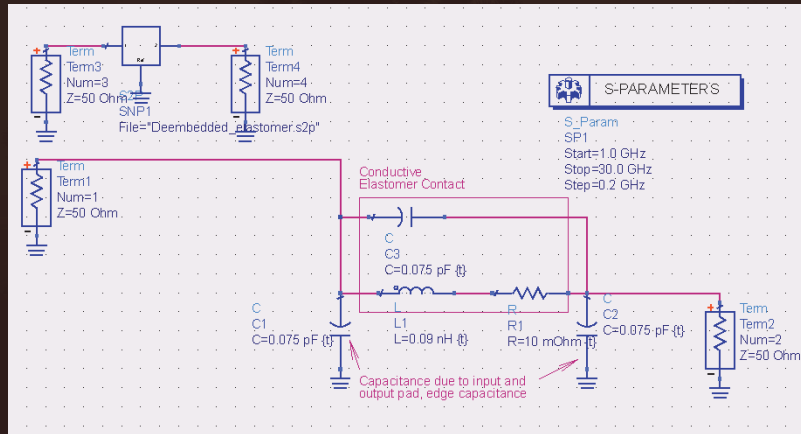
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Conductive Elastomer Characterization Circuit

- inductance based on GS short circuit RF lab measurement
- contact resistance based on DC testing

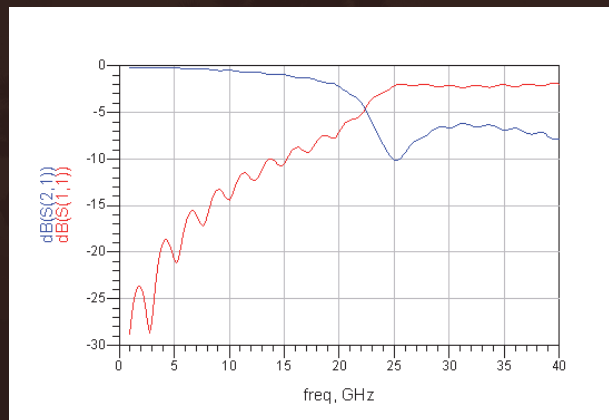


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Circuit model of Measurement Response to 40 GHz

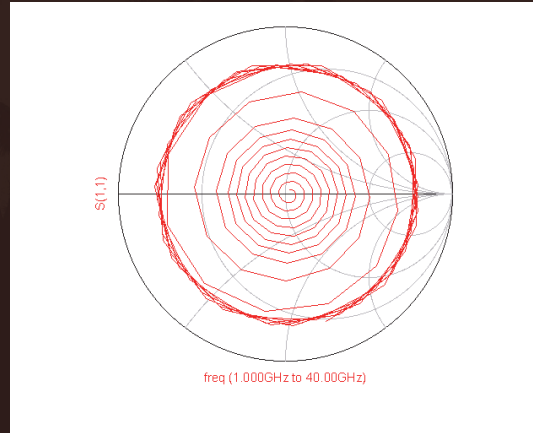


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Circuit model of Measurement S11 Response to 40 GHz



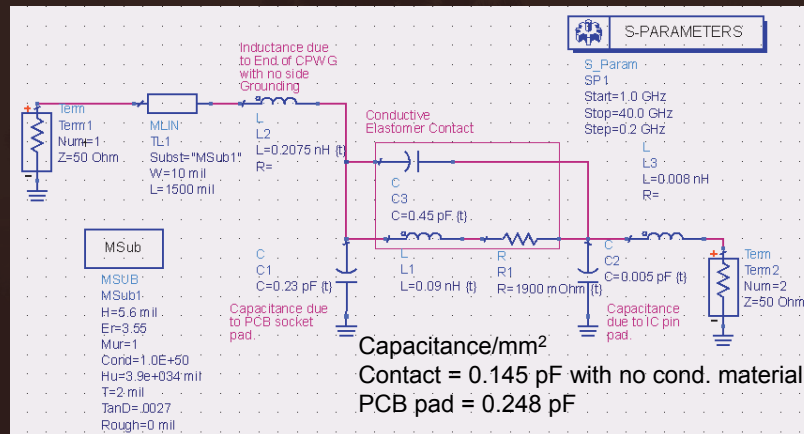
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Circuit Model of the measurement

Poor contact compression results in high contact resistance and higher capacitance than expected.

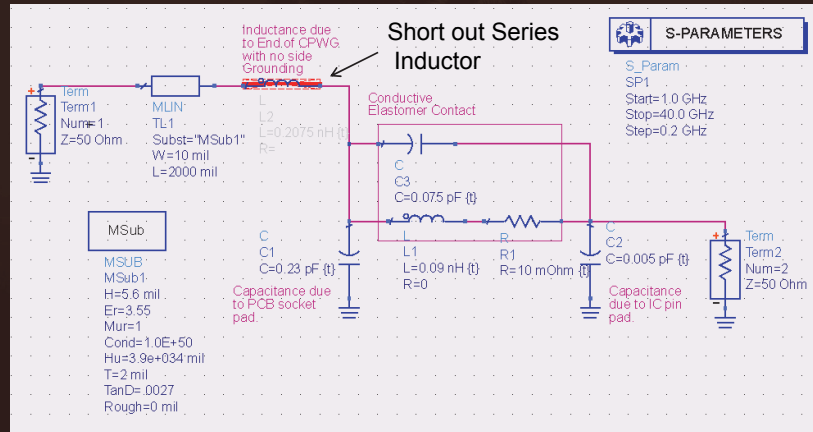


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Put the series L-R and parallel C from the Curve-fit Characterization into this Measurement circuit.

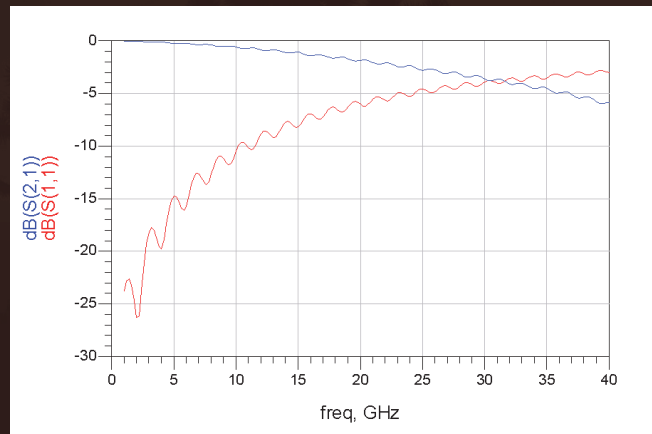


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Put the series L-R and parallel C from the Curve-fit circuit into this Measurement circuit
 This Response is very close to the results in the HFSS Mechanical Model.

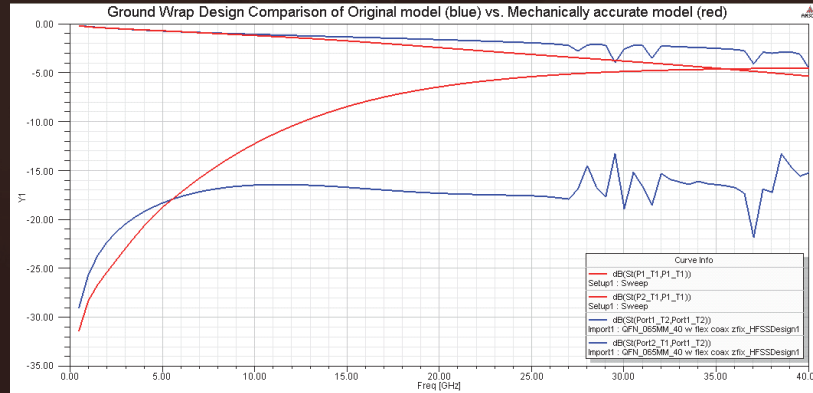


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Red Trace - Mechanical Model with Ground Wrap

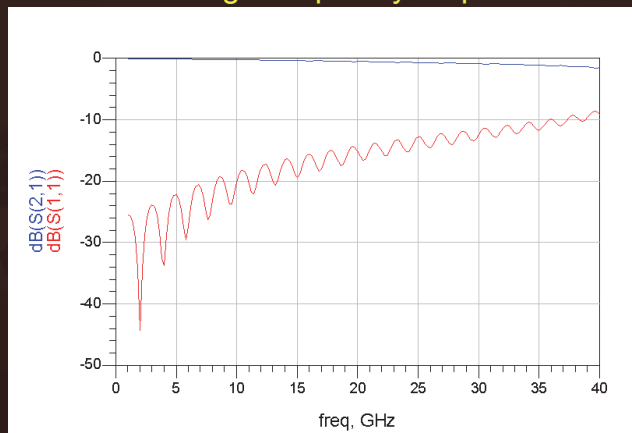


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Reduce the PCB pad capacitance, C1, from 0.23 to 0.09 pF and keep C3 at 0.075 pF gives a better high frequency response.



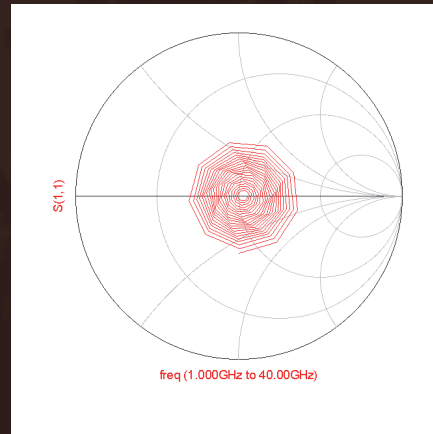
So the idea of reducing the capacitance at the contact area was pursued by removing the ground plane below the microstrip-to-contact transition.

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Reduce the PCB pad capacitance, C1, from 0.23 to 0.09 pF and keep C3 at 0.075 pF gives a better high frequency response.

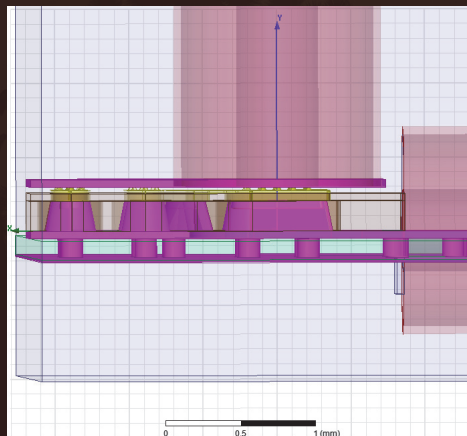


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Side view of the Ground conductors in the HFSS simulation model.

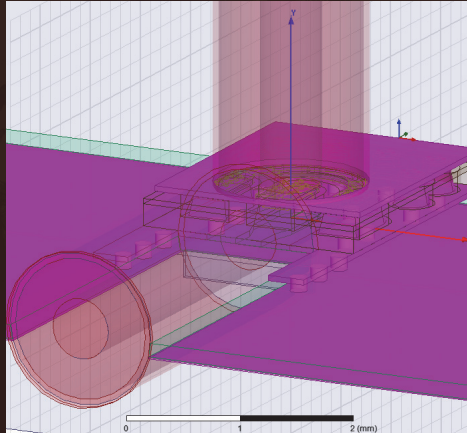


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The Ground Plane on the bottom of the PCB is not removed.

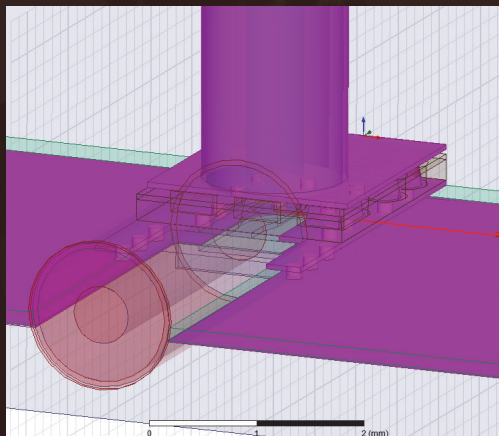


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See the hole in the ground plane on the bottom of the PCB.

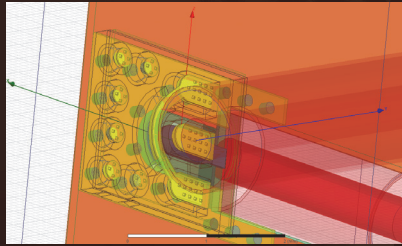


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Ground Plane Removal Study for 350 um



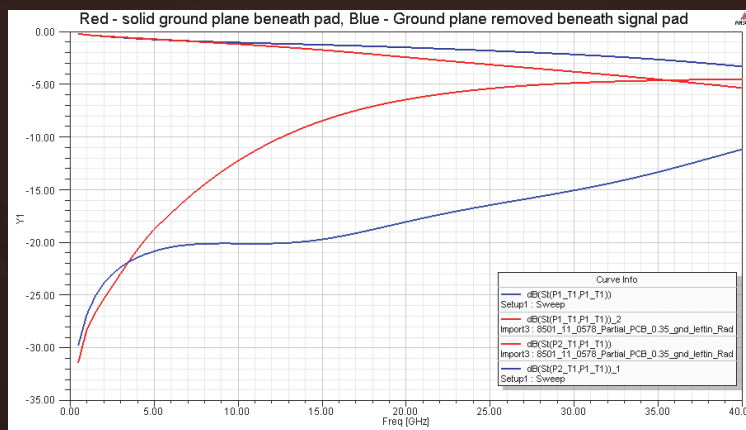
- The removal of the PCB ground plane had a direct affect on the Port 1 return Loss.
- This has also caused a big change in the Port 2 Return Loss.

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Improvement in the Insertion Loss and Port 1 Return Loss when PCB ground plane is removed (blue).



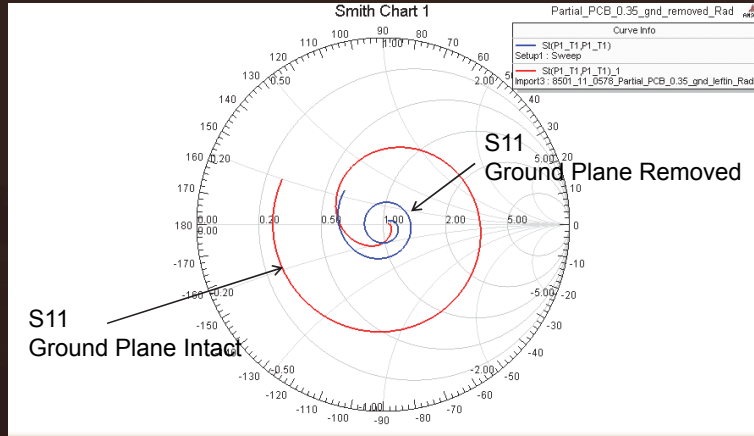
The result was to create a beneficial resonance at ~15 GHz.

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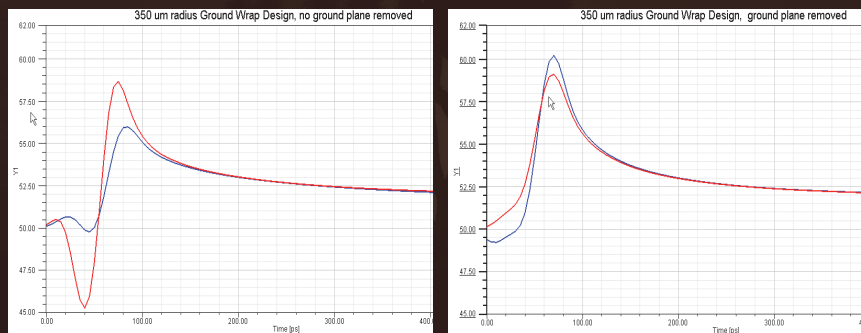
Smith Chart shows improvement in Port 1 Return Loss when PCB ground plane is removed (blue).



Looks similar to ADS circuit analysis results when the C1 capacitance is reduced.

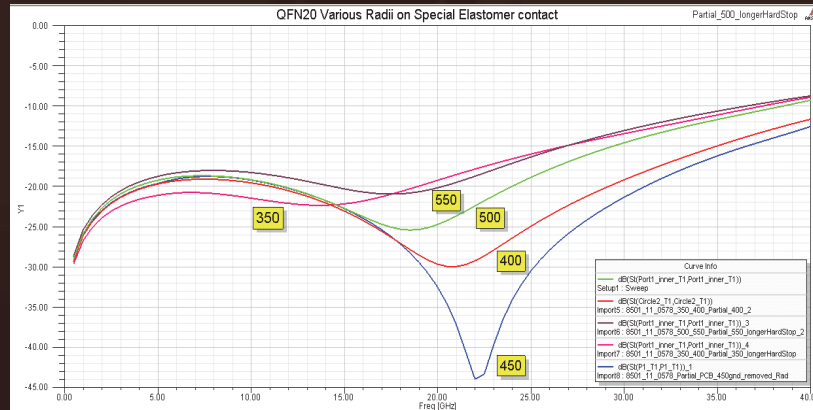
TDR of P1 (red) and P2 (blue) with and without the ground plane removed below the signal contact.

No Ground Plane removed Ground Plane removed



Improvement in the Port 1 Return Loss when PCB ground plane is removed.

Results for various Radii - 350 um to 550 um
Resonance shifts in frequency with different radii.



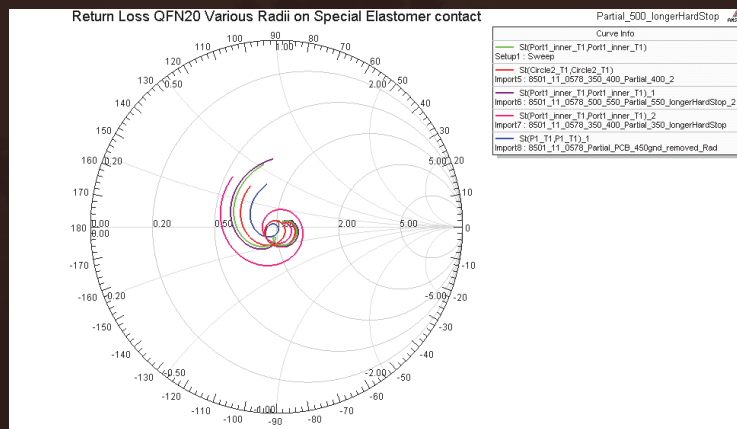
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Smith Chart Port 1 Return Loss when PCB ground plane is removed.

Results for various Radii - 350 um to 550 um

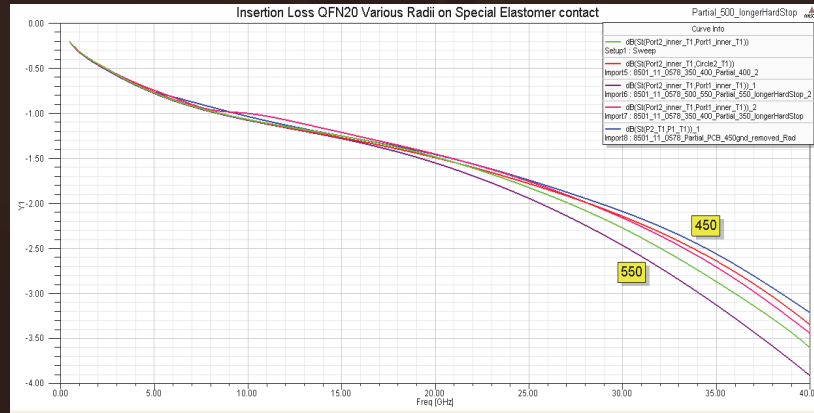


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Insertion Loss of Various Radii when PCB ground plane is Removed

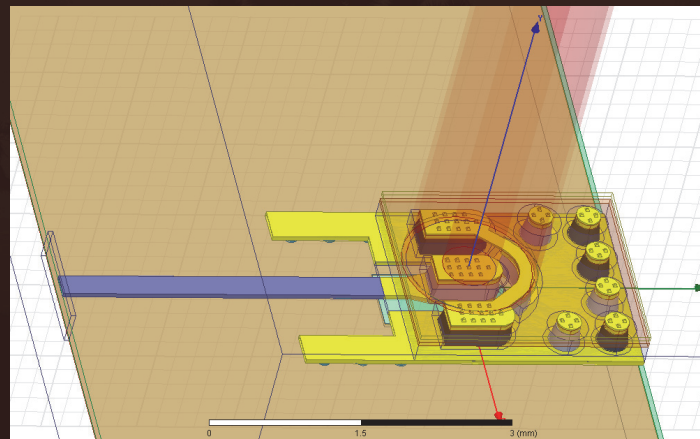


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To complete study, change model from a perfect coax to a microstrip input.

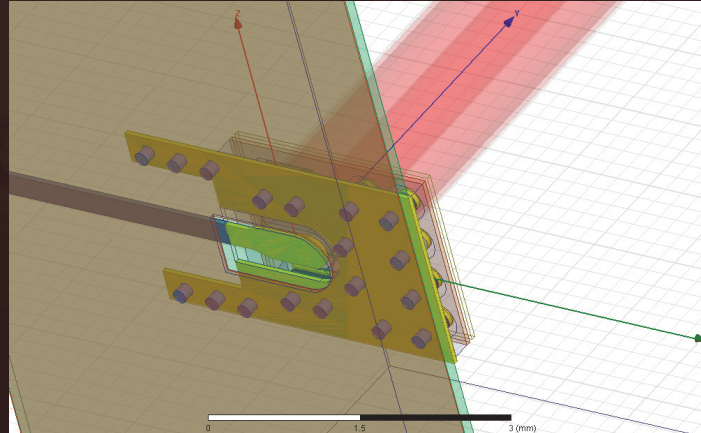


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Change model to a microstrip input, keep the ground plane removal.



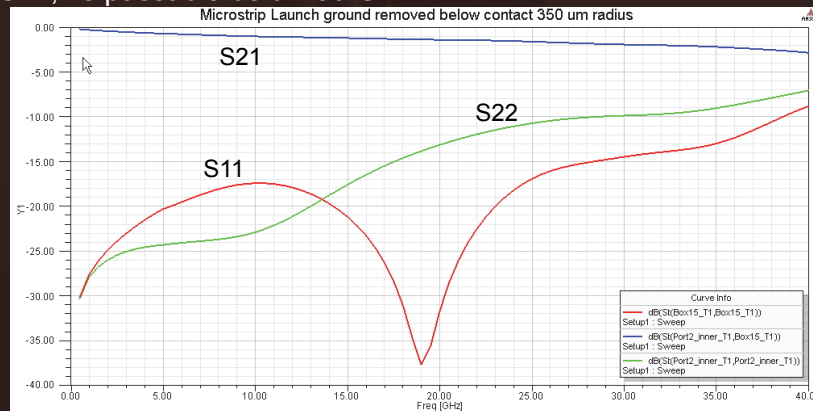
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Results for microstrip input model

- The results are very close to the model using the perfect coax
- S21 and S11 have improved by the same amount, Resonance is 3 GHz lower
- S22, is passable below 30 GHz.



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Conclusion - Use Ground Wrap and Ground plane removal depending on the type of signal using the pin.

Use

- When the IC pin is an Input signal, i.e. RFin for an amplifier.

Don't Use

- When the IC pin is an Output signal, i.e. TX out.

For this example the return loss, S22, at 25 GHz on the IC side was -18 dB without the ground wrap and removal and -11 dB with the ground wrap and removal.

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Contributions/ Acknowledgements

- Brian Groeger, Senior Applications and Development Engineer
- Rodney Ames, Primary Product Design Engineer
- HFSS is a product of ANSYS.
- Advanced Design System, ADS, is a product of Agilent Technologies.

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