BiTS Burn-in & Test Socket Workshop 2010

Session 5

# ARCHIVE 2010

## TECHNIQUES, COMPONENTS & ADVANCES FOR NEXT GENERATION TEST

### Next Generation CiS (Capacitor in Socket) Featuring Discrete Capacitors and Elastomer Hybrid Schemes

Shaul Lupo, Omer Vikinski—Intel Corporation
David Bogardus, Khaled Elmadbouly, Cody Jacob—Interconnect Devices Inc.

### Multi Level Stacked Socket - Challenges & Solutions

Mike Fedde, Ranjit Patil, Ila Pal, Vinayak Panavala—Ironwood Electronics

### Advances in WSP - Wafer Socket Pogo-Pin Probing

Norman Armendariz, James Tong—Texas Instruments

### Answering the Call

Thomas N. Bresnan—R&D Circuits

# Next Generation CiS (Capacitor in Socket) Featuring Discrete Capacitors and Elastomer Hybrid Schemes

**Shaul Lupo, Omer Vikinski**
Intel
**David Bogardus, Khaled Elmadbouly, Cody Jacob**
Interconnect Devices, Inc.

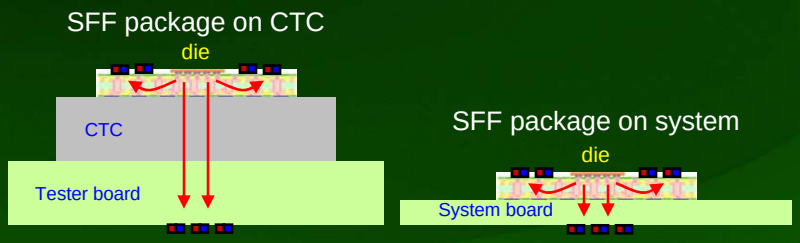
2010 BiTS Workshop
March 7 - 10, 2010

## CiS Development

- Background
- First Gen (1G) Solution
- Second Gen (2G) Solution
- dCiS + Elastomer Socket Advantages Upon Previous CiS Solution

# Background

- CiS (Capacitor in Socket), presented in ITC 2008
- Tester power delivery in high frequencies (>1MHz) is worse by definition versus system for SFF packages

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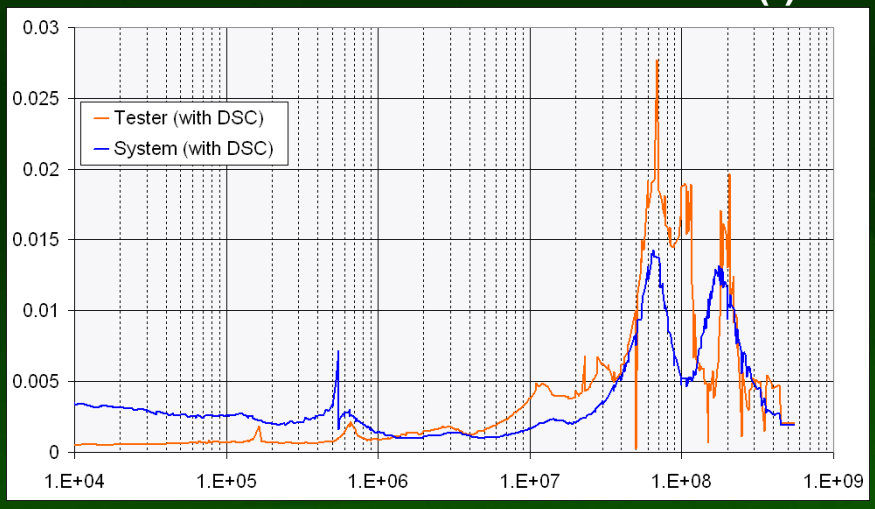
# Background

## Dual Core Processor SFF IFDIM Z(f)

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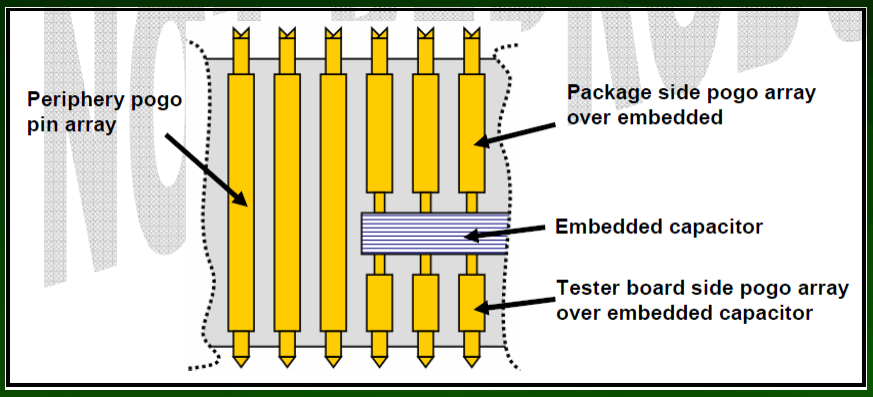
## CiS Solution Approach

- Embedded array capacitor in the test-socket used to reverse this equation.
- Including 3 types of pogo pins.

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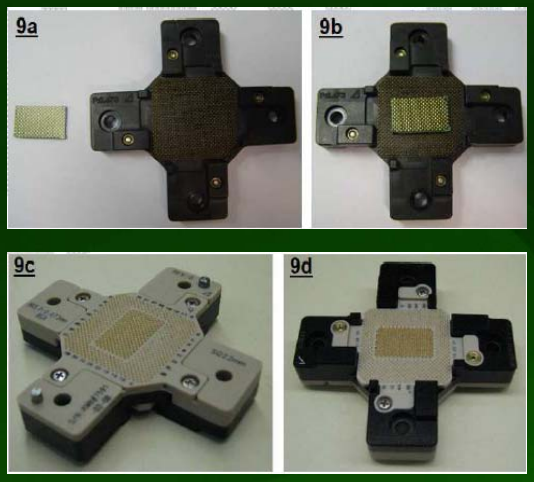
## First Gen (1G) CiS Solution

Original test socket, the embedded capacitor, and the prototype version

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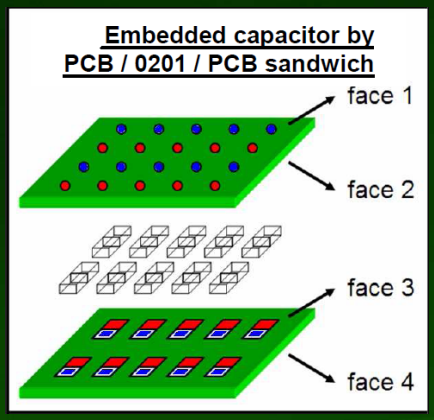
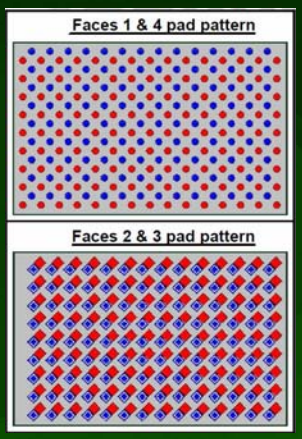
## First Gen (1G) CiS Solution

Embedded capacitor by double PCB and MLCC components hybrid.

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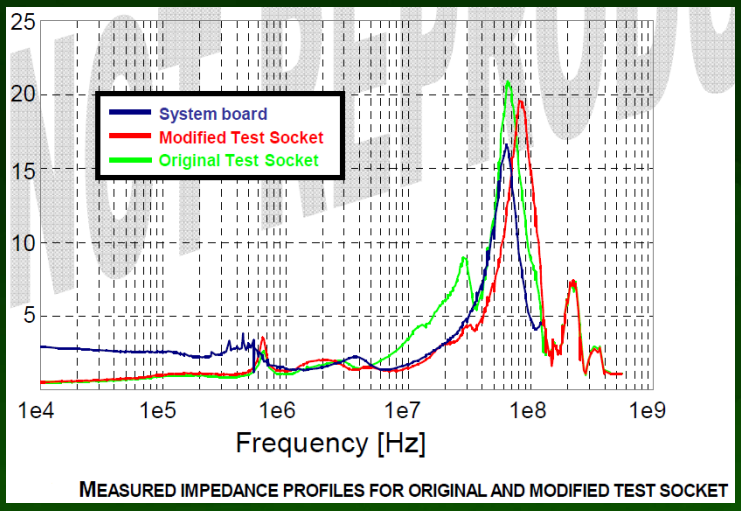
## First Gen (1G) CiS Solution

Results




MEASURED IMPEDANCE PROFILES FOR ORIGINAL AND MODIFIED TEST SOCKET

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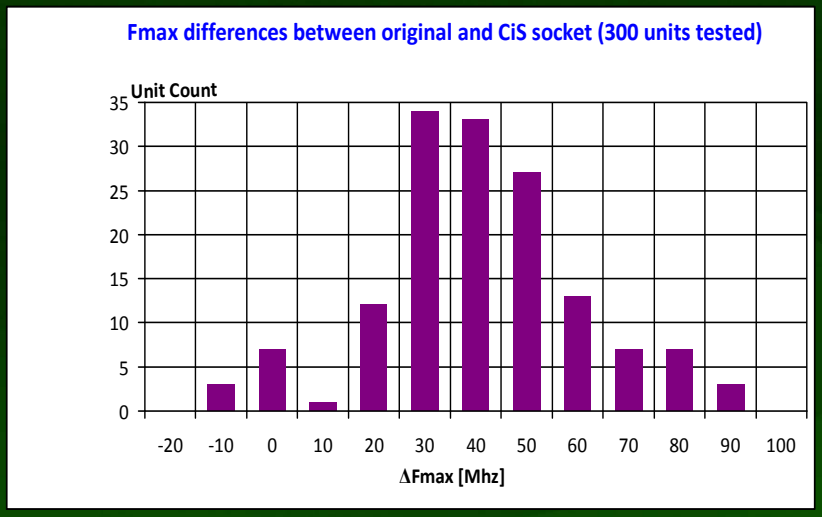
## First Gen (1G) CiS Solution

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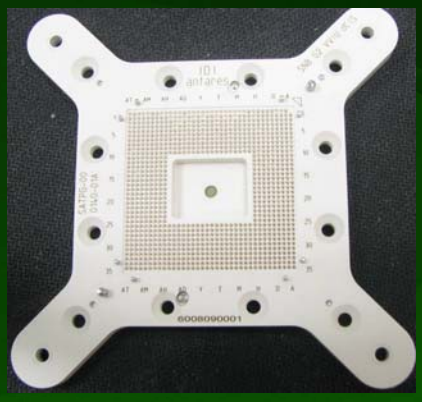
## Second Gen (2G) CiS Solution

Build new socket based on original socket footprint working on Vanguard & Verigy platforms



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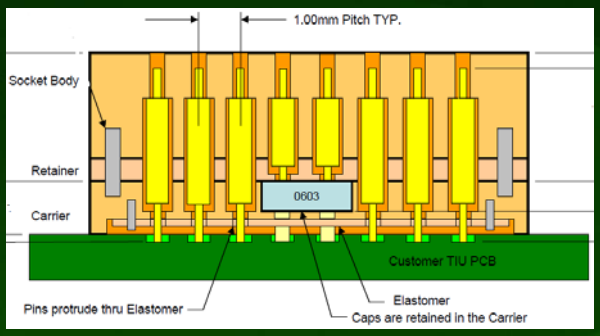
## Second Gen (2G) CiS Solution

- Long pins for regular connection & short pins for the CAPS (2 types of pogo pins)




Cross section

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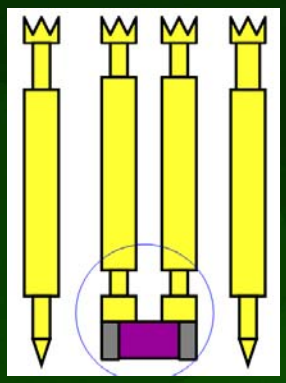
## Second Gen (2G) CiS Solution

- Modify pogo pin tip to a wider one to enable good contact to CAP pad, meet CAP case. Standard LGA plunger tip may miss the cap electrodes due to tolerance variations.
- The custom pin design to penetrate oxidization layer on capacitor surfaces to insure low contact resistance.



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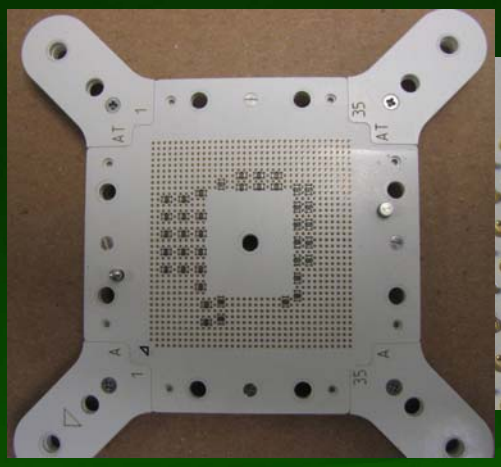
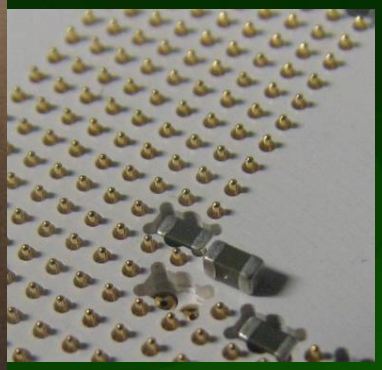
## Second Gen (2G) CiS Solution

- Bottom side: Assign cavities for 0603 CAPS





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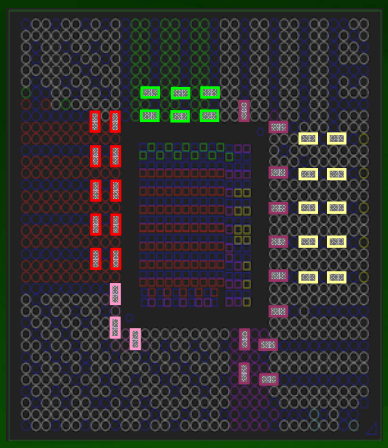
## Second Gen (2G) CiS Solution

**CAPS location**
**(assign CAPS for every P.S.)**



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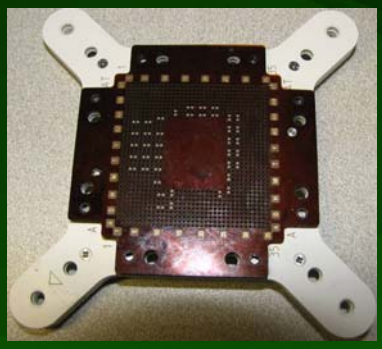
## Second Gen (2G) CiS Solution

- Assemble Elastomer (Kapton material), on bottom side
- Elastomer is functioning as a retainer for non CAP pogo pins and as continuity BTW CAP to PCB in CAPS edge location



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## dCiS + Elastomer Socket 2G Advantages over 1G CiS Solution

- Lower Cost:
  - Due to using two types of pogo pins VS. 3 types in previous solution.
  - Due to using longer pins in CAPS corridor since CAPS located at the bottom. At the previous solution array cap located in the middle, thus pogo pins are shorter.

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- Cycling: Life cycle is higher in the new solution since pogo pins at CAPS corridor are longer
- Flexibility: CAPS replacement to another values and CAPS depopulation. Previous solution is not flexible, need new array CAP (with new CAPS values) for replacement, no option to do CAPS depopulation.

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- Maintenance & Complexity:
  - Previous solution is much more complex for maintenance:
    - Need to keep 3 types of spare pogo pins VS. two types in the new solution
    - Pogo pins array CAP & CAP pogo pins replacement is more complicated in previous socket VS. new socket

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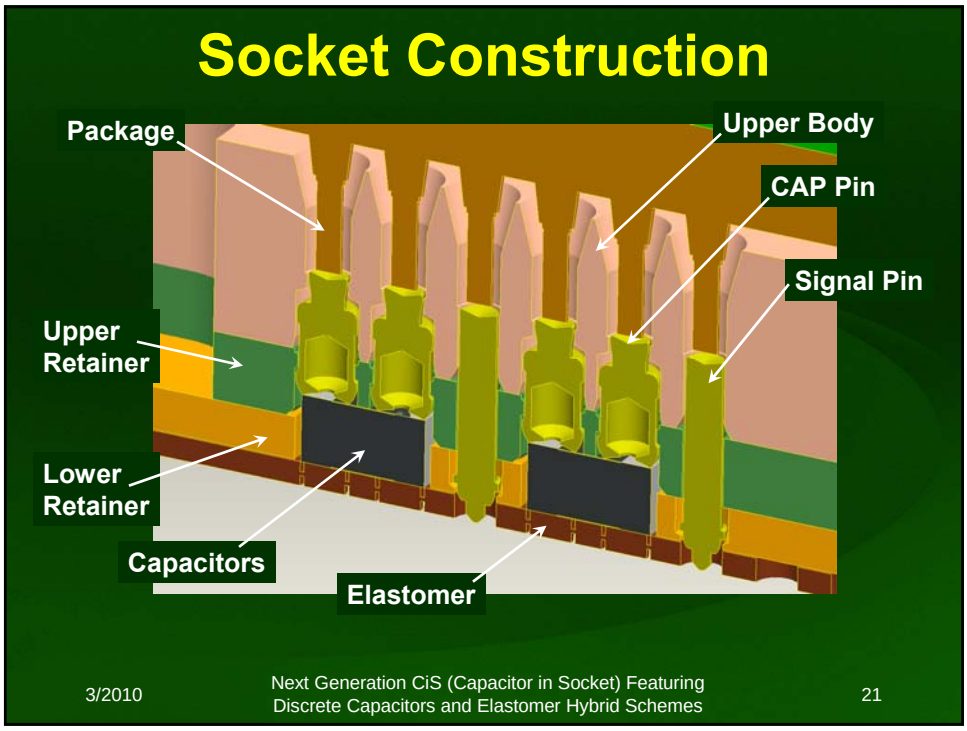
## Socket Validation

- Customer Requirements
- Socket Construction
- 100K Validation



## Customer Requirements

1. Replacement with current POR, follow footprint, KOZ and height of 3.80mm.
2. Simplified socket solution, providing easy serviceability and minimize number of components.
3. Average signal pin CRES to be <90 mΩ.
4. Current carrying capacity is 3.0 amps.
5. Total force per pin is 22 grams.
6. Test temperature - 40°C to 120°C.
7. Meet or exceed targeted cost & cycle life.


Socket Construction
Package
Upper Body
CAP Pin
Signal Pin
Upper Retainer
Lower Retainer
Capacitors
Elastomer
3/2010
Next Generation CiS (Capacitor in Socket) Featuring Discrete Capacitors and Elastomer Hybrid Schemes
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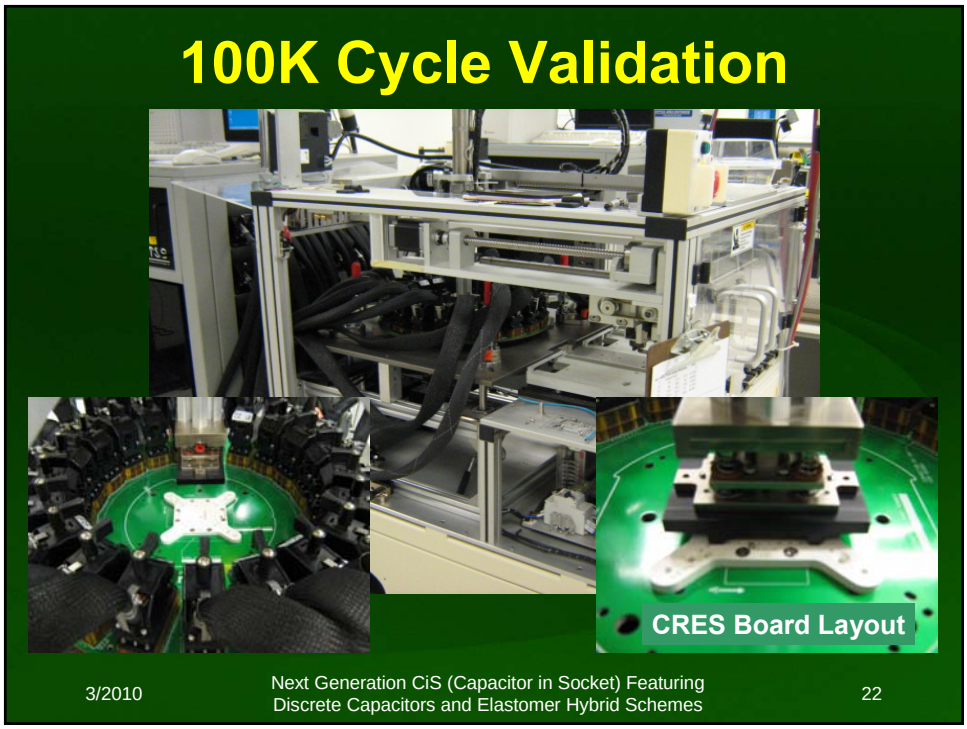
100K Cycle Validation
CRES Board Layout
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Next Generation CiS (Capacitor in Socket) Featuring Discrete Capacitors and Elastomer Hybrid Schemes
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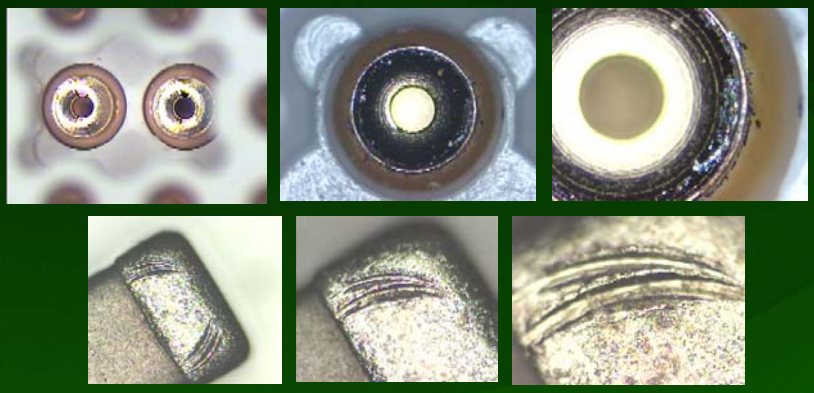
## 100K Cycle Validation

The bottom of the Spring Probe Ring is making strong mark on the Capacitors.



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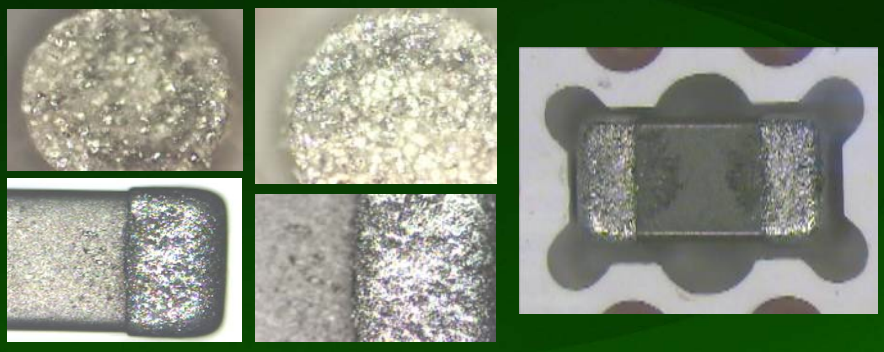
## 100K Cycle Validation

Elastomer columns make clear impression mark on the Capacitors.



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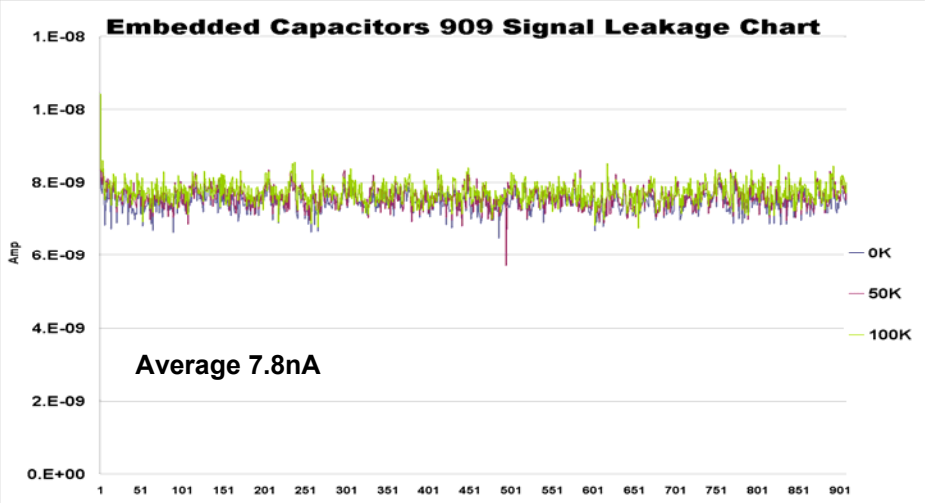
# 100K Cycle Validation

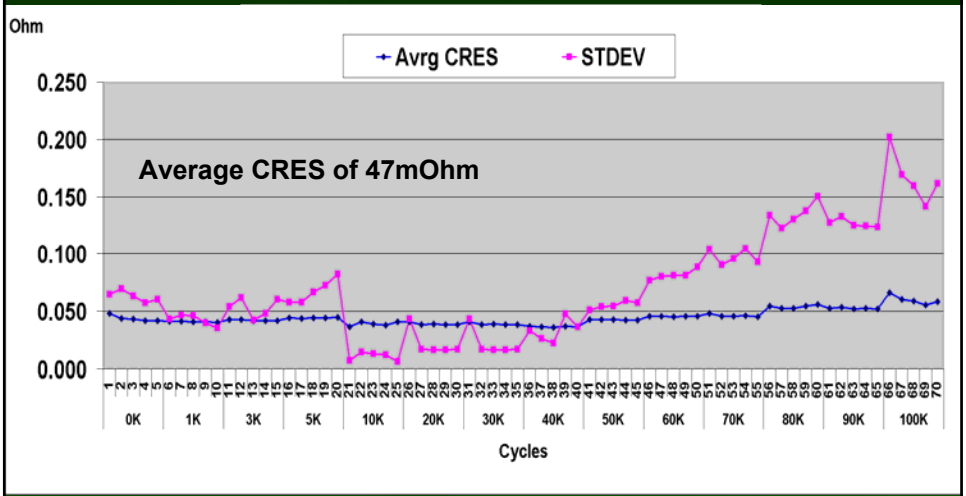
## (909 Signal Pins Only SN#4) 100K Leakage





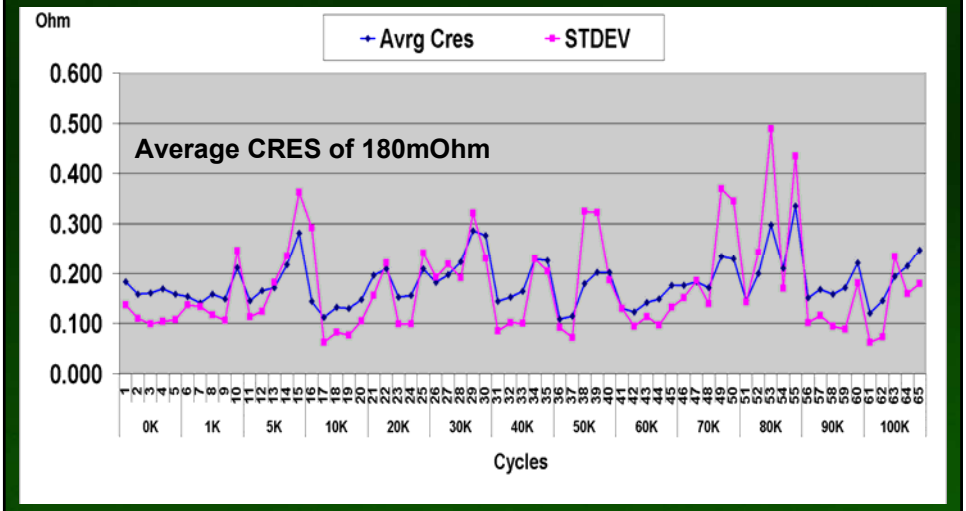

# 100K Cycle Validation

## (909 Signal Pins Only SN#4) 100K CRES



## 100K Cycle Validation

(80 Pins, Cap & Elastomer; SN # 4) 100K CRES

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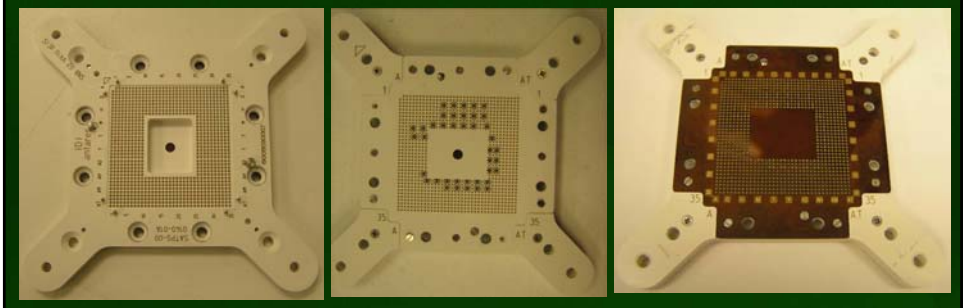
## Socket Validation



After the 100K cycling, socket still looks like new. Socket received no cleaning through entire validation test.

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# Multi Level Stacked Socket Challenges & Solutions

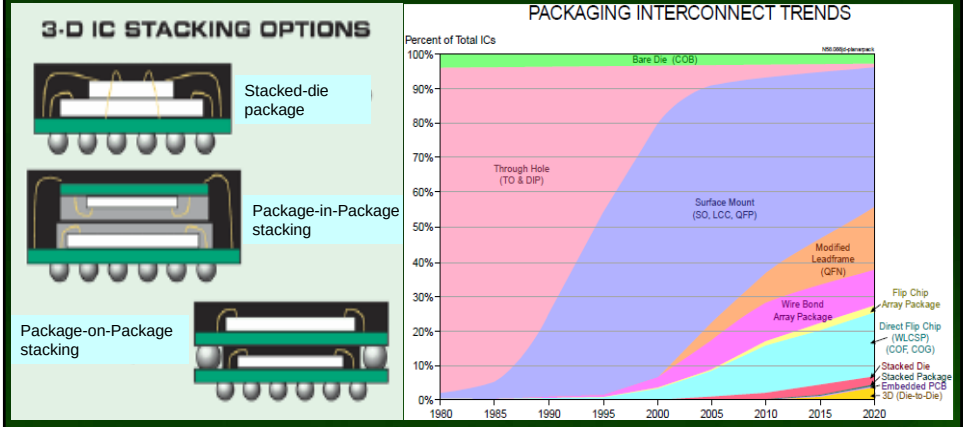
Mike Fedde, Ranjit Patil, Ila Pal & Vinayak Panavala
Ironwood Electronics

2010 BiTS Workshop
March 7 - 10, 2010

## Content

- Introduction
- Multi Level IC Configuration
- Multi Level IC Test Need
- Multi Level IC Socket Configuration
- Electrical Simulation
- Stack up Alignment Challenges
- Stack up Force Challenges
- Conclusion

## Multi Level IC Configuration & Forecast

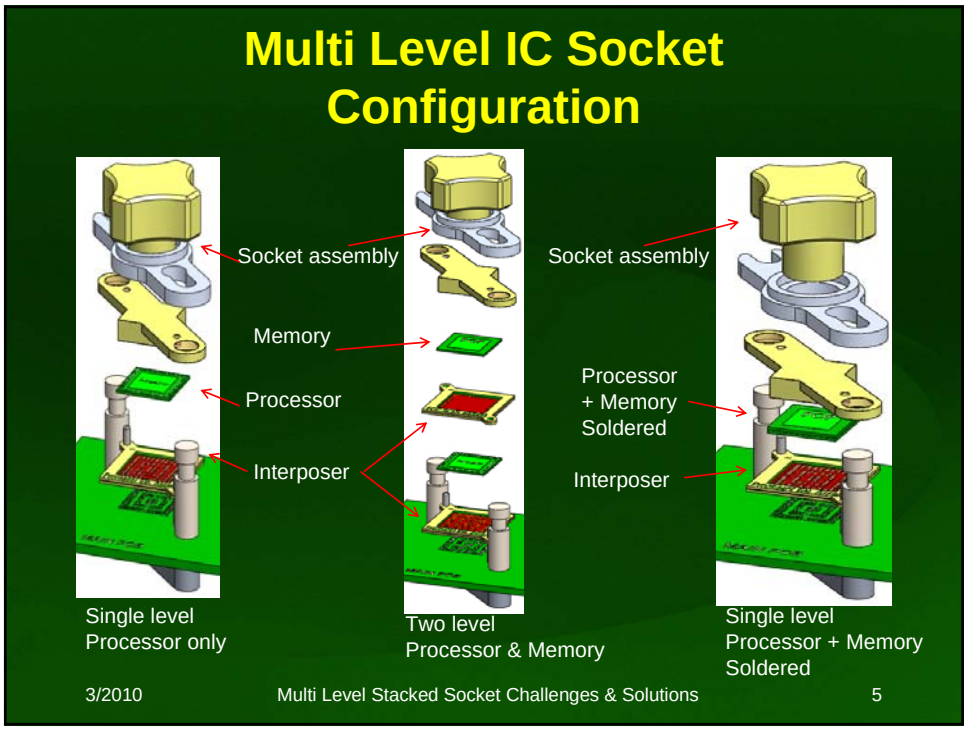



- According to Prismark, In 2020 - 3D packaging share of 7% might total well over 30 billion components that employ stacking technologies.



## Multi Level IC Test Need

- **Test processor by itself in a socket**
- **Test processor signals using a probe which is interfaced between processor and target PCB**
- **Test processor with memory soldered**
- **Test processor with replaceable memory**
- **Test memory signals using a probe which is interfaced between memory and processor**
- **Test memory signals and processor signals using memory probe and processor probe in the stack up between memory and processor on target PCB**


Multi Level IC Socket Configuration
Socket assembly
Memory
Processor
Interposer
Socket assembly
Processor + Memory Soldered
Interposer
Single level Processor only
Two level Processor & Memory
Single level Processor + Memory Soldered
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Multi Level Stacked Socket Challenges & Solutions
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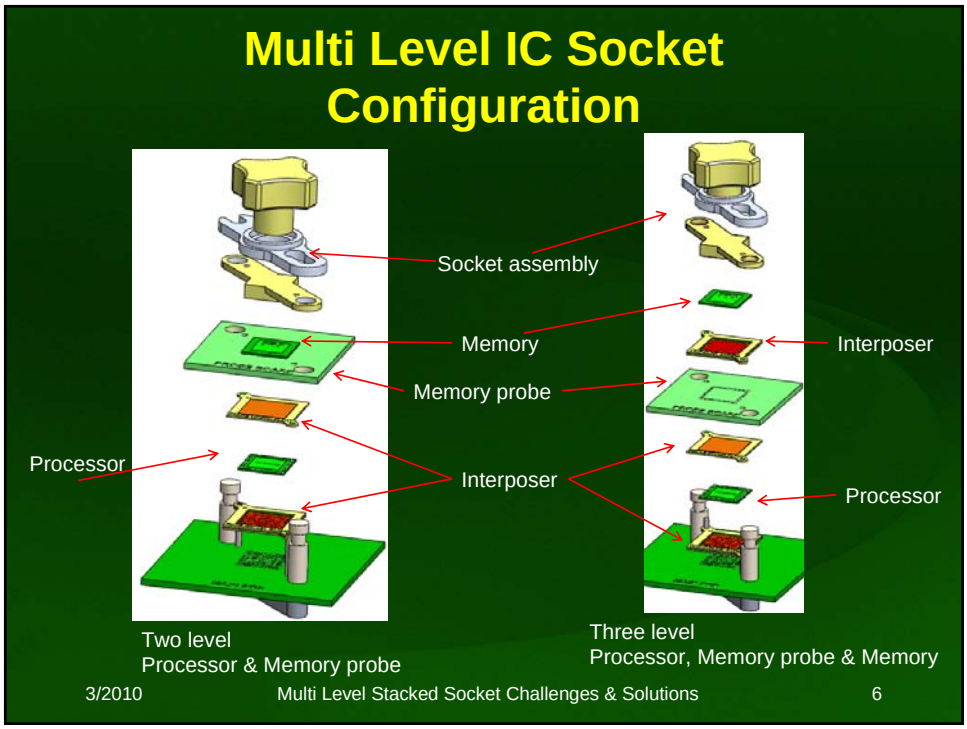
Multi Level IC Socket Configuration
Socket assembly
Memory
Memory probe
Processor
Interposer
Interposer
Processor
Two level Processor & Memory probe
Three level Processor, Memory probe & Memory
3/2010
Multi Level Stacked Socket Challenges & Solutions
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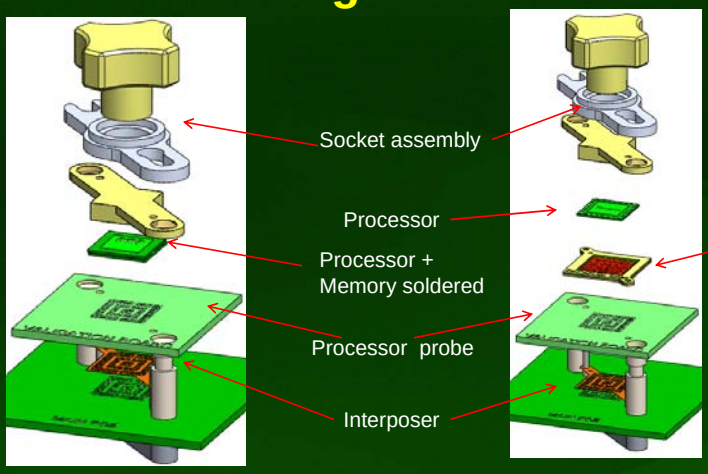
**Paper #2**

## Multi Level IC Socket Configuration




Single level
Processor soldered on probe

Two level
Processor & Processor probe

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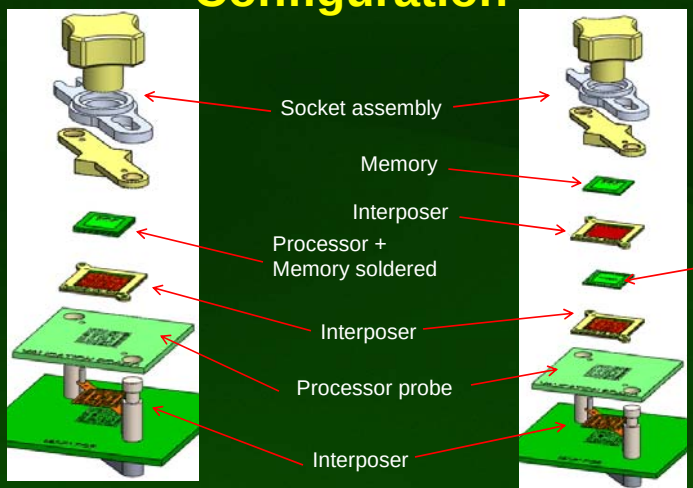
## Multi Level IC Socket Configuration




Two level
PoP & Processor probe

Three level
Processor, Memory & Processor probe

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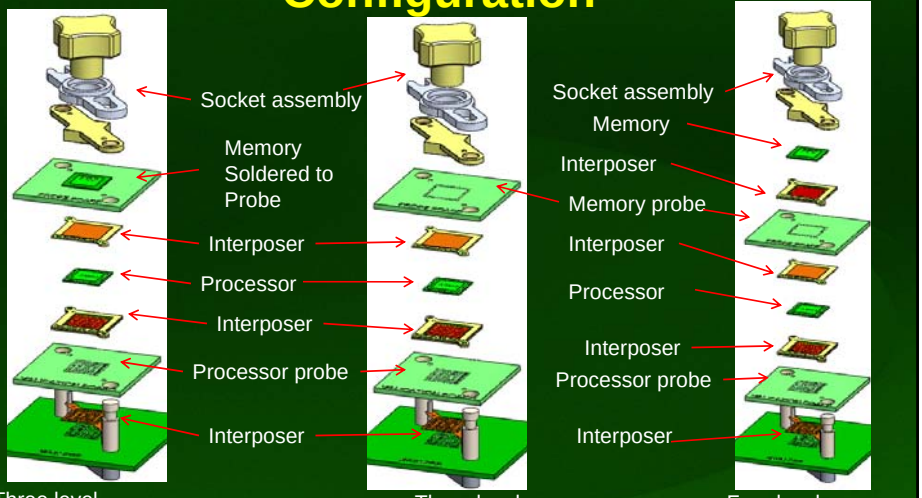
## Multi Level IC Socket Configuration



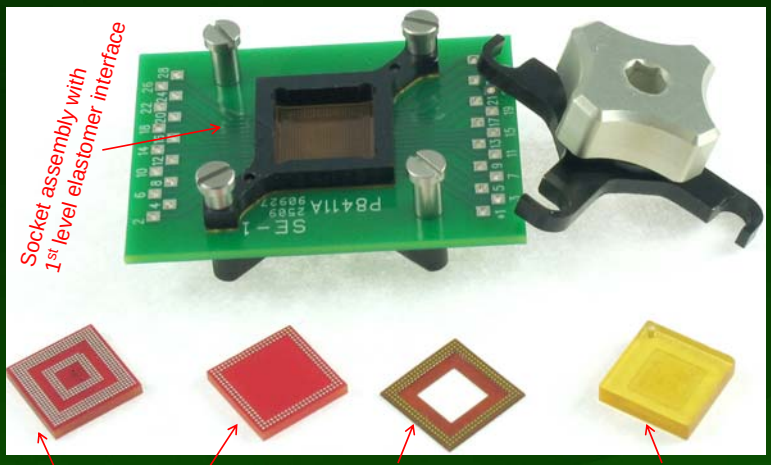

Three level
Memory soldered probe, Processor & Processor probe

Three level
Memory probe, Processor & Processor probe

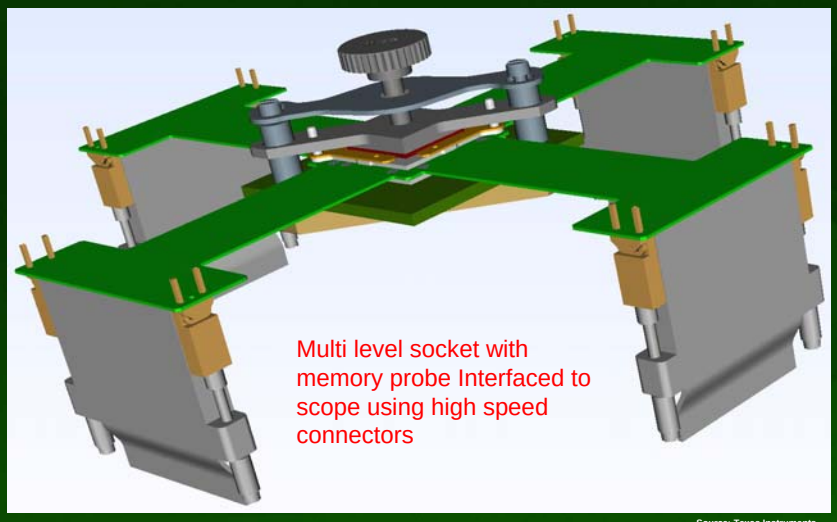
Four level
Memory, Memory probe Processor & Processor probe



## Multi Level IC Socket Configuration



## Multi Level IC Socket Electrical Challenges




Source: Texas Instruments

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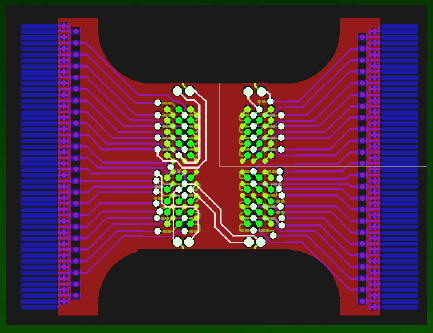
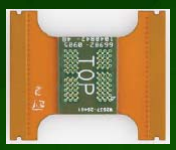
## Multi Level IC Socket Electrical Challenges


Four wing probe for DDR memory

Two wing probe for DDR memory under test



Two wing probe for DDR memory with optimized signal routing

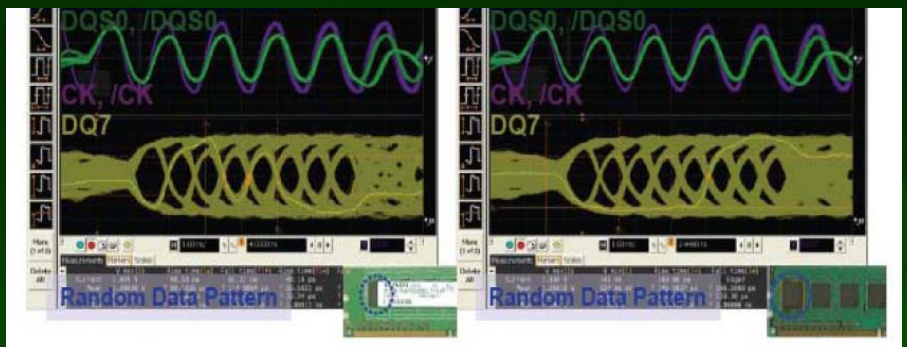



Source: Agilent Technologies

3/2010 Multi Level Stacked Socket Challenges & Solutions 12

## Electrically Transparent Probing

Without interposer | With interposer




Without BGA Probe | With BGA Probe

Source: Agilent Technologies

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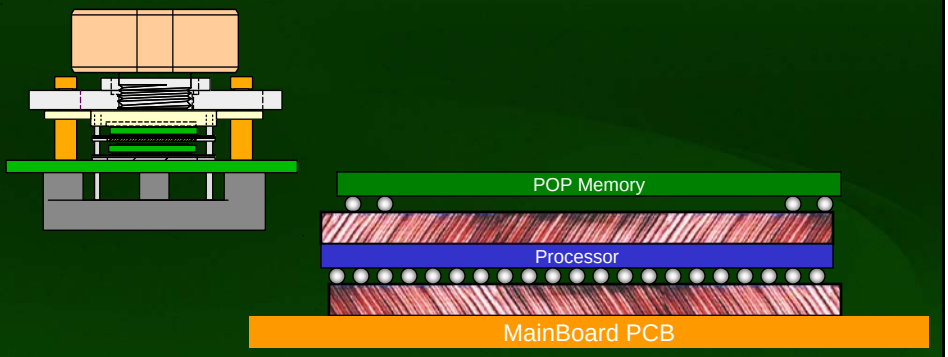
## Multi Level Stack Up Alignment Challenges




**Configuration 1: Processor and Memory**
1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Memory will be centered on the Ball guide and IC guide.

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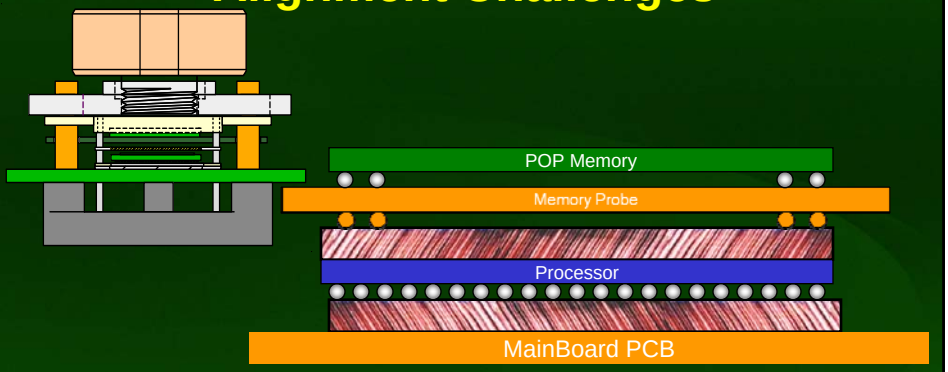
## Multi Level Stack Up Alignment Challenges




**Configuration 2: Processor and Memory Probe**
1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Memory probe will be centered.

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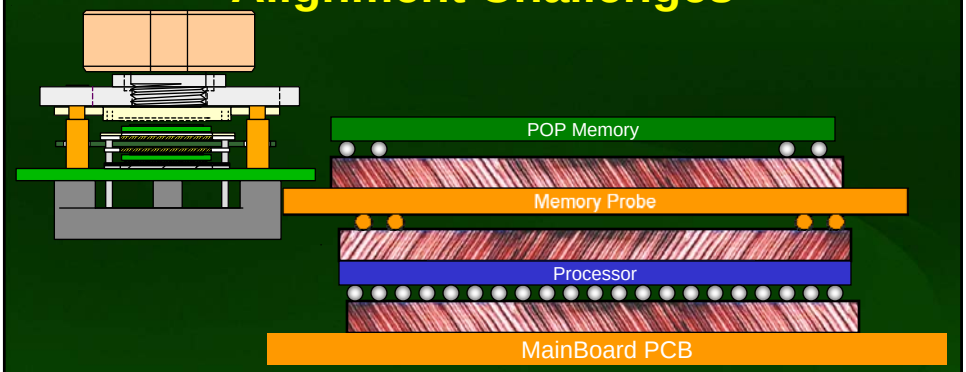
## Multi Level Stack Up Alignment Challenges




**Configuration 3: Processor, Probe board and Memory**
1. Processor is shifted 0.25mm to left with IC guide and Ball guide.
2. From 0.25mm shifted position Probe board will be centered.
3. PoP memory is shifted 0.25mm to left with IC guide and Ball guide.

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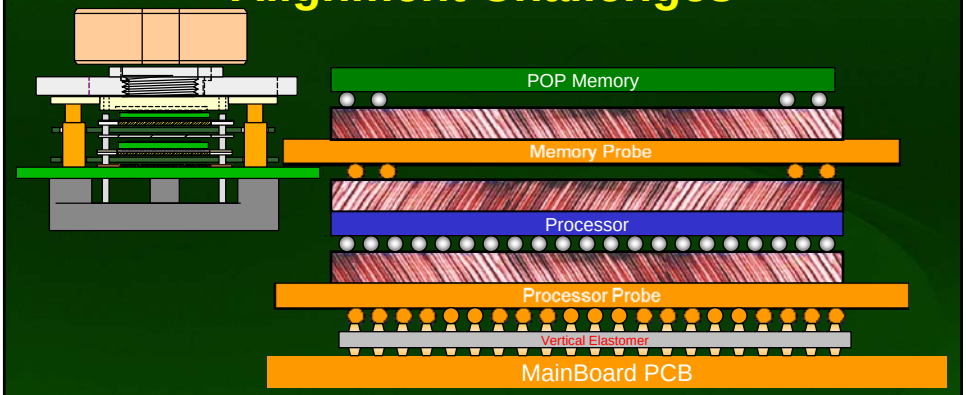
## Multi Level Stack Up Alignment Challenges




**Configuration 4: Processor Probe, Processor, Memory Probe and PoP**

1. Processor and POP sits 0.25mm shifted with pattern on target board. Processor probe and memory probe sits centered with respect to target board.
2. Vertical elastomer on first layer.

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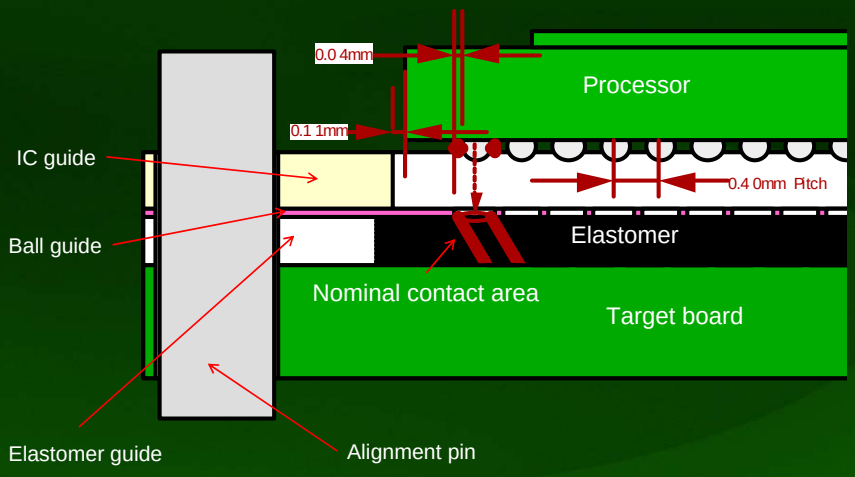
## Multi Level Stack Up Alignment Challenges

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**Paper #2**

## Multi Level Stack Up Alignment Challenges

| | | |
|---|---|---|
| Processor/Elastomer/PCB tolerance | : | ± |
| PCB Alignment Hole position | : | +0.025mm |
| Ball guide Alignment Hole position | : | +0.025mm |
| PCB Pad location/Size | : | +0.05mm |

=0.1mm off from nominal location

With 0.24mm minimum pad diameter for 0.4mm pitch BGA, elastomer contacts more then 58% of the pad. This XY variation occurs on each level of the stack up. Similar calculations were made for Z variations and manufacturing tolerances were updated such that 60% of pad is covered by elastomer.

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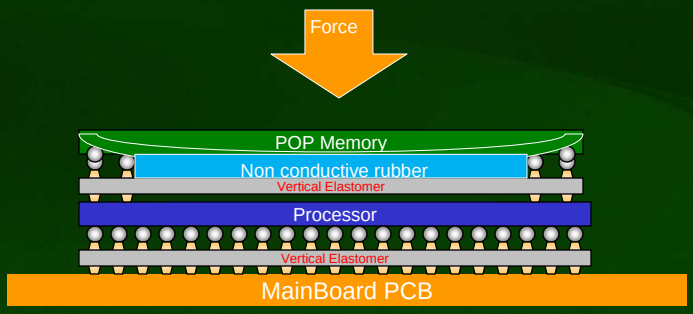
## Multi Level Stack Up Force Challenges




Force balance using additional non-conductive rubber

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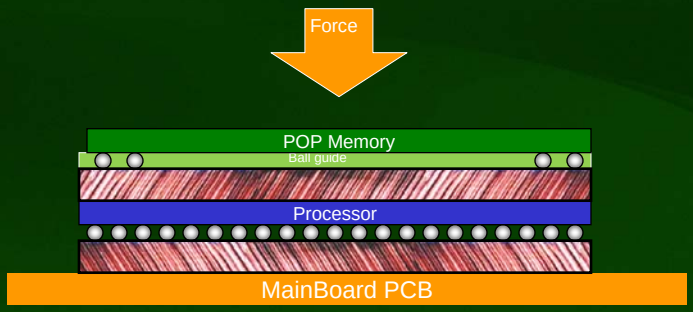
## Multi Level Stack Up Force Challenges




- Force balance using angled interposer itself
- Shift allows normal force to be lower than vertical interposer

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## Multi Level Stack Up Force Challenges

- **Force data for a four level interconnect stack up shown as per ball count**
- **Series network of forces are balanced at each level either by using an additional non-conductive rubber or elastomer by itself**

| | Elastomer | Ball Count | Force/Ball, gm | Total Force, Kg |
|---|---|---|---|---|
| PoP<br>Memory Probe | Angle | 169 | 30 | 5.07 |
| Memory Probe<br>Processor | Angle | 169 | 30 | 5.07 |
| Processor<br>Processor Probe | Angle | 515 | 30 | 15.45 |
| Processor Probe<br>Target Board | Straight | 515 | 35 | 18.025 |

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## Conclusion

- 3D packages are the future
- Pitch, pin count , performance complexities increase due to consumer demand
- Two level package needs four level interconnect for development
- XYZ alignment challenges in each interconnect level push manufacturing capabilities to its extreme
- Force balancing at each level enables innovative design and requires new materials with unique properties

# Advances in WSP- Wafer Socket Pogo-Pin Probing

Norman Armendariz
James Tong

2010 BiTS Workshop
March 7 - 10, 2010

TEXAS INSTRUMENTS

## CONTENT

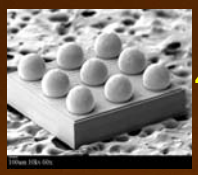
## INTRODUCTION

- WSP- Wafer Socket Probe card technology based on pogo-pin contacts has been qualified for testing WLCSP-Wafer-Level Chip Size Packages on 250 µm diameter solder bumps at 400 µm pitch, instead of current Cantilever and C-VPC; Conventional Vertical Probe Cards.
- WSP card technology has demonstrated a reduced cost of operations with increased electrical and physical performance, and is increasingly displacing conventional wafer-probe methods for WLCSP Devices requiring RF, Non-RF and Non-RF w/ Kelvin capabilities on test floors.



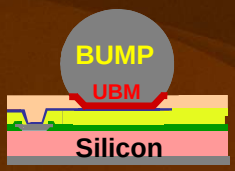
## WLCSP

Texas Instruments has been successfully integrating WSP-Wafer Socket Probe technology; primarily for WLCSP-Wafer Level Chip "Size" Packages using solder bump interconnections into TI and Sub-Con Test Floors.



400 µm pitch

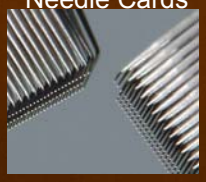
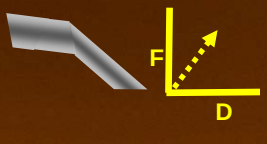
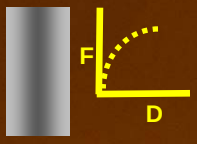
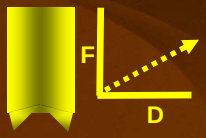
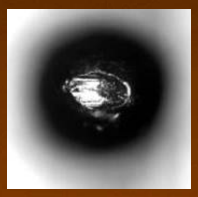
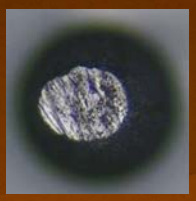
RDL




WSP is categorized into (4) major wafer-level probing applications, from 400 to 150µm pitch on 250 to 75µm diameter solder bumps and Al pads.

- RF-Radio Frequency
- NRF-Non RF
- NRF-Non RF w/ Kelvin
- FC-Flip Chip

## PROBE TECHNOLOGY COMPARISONS

| Cantilever: Needle Cards | C-VPC: Conventional Vertical Cards | WSP: Wafer Socket Probe Pogo-pin |
|---|---|---|
|  |  |  |
|   |   |   |
|  |  |   |

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## WSP MAJOR ATTRIBUTES

- Self-Aligning 4 pts
- Bump Damage < CVPC
- No Reflow Required
- Hand-Test Capable
- Lifetime > 3 M TDs
- PC Analyzer Not Req'd.
- Single-pin repairable
- CRes < CVPC
- Cost ~85% of CVPC
- Cleaning < CVPC
- Kelvin Capable 400um
- Deflection > CVPC
- Force < CVPC
- Interchangeable

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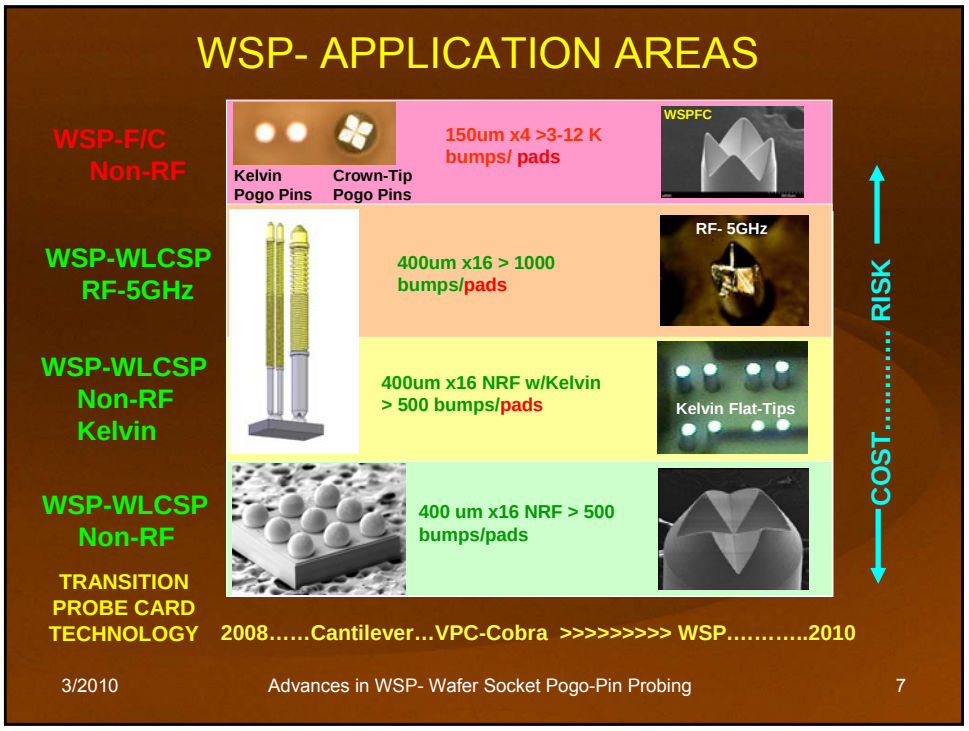
WSP- APPLICATION AREAS
WSP-F/C Non-RF
Kelvin Pogo Pins
Crown-Tip Pogo Pins
150um x4 >3-12 K bumps/ pads
WSPFC
WSP-WLCSP RF-5GHz
400um x16 > 1000 bumps/pads
RF- 5GHz
WSP-WLCSP Non-RF Kelvin
400um x16 NRF w/Kelvin > 500 bumps/pads
Kelvin Flat-Tips
WSP-WLCSP Non-RF
400 um x16 NRF > 500 bumps/pads
RISK
COST
TRANSITION PROBE CARD TECHNOLOGY
2008……Cantilever…VPC-Cobra >>>>>>>>> WSP……2010
3/2010
Advances in WSP- Wafer Socket Pogo-Pin Probing
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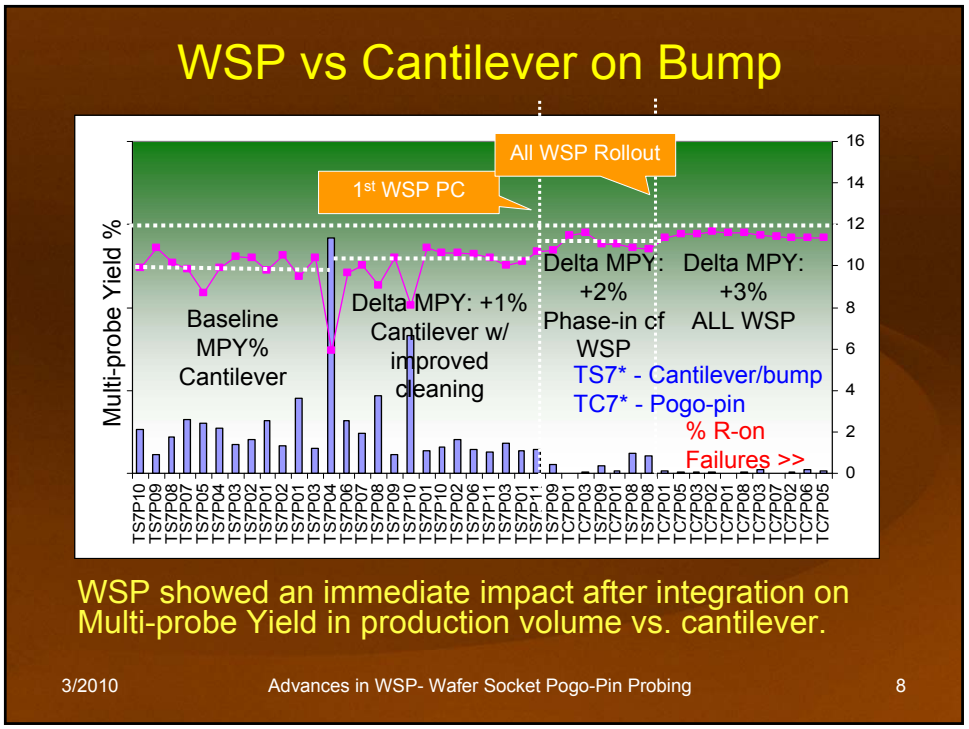
WSP vs Cantilever on Bump
All WSP Rollout
1st WSP PC
Multi-probe Yield %
Baseline MPY% Cantilever
Delta MPY: +1% Cantilever w/ improved cleaning
Delta MPY: +2% Phase-in cf WSP
Delta MPY: +3% ALL WSP
TS7* - Cantilever/bump
TC7* - Pogo-pin
% R-on Failures >>
WSP showed an immediate impact after integration on Multi-probe Yield in production volume vs. cantilever.
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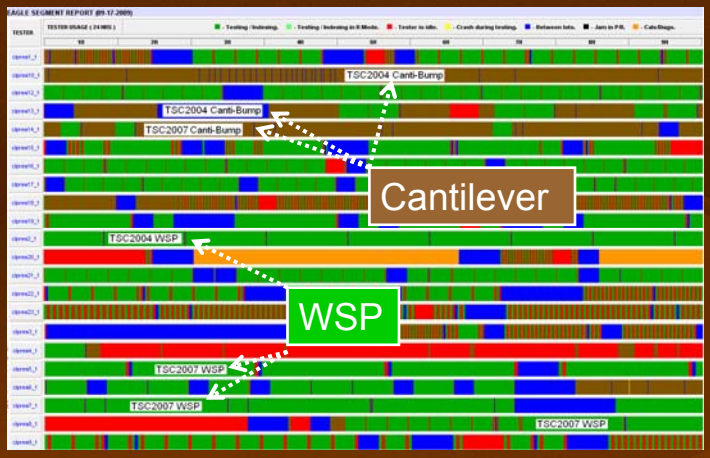
## TEST FLOOR UTILIZATION- WSP vs. Cantilever on Bump




Test floor test cells exhibited significantly higher utilization-rates for WSP, as compared to probing the same WLCSP devices with cantilever probe cards.

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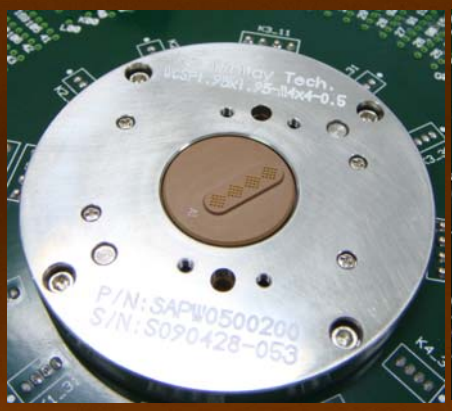
## WSP vs. C-VPC on Bump



WSP-NRF Probe Head

C-VPC NRF Probe Head

Head-to-head comparison performed between a WSP vs. a C-VPC probe head on same WLCSP bumped device using the same PCB and tester.

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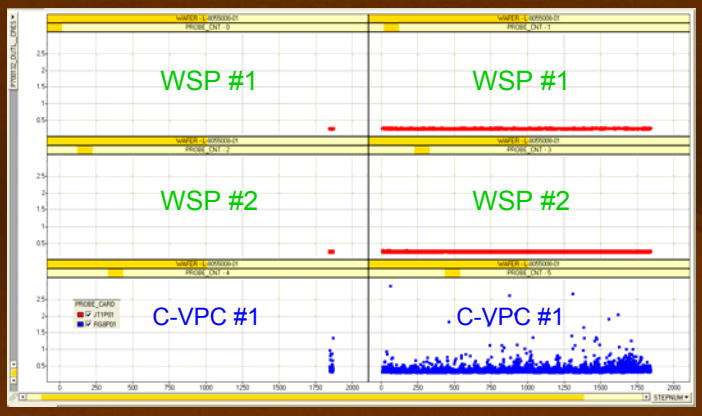
## WSP vs C-VPC: CRes Comparison




Immediate Re-probe First Pass Probe

WSP demonstrated better contact, measured by CRes, in terms of lower Immediate Re-probe and higher First Pass-Probe rates, as compared to the C-VPC probe head.

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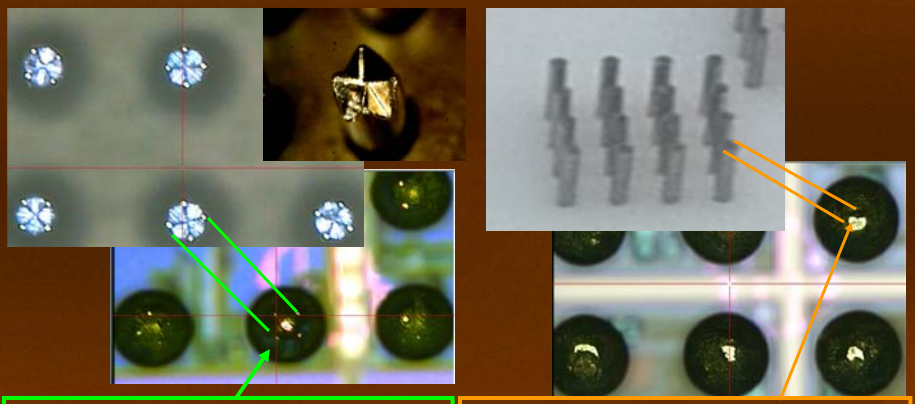
## WSP vs. C-VPC Probe Tip Effects



Four WSP pogo pin Crown tips self-align and "pierce" the sides with min. damage and no effect on ball ht. with min. CRes. Valleys between tips allow debris to channel away during probing.

C-VPC Flat tips "impact" the top side of the ball . Ball height affected. CRes not as stable, requiring more force and more cleaning to remove compacted debris and may require. reflow.

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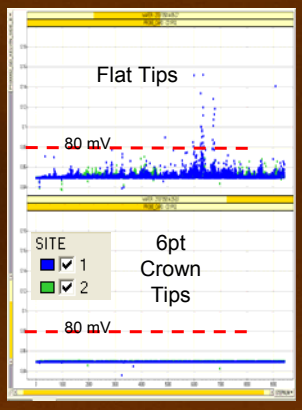
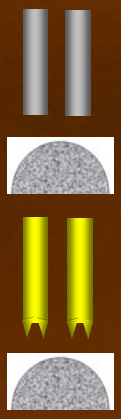
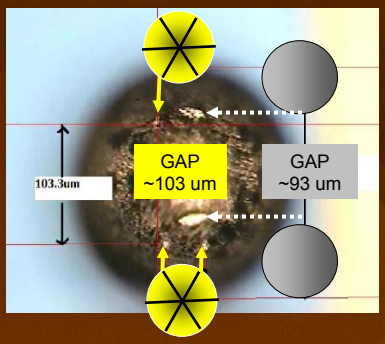
## WSP-Kelvin Crown vs. Flat Tips



Kelvin 6 pt Crown-and Flat- Tip Indent Marks.




A Kelvin measurement uses (2) probes to contact (1) solder ball. Gate-Drain Kelvin Voltage Drop shows 6pt Crown Tips contact more stable than Flat-Tips. However, gap between indent marks ~ 10 µm more for 6 pt Crown tips vs. Flat- Tips.

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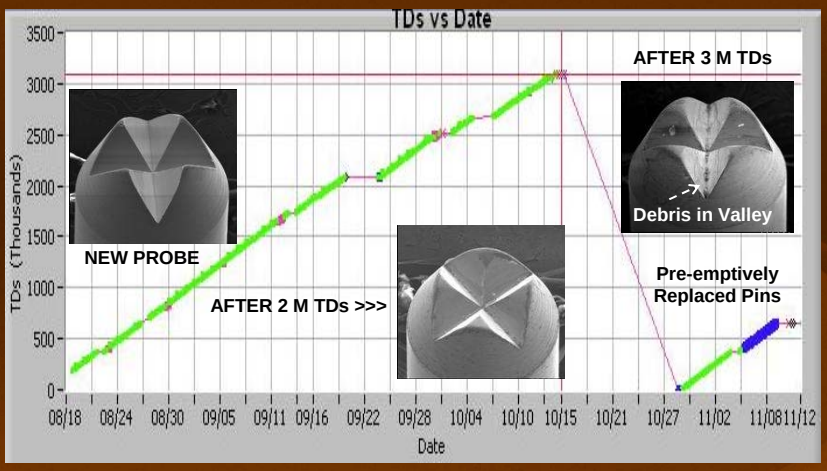
## Solid Pd-Alloy Probe Material Wear Characteristics




Wear observed from WSP solid Pd-alloy pogo pin crown tips exhibited lifetimes exceeding 3 M TDs with “valleys” facilitating self-cleaning processes.

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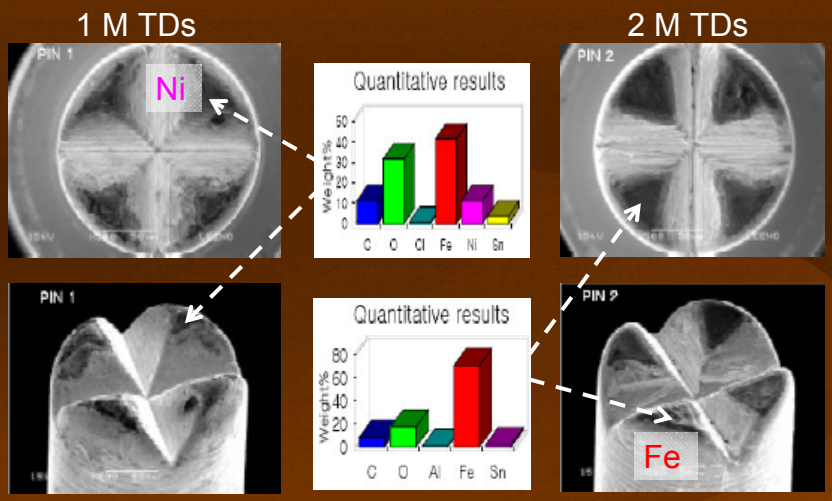
## Au/Ni-Plated Probe Tip Material Wear Characteristics

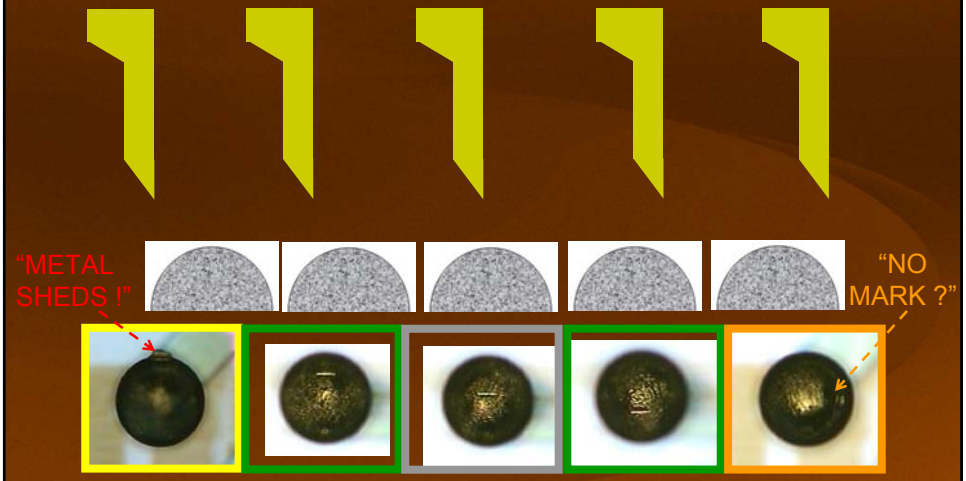



Wear observed from WSP Au/Ni plated pogo pin crown tips exhibited lifetimes exceeding 2 M TDs.



## WSP Angled-Probe Tip Effect on Bump

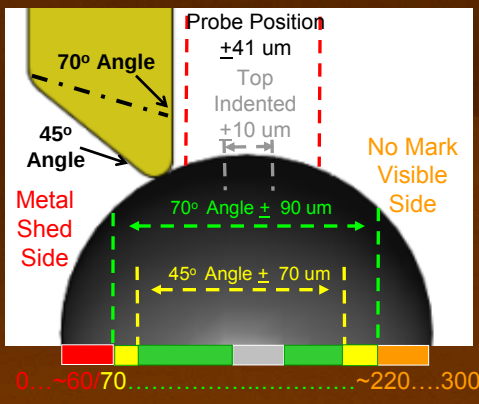
Performed DOE to understand the effect of using Probe tips with 45 and 70º Angled Tips on a Solder Ball surface.




Probed in 10 um increments across a 300um dia. solder ball surface.

## Angled Probe Tip Characterization

Results showed that the 70º rake angled tip would deform "shed" ball at ~60um and the 45º tip would "shed" ~70 um from the solder ball edge.



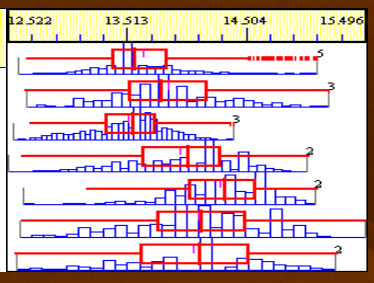

Although good electrical contact was observed on the "No Mark" side; Lack of a mark considered problematic for test floor operations.

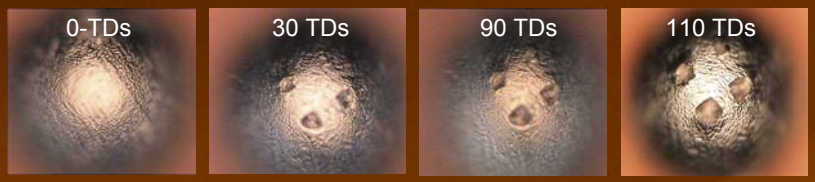


## WSP Effect on Bump Integrity

CRes Avg (Ω) >

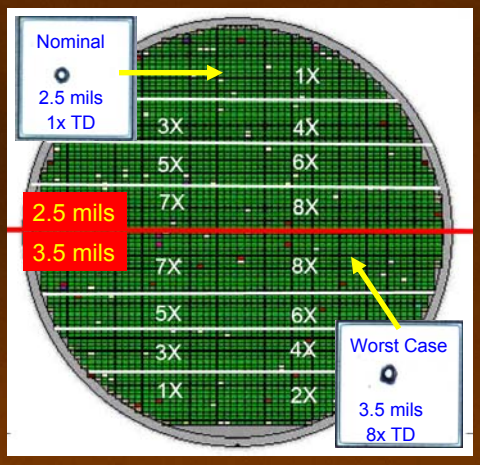
| | Mean | Std Dev | Min | Max |
|---|---|---|---|---|
| 0 TDs | 13.65 | 0.4245 | 12.60 | 15.09 |
| 30 TDs | 13.85 | 0.4679 | 12.68 | 15.19 |
| | 13.52 | 0.3243 | 12.57 | 14.39 |
| | 13.95 | 0.4577 | 12.52 | 15.02 |
| 90 TDs | 14.29 | 0.4015 | 12.65 | 15.08 |
| 110 TDs | 14.11 | 0.5381 | 12.61 | 15.50 |
| | 14.07 | 0.5734 | 12.60 | 15.24 |




No statistically difference observed after repeatedly probing a WLCSP solder ball > 110 TDs, in terms of CRes or damage to RDL or DUT.

## WSP on Al-Pad Integrity




Probed a wafer with WSP radiused pogo-pins in 2 separate regions, each with different probe over-travel conditions (2.5 and 3.5mils).

In each of these 2 regions, an increasing number of touchdowns (1x to 8x) were repeatedly applied to the same (90 x 90um) Al pad, but on different die within different TD x sections of the wafer.

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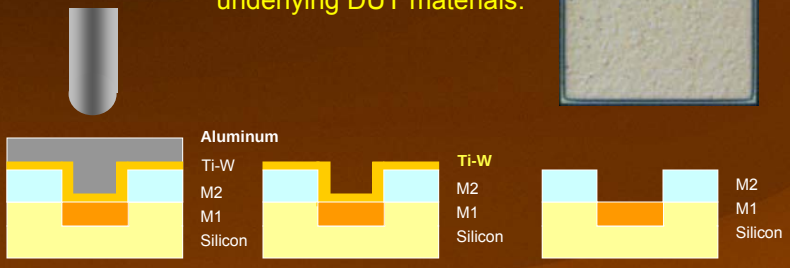
## WSP Probing Effect on Al Pads

After probing, each segment chemically de-processed / inspected for any damage / cracking caused to the underlying DUT circuitry.


Ti-W surface appeared embossed from probe indent, but no penetration or cracks detected to underlying DUT materials.

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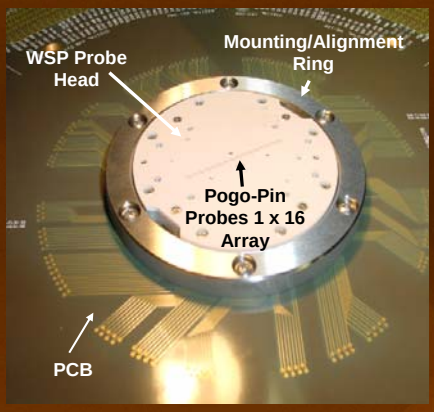
## WSP Interchangeability:

Universal standard mounting / alignment ring on the PCB developed to facilitate "swapping" probe heads from the same or different probe head suppliers with following advantages:

- –A new PCB design is not required.
- –Simplifies the layout; becomes probe head manufacturer independent.
- –Multiple vendors can be utilized on the same PCB allowing for multiple sourcing.
- –Mounting rings can be bought in bulk and ahead of time.




WSP Probe Head utilizing the universal mounting / alignment ring on PCB

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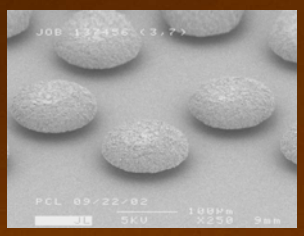
## WSP Flip-Chip Strategy

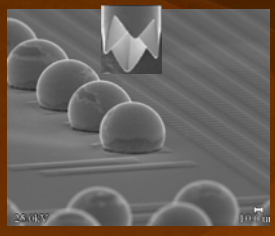
Leverage the attributes of WSP "crown" tip pogo-pins, as demonstrated on 400 um pitch (250µm bump diameters) WLCSP bumped devices, but scaled-down to apply on Flip Chip bump geometries, >150um pitch (75µm spherical bump diameters).

WSP

WLCSP 400um Pitch, 250um Dia. Spherical Bump



FLIP CHIP 150um Pitch, 130um Dia. Mushroom Bump



FLIP CHIP 150um Pitch, 75 um Dia. Spherical Bump

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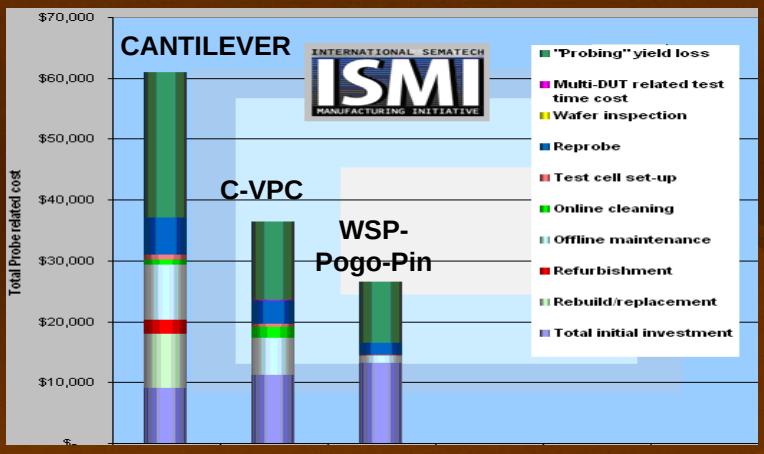
## COO- COST OF OWNERSHIP




ISMI Probe COO empirical model shows WSP technology as a more cost-effective test solution than current technologies for a particular WLCSP device evaluated.



## WSP SUMMARY

- WSP targeted to displace all of the Cantilever that probe bumped WLCSP devices.
- WSP expected to increasingly displace Cantilever that probe Al-pads, if within WSP geometric capability.
- WSP expected to increasingly displace most C-VPC used on both WLCSP and Flip Chip Devices.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Dale Ohmart
Minette Ohmart
Al Weglietner
Angel Melquiadez
Ace Arricivita
Ronald Payumo
Mike Yadzani
Jesse Ko
ECT
NHK
WinWay
MJC
yokowo
Ardentec
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# Answering the Call

**Tom Bresnan**
**R&D Circuits**

**2010 BiTS Workshop**
**March 7 - 10, 2010**

- "While Moore's Law has spawned a profusion of product features and functions through ever cheaper and abundant transistors, it has left test with increasing complexity and cost. …

**Navid Shahriari**
Director of Sort Test Technology Development
Intel Corporation
BiTS 2009 Distinguished Speaker



**Paper #4**

…Additionally, market forces necessitate ever-smaller form factors as mobile products become ubiquitous. …

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…This combination of shrinking geometry, increasing bandwidth and expanding features creates a confluence of mechanical, electrical and thermal challenges that run head-on into a severely cost constrained environment in the midst of an economic downturn."

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## Agenda

- Answering the Call!
- Inspiration
  - Navid's presentation
  - Detofsky (et al) presentation
- Moore's Law is Alive and Well
  - It all comes together at the test interface

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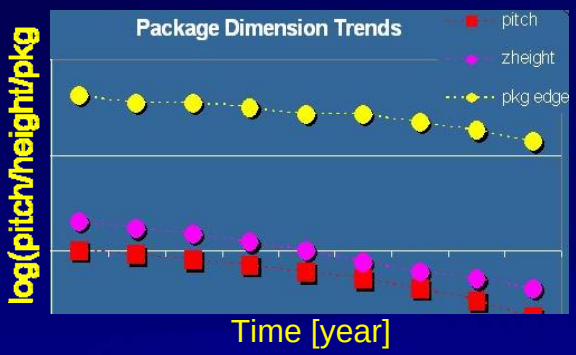
## The Problem Statement

- Aggressive package scaling continues on modern microprocessors

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## The Problem Statement..

- Package designers trade off
  - Package area reductions
  - On-package components
    - capacitors
- Removal means
  - Power integrity burden
    - Motherboard
    - DIB

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## Comparing the TIU and CRB

- The TIU has decoupling capacitors much farther away from the DUT than the CRB (Customer Reference Board)
- Next few slides courtesy Intel and used with permission. (Abram Detofsky, et al)

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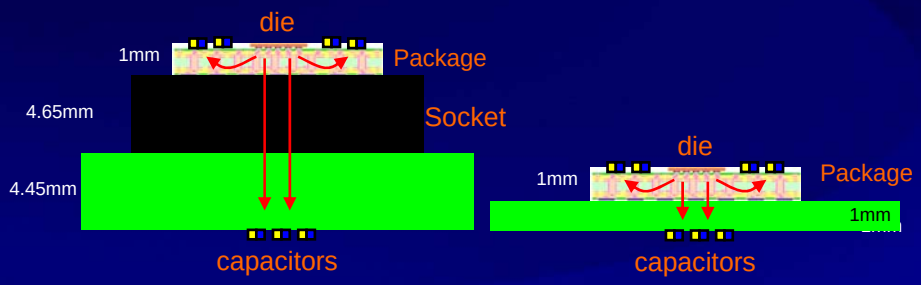
## Comparing the TIU and CRB

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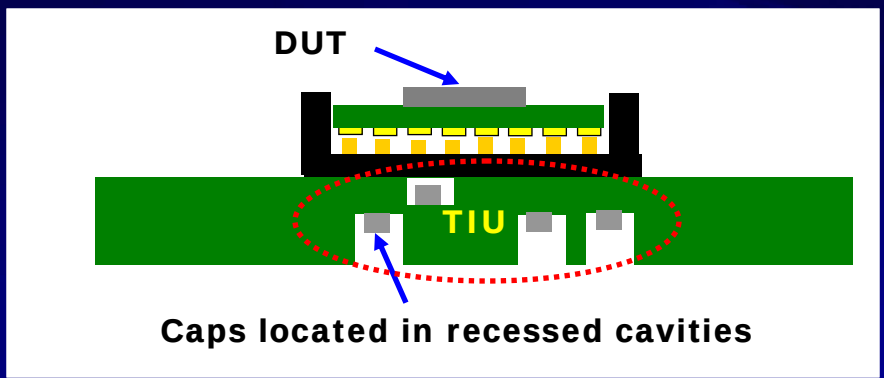
## Alternative Solutions

- Recessed cavity PCB

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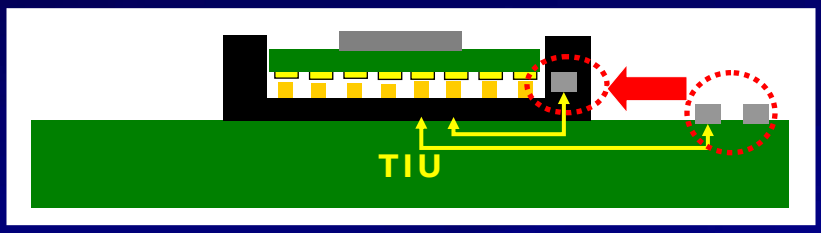
## Alternative Solutions

- Embed capacitors (in socket body)

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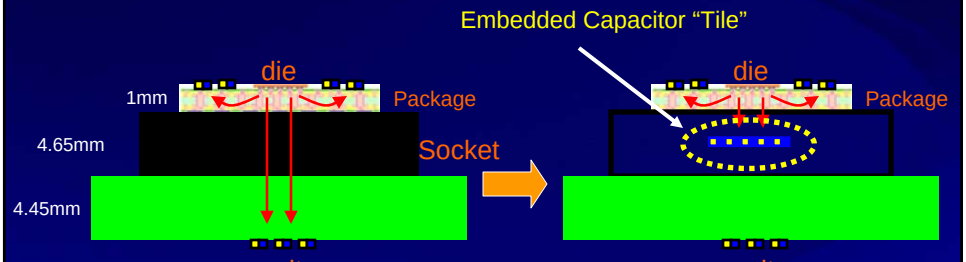
## Intel proposed solution

- CiS (capacitor in socket)




Old Contactor CiS Contactor

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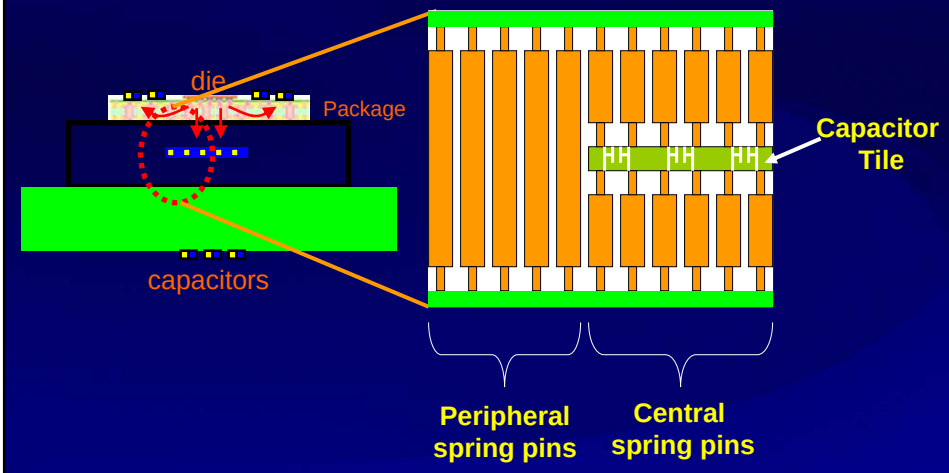
## CiS contactor

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## The drawbacks

- High risk PCB manufacturing
- New mechanical structures
  - Components in socket body
- Devices in socket
  - Multiple spring pin dimensions
  - Load matching
  - Distributed / shared capacitance
    - Diminished?

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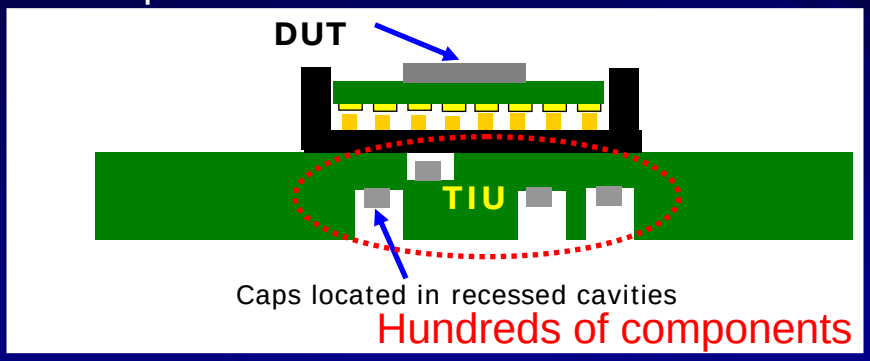
## Recessed cavity PCB

- High risk PCB manufacturing
- Sequential laminations = $$

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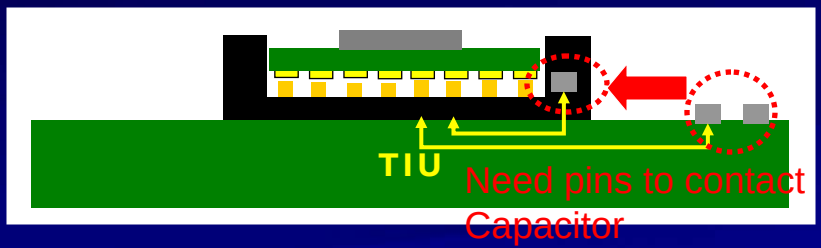
## Embedded capacitors

- New combination of component and socket
- More pins = more inductance

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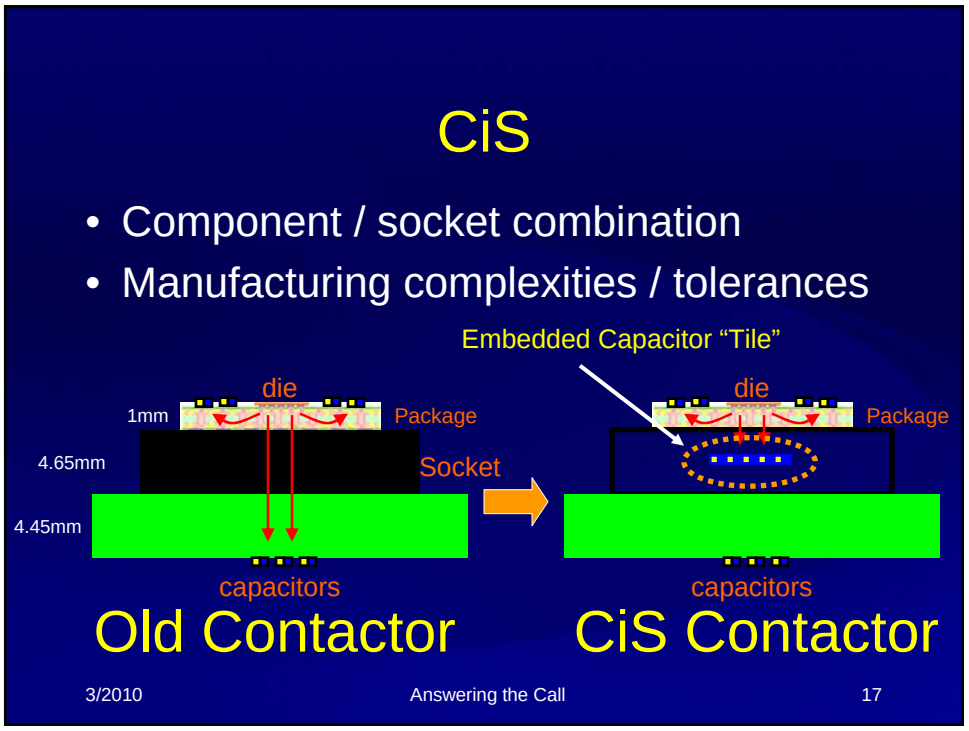
CiS
• Component / socket combination
• Manufacturing complexities / tolerances
Embedded Capacitor "Tile"
die
1mm
Package
4.65mm
Socket
4.45mm
capacitors
Old Contactor
die
Package
capacitors
CiS Contactor
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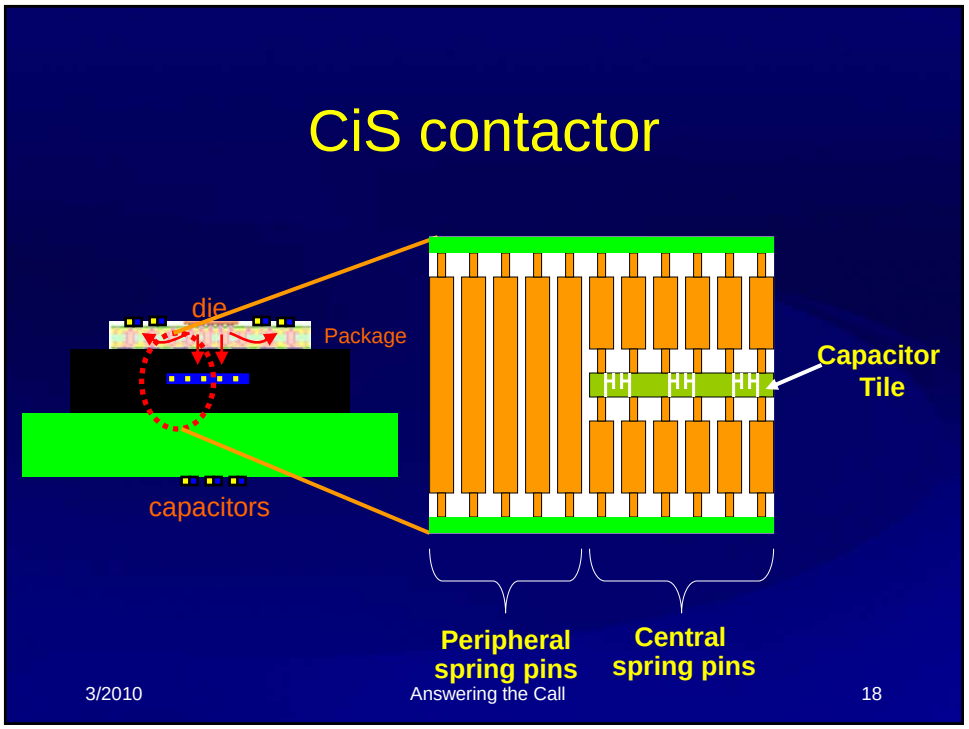
CiS contactor
die
Package
capacitors
Capacitor Tile
Peripheral spring pins
Central spring pins
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## Proposed Solution

- Standard board manufacturing
  - Some risk (low)
- Components / PCB
  - No new combination of materials / processes
- Various options
  - Not just power delivery

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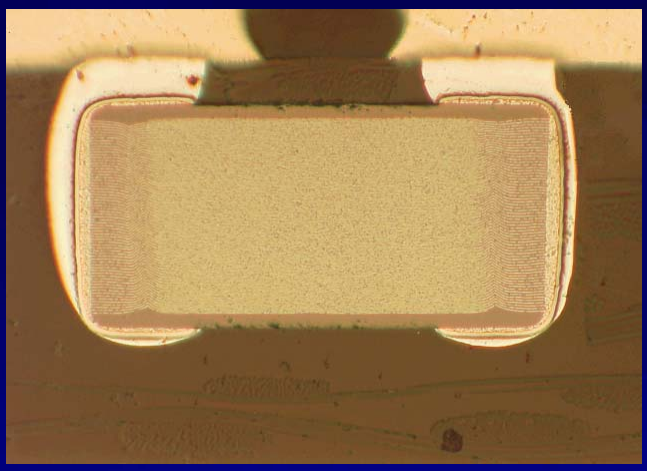
## Embedded Components



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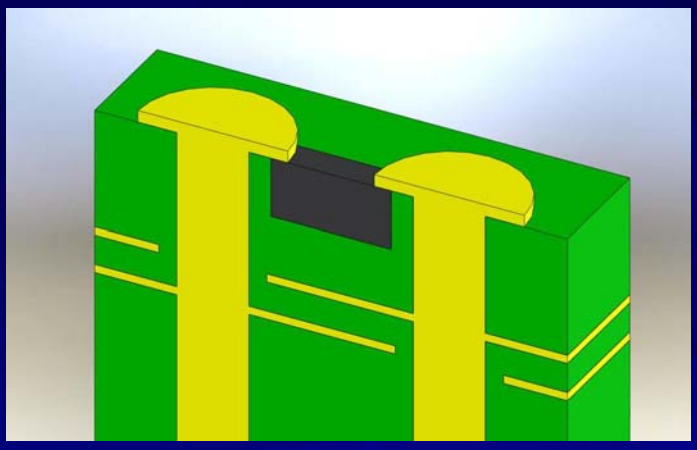
## Embedded Components



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## Embedded Components

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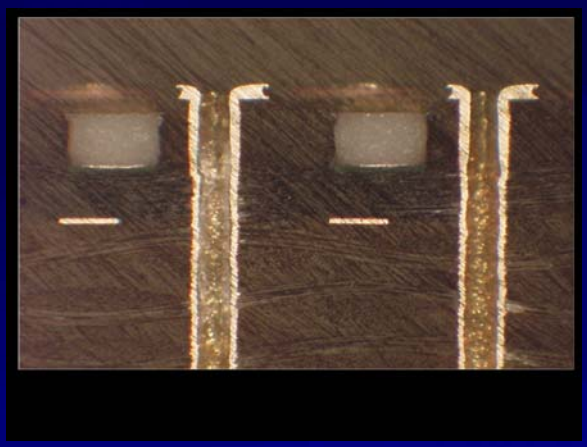
## Embedded Components



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## Proposed Solution

- Power delivery
  - Capacitors assembled under layer one
  - Scalable to pitch
  - Variety of attachment methods
    - Solder
    - Conductive epoxy

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## Proposed Solution

- Via transition elimination
  - Capacitors assembled on circuit layers
    - Eliminates need for via to surface and back
  - Space for vias already allotted
    - Similar design rules

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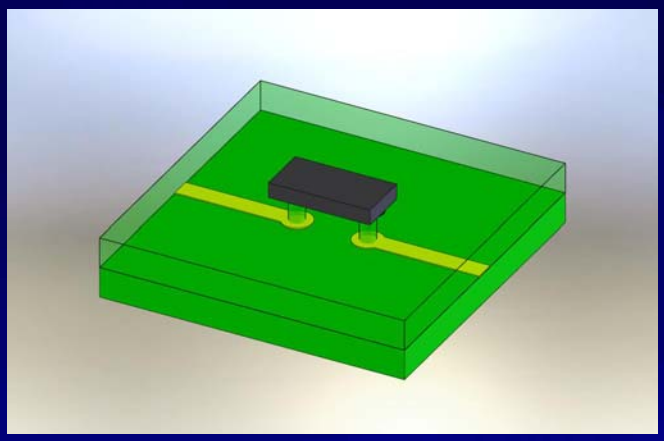
## Surface mount w/ vias



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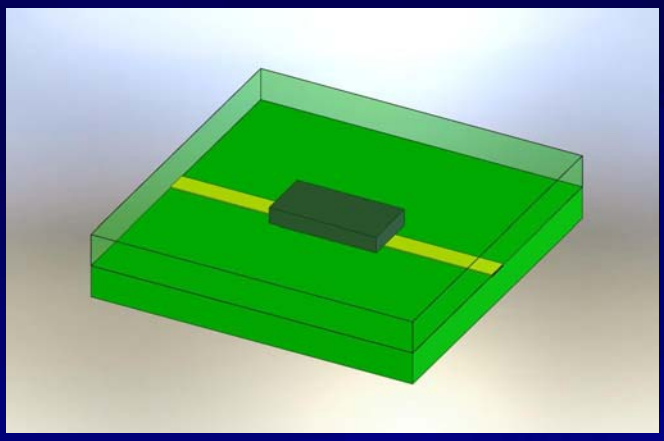
## Embedded, no vias



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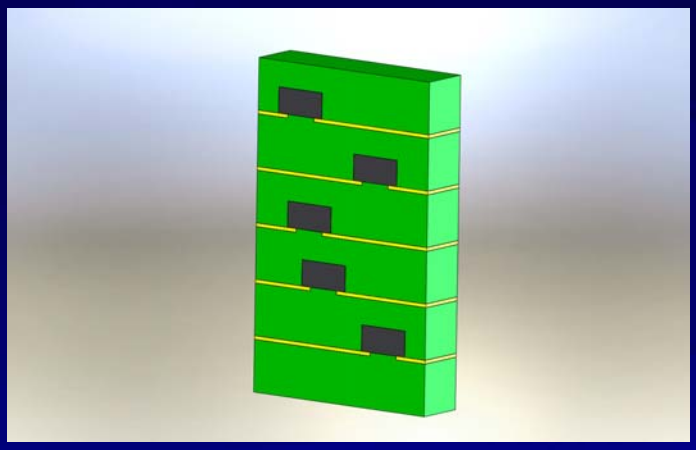
## Embedded, multiple layers



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## IST PWB Reliability Testing

- I.S.T. = Interconnect Stress Test
- Determines overall reliability of PWB
- Tests Copper Interconnection AND Material
- IPC Approved Test Method
- Industry Wide (Customer) Acceptance

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## I.S.T. Defined

- Interconnect Stress Test
  - Thermal Cycles by Electrically Heating an IST Test Coupon
  - Continuously measures resistance of the circuits during cycle
  - 10% Increase in Resistance is Failure – Test Stops in Seconds

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## Test Plan

- TV22029A
  - S1 buried capacitors only
  - S2 for buried capacitors connected to a thru hole
  - S3 for L4-L19 plated thru holes
  - S4 plated thru holes

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## The Test Plan

- S1 & S2 measurements (in pF)
  - AR, Bake, Pre-Con, x100
    - Bake = 150°C – 2 hours
    - Pre-Con= 2x reflow @ 210°C
      - Simulate 2 assembly cycles
  - 1,000 cycles to 110°C

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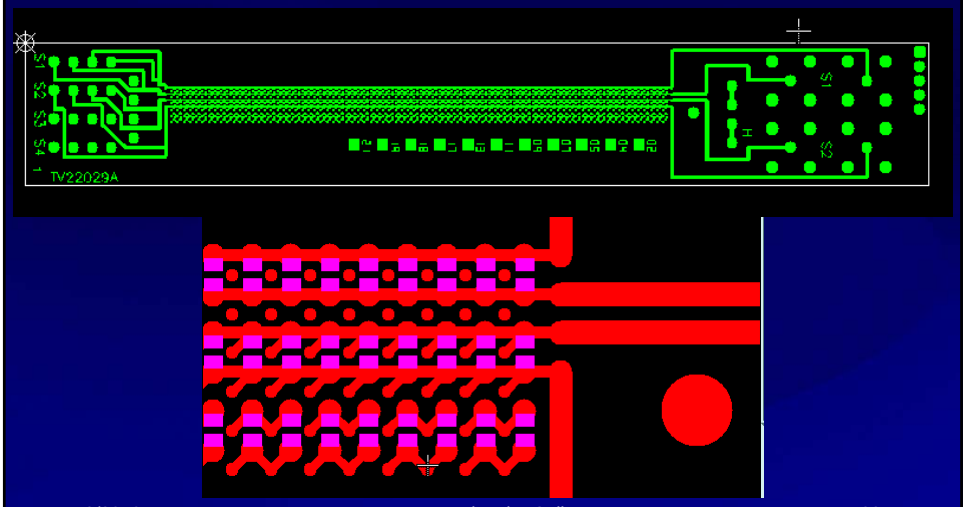
## The Coupon

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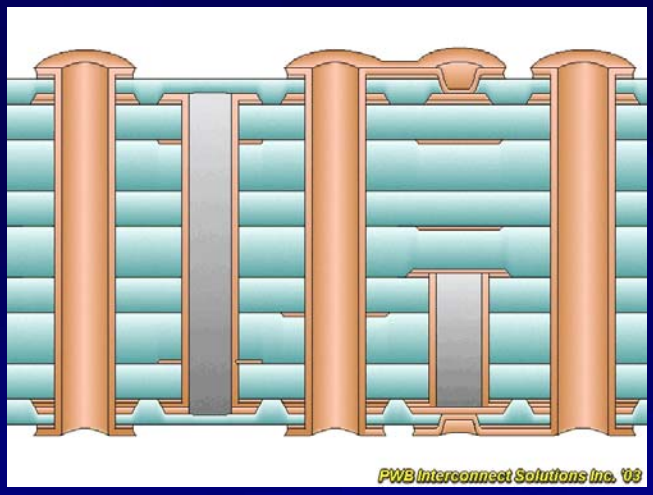
## Thermal Cycling – Cross Section Animation

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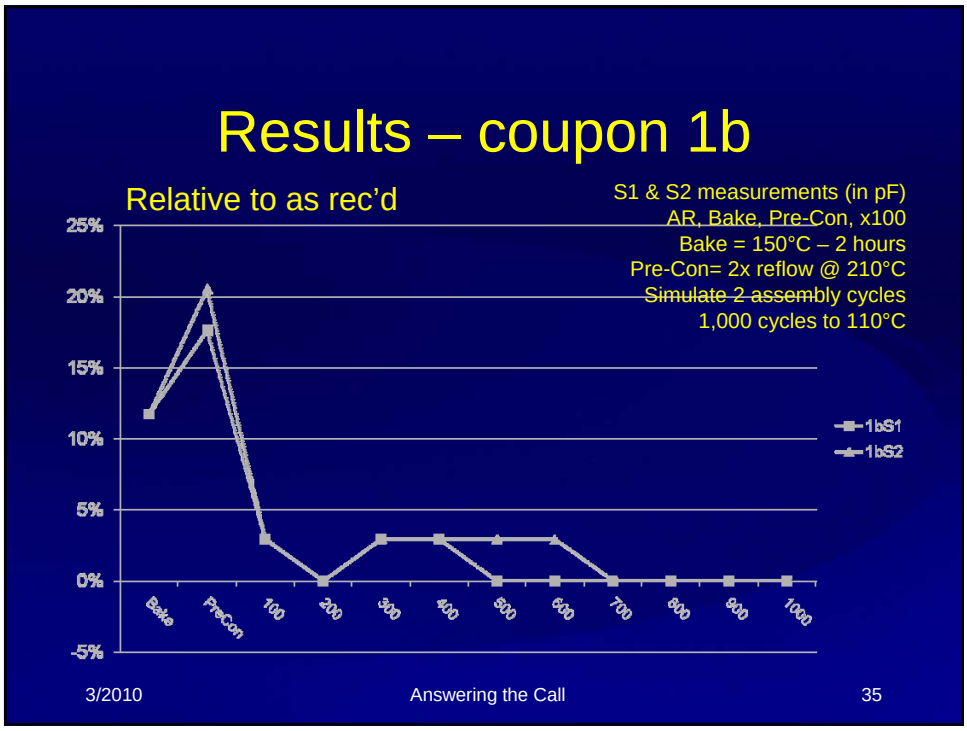
Results – coupon 1b
Relative to as rec'd
S1 & S2 measurements (in pF)
AR, Bake, Pre-Con, x100
Bake = 150°C – 2 hours
Pre-Con= 2x reflow @ 210°C
Simulate 2 assembly cycles
1,000 cycles to 110°C
25%
20%
15%
10%
5%
0%
-5%
Bake
PreCon
100
200
300
400
500
600
700
800
900
1000
1bS1
1bS2
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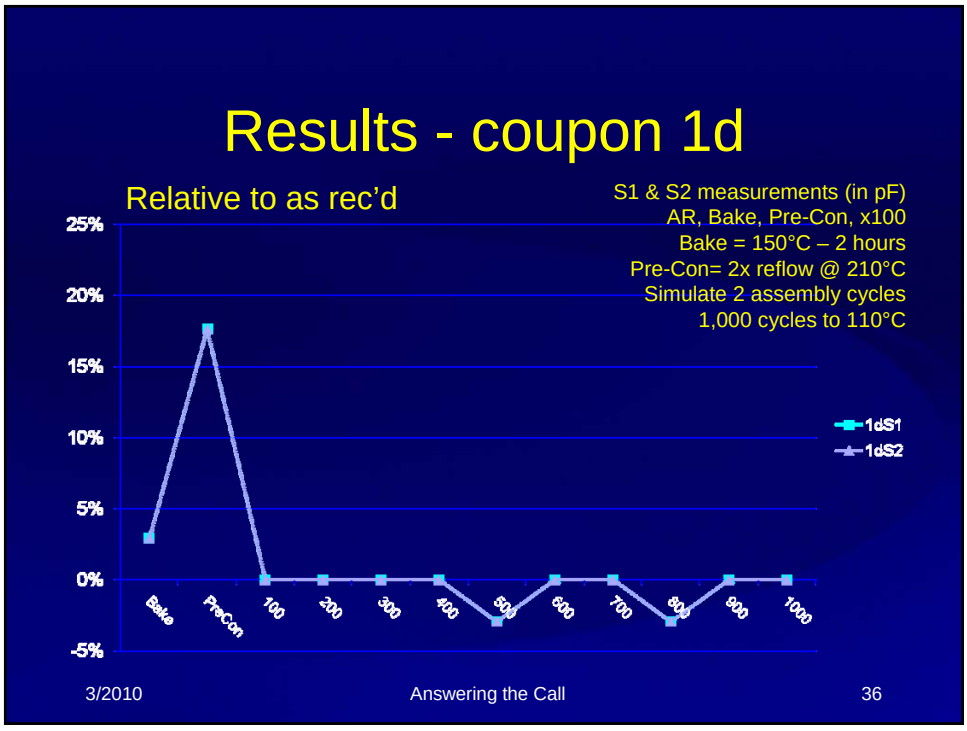
Results - coupon 1d
Relative to as rec'd
S1 & S2 measurements (in pF)
AR, Bake, Pre-Con, x100
Bake = 150°C – 2 hours
Pre-Con= 2x reflow @ 210°C
Simulate 2 assembly cycles
1,000 cycles to 110°C
25%
20%
15%
10%
5%
0%
-5%
Bake
PreCon
100
200
300
400
500
600
700
800
900
1000
1dS1
1dS2
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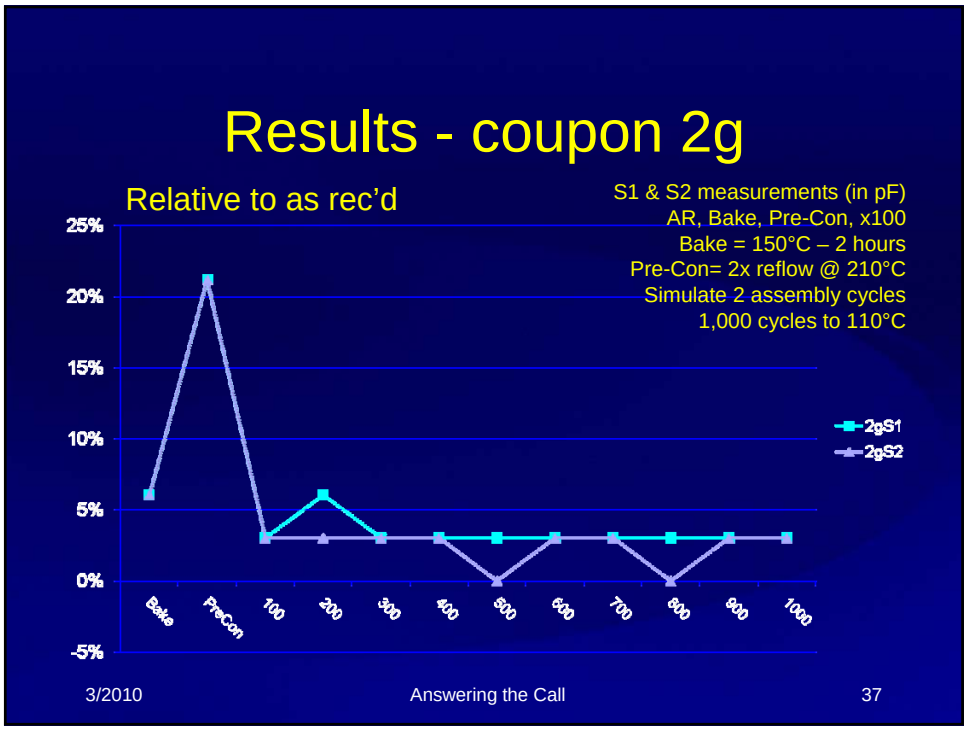
Results - coupon 2g
Relative to as rec'd
S1 & S2 measurements (in pF)
AR, Bake, Pre-Con, x100
Bake = 150°C – 2 hours
Pre-Con= 2x reflow @ 210°C
Simulate 2 assembly cycles
1,000 cycles to 110°C
25%
20%
15%
10%
5%
0%
-5%
Bake
PreCon
100
200
300
400
500
600
700
800
900
1000
2gS1
2gS2
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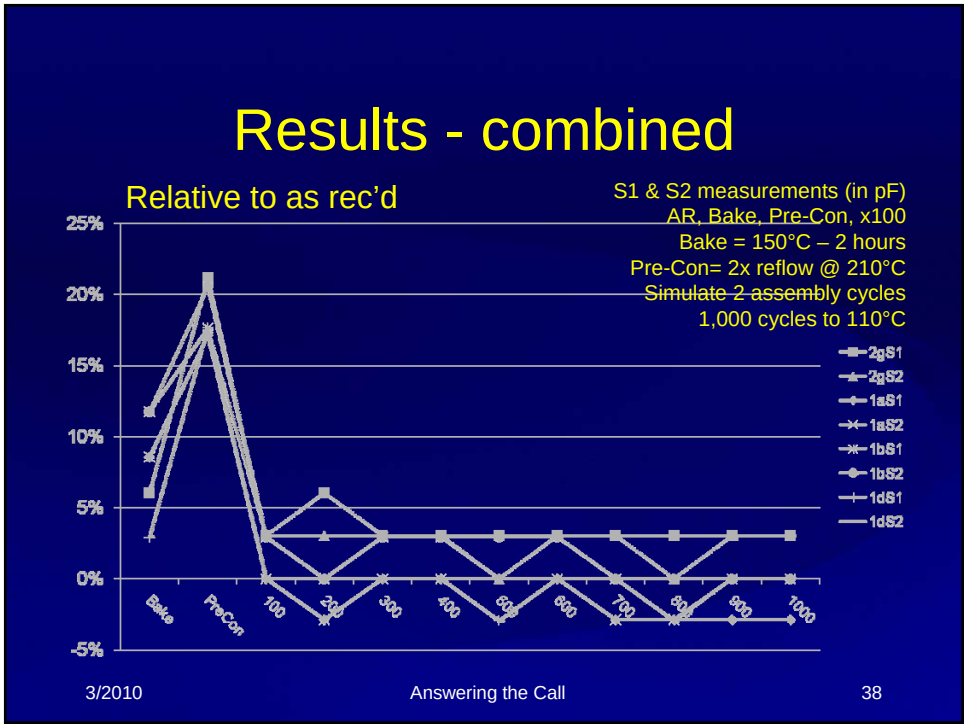
Results - combined
Relative to as rec'd
S1 & S2 measurements (in pF)
AR, Bake, Pre-Con, x100
Bake = 150°C – 2 hours
Pre-Con= 2x reflow @ 210°C
Simulate 2 assembly cycles
1,000 cycles to 110°C
25%
20%
15%
10%
5%
0%
-5%
Bake
PreCon
100
200
300
400
500
600
700
800
900
1000
2gS1
2gS2
1aS1
1aS2
1bS1
1bS2
1dS1
1dS2
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## Challenges

- Very complex contactor
  - Their words
  - Multiple pin dimensions
  - Factory maintenance a concern
  - Scalability
- How can the supply base address these concerns?
- How can we do this better?

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## Conclusions

- Answering the call!
- Removed the challenges
  - of the complex contactor
- Standard manufacturing processes
- Test results!

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## Acknowledgements


- Intel
  - Abram Detofsky
  - Omer Vikinski
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