BiTS Burn-in & Test Socket Workshop

2007 TUTORIAL

ARCHIVE 2007

TUTORIAL 1

"ATE PRINTED CIRCUIT BOARD DESIGN; PERFORMANCE VS. DESIGN FOR MANUFACTURABILITY VS. TIME TO TEST"

by

Steve Arobio – Chief Operating Officer, Dynamic Test Solutions

CURRENT PRINTED CIRCUIT BOARD design requirements have challenged the manufacturing processes to new limits. In the ATE industry in particular, test performance, signal speeds, multi-site device testing and shortened time to test demands have pushed the PCB Industry to more layers, tighter pitch, higher aspect ratios, exotic materials and customized processes. At times, the consequences have been poor yields, extensive test floor trouble-shooting, longer lead times and higher costs. This tutorial will address several of the performance drivers, along with the possible trade-offs associated with each of them, to give the Test Engineer a choice.

ATE PRINTED CIRCUIT BOARD DESIGN

DESIGN vs. MANUFACTURING CAPABILITIES

vs.

TIME TO MARKET

by

Steve Arobio

Dynamic Test Solutions

BiTS 2007 Tutorial

ATE PRINTED CIRCUIT BOARD DESIGN

- Printed Circuit Board Industry
- History of the Printed Circuit Board
- PCB Manufacturing Process:
  - Basic Building Blocks
- ATE Technology Challenges
- PCB Manufacturing Limitations
- Bridging the “GAP”

ATE PRINTED CIRCUIT BOARD DESIGN

- Automated Test Design
  - Technology Challenges
  - Cost Drivers
  - Design for Manufacturing
  - Sub-optimization

PRINTED CIRCUIT BOARD INDUSTRY

- World Wide Market
  - $50 Billion
- United States
  - $5 Billion
- Asia
  - $38 Billion
- Europe
  - $3.5 Billion
- Automated Test Equipment (ATE)
  - $500 Million
    - Wafer and Final Test = $300 Million
    - Burn-in Test = $200 Million

A BRIEF HISTORY OF THE PRINTED CIRCUIT BOARD (PCB)

- 1903: PCB first patented as a Printed Wiring Board.
- 1936: Dr Paul Eisler, an Austrian scientist working in England is credited with making the first printed circuit board to replace radio tube wiring, with something less bulky.
- 1943: US Army used printed circuit boards on a wide scale to make rugged radios for World War II.
- 1948: US released the PCB for Commercial use.

A BRIEF HISTORY OF THE PRINTED CIRCUIT BOARD (PCB) (cont.)

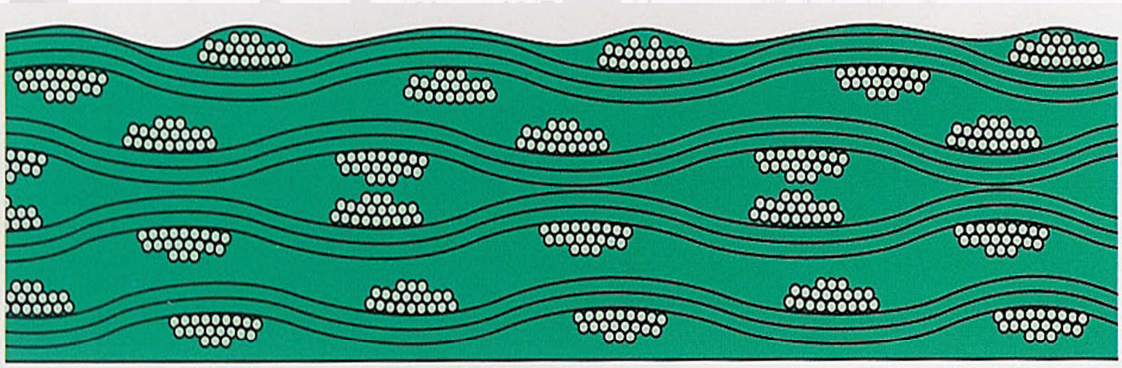
- 1950's - 1960's: Expanded use of single sided printed circuit boards.
- 1960's - 1970's: Processes were developed for adding copper to the walls of the drilled holes in the printed circuit boards, permitting top and bottom circuitry to be electrically connected.
- 1980's: Multilayer development to accommodate higher component densities and complexities.
- Today: Layer counts greater than 50 layers, device footprints less than .4mm, Environmental sensitivity.

THE PCB MANUFACTURING PROCESS

- Materials Release / *Shear*
  - Insulators / Dielectric Material
    - Base Laminate – Fully cured, glass reinforced resin impregnated composite material.
    - Pre-preg – Semi-cured (B-stage), glass reinforced resin impregnated composite material.
  - Critical Material Characteristics to Consider
    - Glass Transition (Tg): The temperature at which the resin turns from a "glassy" state to a plastic state. Operating above Tg results in expansion of the material, and in particular, in the Z-axis.
    - Dielectric Constant (Dk): Is the measure of the extent of a material to which it concentrates electrostatic lines of flux. It is the ratio of the amount of stored energy when a potential is applied, relative to the permittivity of a vacuum.
    - Loss Tangent: Also known as the dissipation factor, it is the ratio of the power loss in a dielectric material to the total power transmitted through the dielectric, the imperfection of the dielectric.

THE PCB MANUFACTURING PROCESS

Typical Laminate Construction



IPC-600g-222a

THE PCB MANUFACTURING PROCESS

- Materials Release / *Shear*
  - Insulators / Dielectric Material
    - Commonly Used Laminates

Material Type	Tg	Dk	Loss Tangent	Cost Factor
Standard FR-4	165 C	4.30	.0250 @ 1 MHz	1.0
High Temp. FR-4	180 C	4.50	.0035 @ 1 MHz	1.2
Polyimide	260 C	3.40	.0035 @ 1 MHz	1.5
Rogers 4003	280 C	3.55	.0027 @ 10 GHz	2.0
Rogers 4350	280 C	3.66	.0037 @ 10 GHz	2.0
Nelco 4000-6	175 C	4.30	.0230 @ 1 MHz	1.0
Nelco 4000-13	210 C	3.60	.0080 @ 10 GHz	1.2
Nelco 4000-13SI	210 C	3.20	.0070 @ 10 GHz	1.5
Arlon 25 N	260 C	3.38	.0025 @ 10 GHz	N/A
Speedboard C	220 C	2.60	.0038 @ 3 GHz	N/A

THE PCB MANUFACTURING PROCESS

- Materials Release / *Shear*
  - Conductive Material
    - Copper foil
      - Electro-deposited (ED)
      - Rolled and Annealed (RA)
    - Typical Foil Thicknesses
      - ½ oz .0007”, 18 micron
      - 1 oz .0014”, 35 micron
      - 2 oz .0028”, 71 micron
      - 4 oz, 7 oz, 10 oz for high current applications

THE PCB MANUFACTURING PROCESS

- Inner Layer Patterning: *Image*
  - Surface Preparation: Promotes adhesion of the Photoresist.
  - Photoresist Lamination: Negative acting photo polymer.
  - Exposure:
    - Conventional: Light source utilizing silver based or diazo photo-mask.
    - Laser Direct Imaging: CAD data output directly imaged onto the resist coated panel.
  - Aqueous Developing: "Washing" away of the non-polymerized photoresist.

THE PCB MANUFACTURING PROCESS

- Inner Layer Patterning: *Etching*
  - Etching: Conveyorized operation to selectively remove the base copper not protected by the dry film photoresist.
    - Cupric Chloride Etching Chemistry
    - Ammonia Etching Chemistry
  - Stripping: Conveyorized operation to remove the dry film photoresist protecting the copper pattern.
    - High pH Chemistry
- Automated Optical Inspection (AOI)

THE PCB MANUFACTURING PROCESS

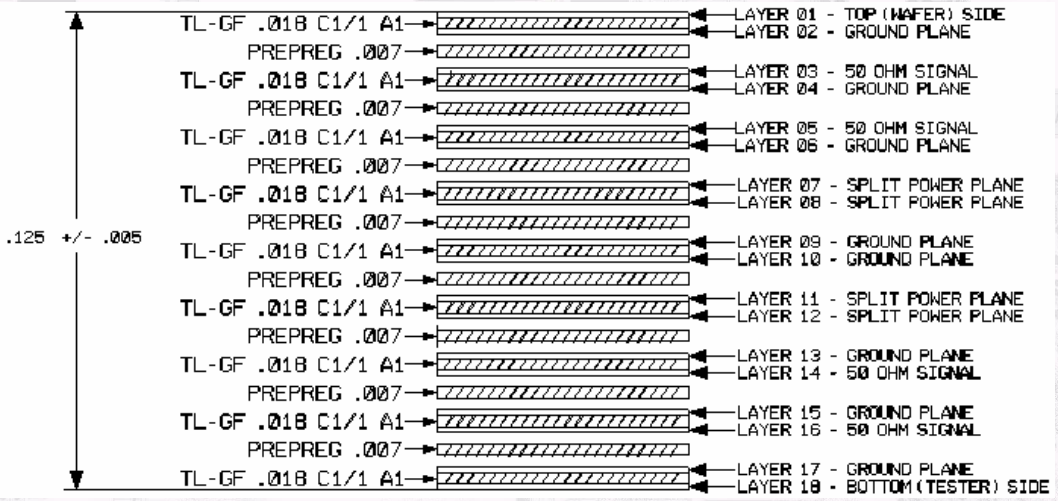
- Multilayer Lamination
  - Surface Preparation and Treatment: Cleaning of the individual completed cores.
    - Promotes Adhesion and Bond Strength
  - Lay-up: Sometimes referred to as “Booking”, the stacking of the cores, alternating layers with pre-preg, between lamination plates.
    - In accordance with the Lay-up Sheet or the PCB Manufacturer’s Lay-up Construction.
    - Copper Foil for Outer Layers.
  - Registration: Maintaining layer to layer alignment.
    - Pin-lamination: Layer to layer alignment is maintained by pinning to post-etch, optical punched holes.
    - Riveting: Pin-less alignment using artwork defined targets and rivets.

THE PCB MANUFACTURING PROCESS

- Multilayer Lamination
  - Lamination: The application of heat and pressure to the “Book” to cause the pre-preg to flow, drive out air, and bond the layers together.
    - Lamination Temperature is dependent on the material type.
    - Pressure is adjusted based on Panel Size, Layer Count, Copper Weight and Board Lay-out.
    - Cure Cycle is critical for lamination integrity.

THE PCB MANUFACTURING PROCESS

Example of a Typical Multilayer Construction

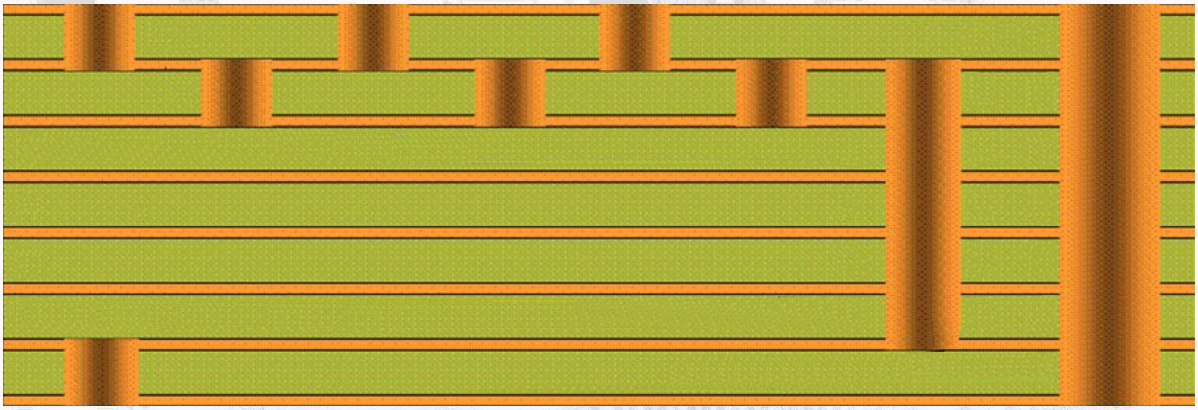


THE PCB MANUFACTURING PROCESS

- Drilling
  - Mechanical
    - Larger than .004” Drill Diameter
    - Mechanical positioning
  - Laser
    - Smaller than .005” Drill Diameter
    - Micro-vias
      - .002” - .003”
    - Optical positioning
  - Types
    - Through Holes
    - Blind Vias
    - Buried Vias
    - Back Drill or Stub Drill

THE PCB MANUFACTURING PROCESS

Examples of Drilled Holes



THE PCB MANUFACTURING PROCESS

- Smear Removal / Etchback: The process which removes resin residue from the inner layer interconnections.
  - Melted resin from the high-speed drilling operation.
    - Chemical Process using Chromic or Sulfuric Acid
    - Plasma using Fluorine and Oxygen Gases
- Electroless Copper Deposition: The “Seeding” of the drilled hole wall with a thin coating of copper.
  - 30-40 micro-inches

THE PCB MANUFACTURING PROCESS

- Outer Layer Patterning: *Image*
  - Surface Preparation
  - Photo Resist Lamination
  - Exposure
  - Aqueous Developing

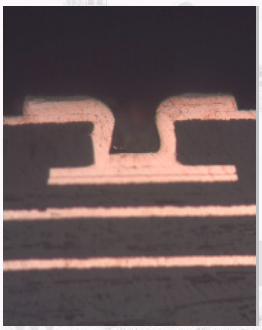
THE PCB MANUFACTURING PROCESS

- Electro-plating Process – *Copper Plate*
  - Requires Rectification
  - .001” minimum thickness required
  - Aspect ratio: Relationship between the diameter of the drilled hole and the total thickness of the material being plated.
    - Through Holes: 15:1
    - Buried: 15:1
    - Blind1:1
    - Micro-vias: 1:1
- Electro-plating Process - *Etch Resist*
  - Tin: Lead free etch resist.
  - Electro-plated Nickel and Gold: Final surface finish for ATE.
  - Tin-Nickel: Final surface finish for Burn-in Boards.
  - Tin-Lead: Popular final surface finish prior to ROHS.

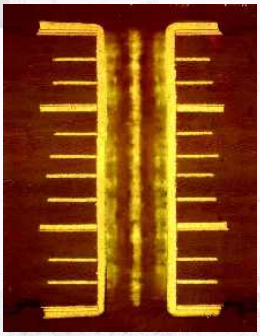
THE PCB MANUFACTURING PROCESS

Examples of Plated Holes

Micro-via



Plated Through Hole

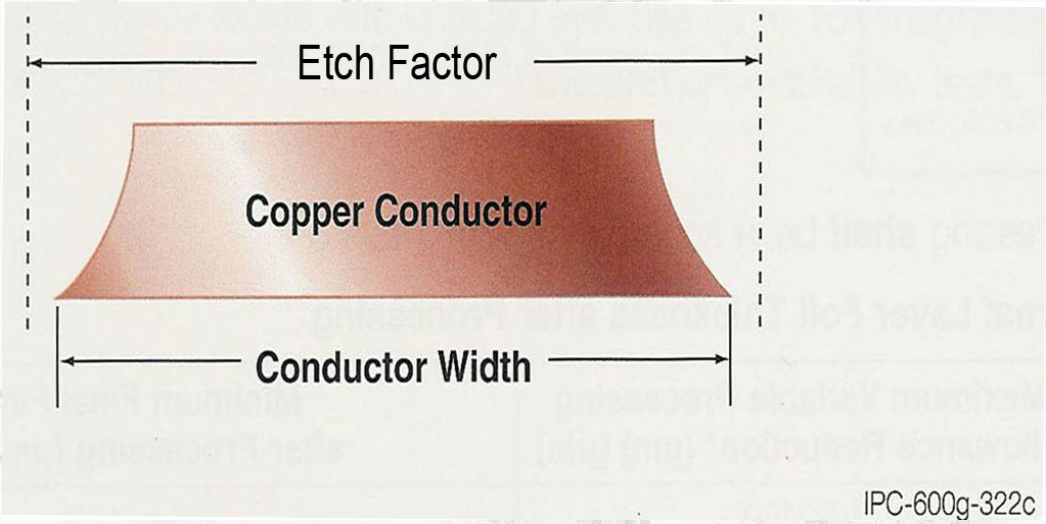


THE PCB MANUFACTURING PROCESS

- Outer Layer Patterning: *Strip and Etch*
  - Strip Photoresist
  - Etching
    - Etch Factor: A compensation of the trace width to allow for process loss.
      - ½ oz. copper = .0005”
      - 1 oz. copper = .001”
      - 2 oz. copper = .002”
- Pre-mask Electrical Test
  - Bare Board
  - Flying Probe
    - Cost effective for small production lots.
    - Minimal set-up.

THE PCB MANUFACTURING PROCESS

Etch Factor



THE PCB MANUFACTURING PROCESS

- Solder Mask: a coating applied over the outer layer circuitry, with clearances around the pads to facilitate the component assembly operations.
  - Provides protection
  - Reduces Assembly related defects.
    - Solder Bridges
  - Provides an air tight seal for Vacuum applications.
- Applications.
  - Liquid Photo-imageable (LPI)
- Dry Film
- Non-conductive Via plug

THE PCB MANUFACTURING PROCESS

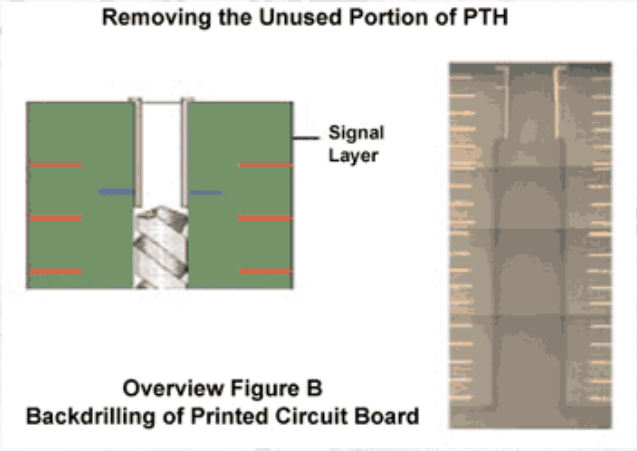
- Surface Finishes
  - Electroplated Nickel and Gold
    - Etch Resist
    - 30–50 micro-inches over 150-300 micro-inches nickel
    - Robust finish for wear and resists oxidation
  - Hot Air Solder Level(HASL)
    - Most popular Surface Finish for Component Assembly
    - .0003” - .001”
    - Environmental Hazard - Lead
  - Electroless Nickel and Immersion Gold
    - 200 Micro-inches Nickel / 2-5 micro-inches Gold
  - White Tin Immersion
  - Immersion Silver
    - Special Handling
  - OSP
    - Short Shelf Life

THE PCB MANUFACTURING PROCESS

- Profiling: The machining operations that remove the PCB from the production panel.
  - NC Routing
  - Second Drilling
  - Machined Slots
  - Counterbores
  - Countersinks
  - Back Drill / Stub Drilling

THE PCB MANUFACTURING PROCESS

Back Drilling / Stub Drilling



THE PCB MANUFACTURING PROCESS

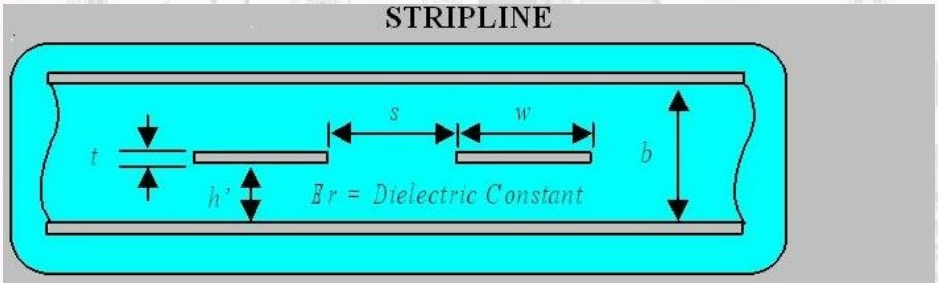
- Quality Assurance: *Final Inspection*
  - Visual Inspection
    - Cosmetic defects
  - Electrical Test
    - Opens, Shorts, Leakage
  - Impedance Testing
    - TDR
  - X-ray Fluorescence
    - Surface Finish Thickness Verification
  - Micro-section Examination
    - Plating Integrity
    - Lamination Integrity
  - Temperature Cycling
    - Assembly Simulation

ATE Technology Challenges

- Impedance
  - Modeling
    - Trace width
    - Dielectric spacing
    - Dielectric constant
  - Manufacturing Challenges
    - Image
    - Etching
    - Lamination
    - Tolerance Stacking

ATE Technology Challenges

Example of an Impedance Model



Enter the Following Values:			Results		
Er=	4.50	Impedance Zo[Ohm] =	51.03	Tr [nsec]=	1
t (mils)=	0.70	Differential Zdf [Ohm] =	89.32	Swing [V]=	5
w (mils)=	8.00	Resistance [mOhm]/Inch =	122.31	XTmax [V]=	1.05839248
s (mils)=	8.00	Propagation Delay [psec]=	719.00		
h' (mils)=	11.00	Capacitance Co [pF]=	14.09		
b (mils)=	22.7	Inductance Lo [nH]=	36.69		
Trace Length (in)=	4			Misc	0.71899523

ATE Technology Challenges

- Circuit Traces / Spaces
  - Less than .004” / .004”
- Layer Counts
  - Greater than 30, 40, 50 layers
- Final Board Thickness
  - Greater than .250”
- Aspect Ratio
  - 20:1
- Drilled Hole to Copper Spacing
  - Less than .005”
- Flatness and Coplanarity
  - .005” per inch
- Cosmetics

ATE Technology Challenges

- Today's ATE Design Expectations are out-pacing the PCB Manufacturing Capabilities.
  - Technology
  - Reliability
  - Cost
  - Lead-times

PCB Manufacturing Limitations

- Why "The GAP"?
  - Relatively Unsophisticated Business
    - Most start-ups by PCB employee turned entrepreneur
  - Lower Education Requirements and Relatively Untrained Work Force
  - High Capital Requirement
    - Start Up and Annual Technology Upgrades
  - Environmental / Safely Considerations
    - EPA, OSHA, Local Regulations
  - Offshore Competition
    - Cheap Labor
  - PCB Process virtually unchanged over the past 30 years

Bridging "The Gap"

- Process Engineering and Innovation
- Design for Manufacturing
- Equipment
- New Processes

Bridging "The Gap"

- Process Engineering and Innovation
  - First Article Run
    - Results are un-predictable
    - Extends cycle time
- Process Control Through:
  - Process Engineering Team
  - Resident Expert
  - Excessive Overage
    - Not always repeatable
    - Adds significant cost

Bridging "The Gap"

- Equipment
  - Drilling
    - Single Spindle Machines
      - Allow for more flexibility on small manufacturing lots.
    - Higher Spindle Speeds
      - Facilitate small hole drilling.
    - Accuracy
      - Drill run-out and Electronic QC checks are performed in Real Time.
    - Laser
      - Makes possible the efficient drilling of tens of thousands of very accurately placed micro-vias.
  - Image
    - Trace/Space below .005" / .005"
    - Laser Direct Imaging
      - Improved Accuracy; No Artwork Required; Finer Traces / Spaces.
  - Plating
    - Reverse Pulse-Plating Rectification
    - Chemistry Improvements for High Aspect Ratio Holes

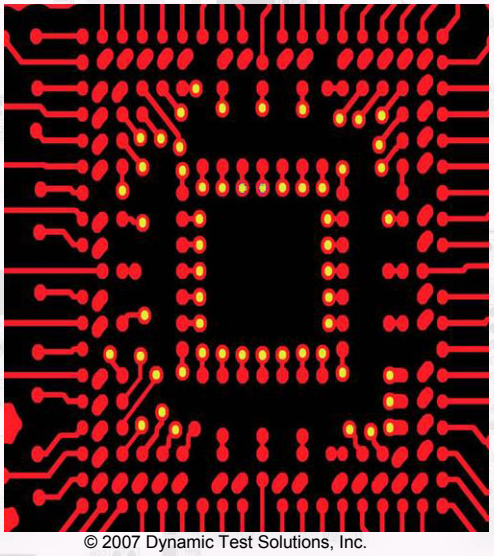
Bridging "The Gap"

- New Processes
  - Micro-via
    - Less reliance on high aspect ratio drilling / plating
    - Multiple laminations possible with-out compromising registration
    - Higher process cost / Lower reject cost
    - Gain "real estate" for routing traces
  - Filled Via or Via in Pad
    - Gain "real estate" for routing traces in tight areas.
  - Reliance on Automation in Inspection / QA
    - Electrical Test
  - CAM Engineering Automation
    - Scripting of Design Rule Checks (DRC) for manufacturing optimization.

Bridging "The Gap"

Micro-via Design "Strategy"

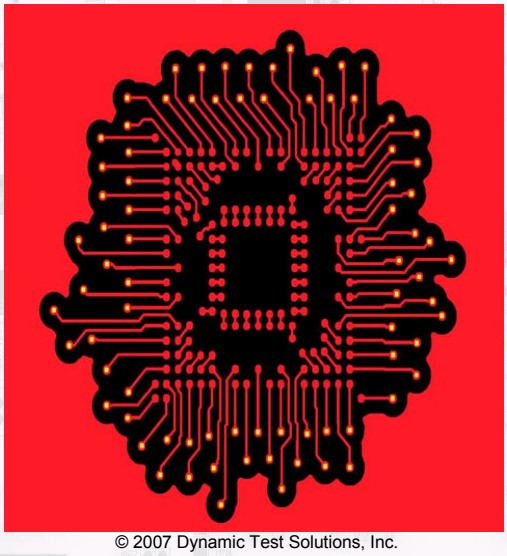
Via Locations with-in the DUT



Bridging "The Gap"

Micro-via Design "Strategy"

Via Locations outside of the DUT



Automated Test Design

- Technology Challenges
  - Device Pitch
    - .5mm, .4mm, .3mm
  - Overall Board Thickness
    - Greater than .250”
  - Large Board Size
    - Greater than 18” x 24”
  - Impedance Tolerances
    - Less than +/- 10 %
  - Surface Finishes
    - Selective Plating Processes
  - Total Time to Test
    - 5 Weeks: Inclusive of Design, Fabrication and Assembly

Automated Test Design

- Cost Drivers
  - Trace / Spacing , less than .004” / .004”
    - Yields
  - Impedance requirements of 5% or less.
    - Is it really required?
      - The ATE industry is not consistent on this.
    - Is it required on all layers and on all signals?
  - Board Thickness greater than .250”.
    - Handling Challenge
    - Conveyorized processing equipment is set up for thick panels and cannot reliably process thin cores.
    - Z-axis Expansion

Automated Test Design

- Cost Drivers
  - Core Thickness less than 004".
    - Handling Challenges
  - Multiple Surface Finishes
    - Add process steps to an already lengthy manufacturing process, and when the panels are 70%-80% complete.
  - Aspect ratio > 15:1
    - Longer plating times
  - Blind, Buried, Micro-vias
    - Additional process steps

Automated Test Design

- Cost Drivers
  - Mixed Materials
    - Different process parameters
    - Different dimensional stability
  - Panel sizes > 18 x 24
    - Poor material utilization
  - Via in Pads
    - Extra Process steps required.
  - Non-standard Materials
    - Unbalanced copper weights
    - Lead times, Minimum Lot Purchases

Automated Test Design

- Cost Drivers
  - Machining Counter bore, Countersink, Slots, Non Plated Holes
    - +/- .001” Tolerances
  - Back Drilling

Automated Test Design

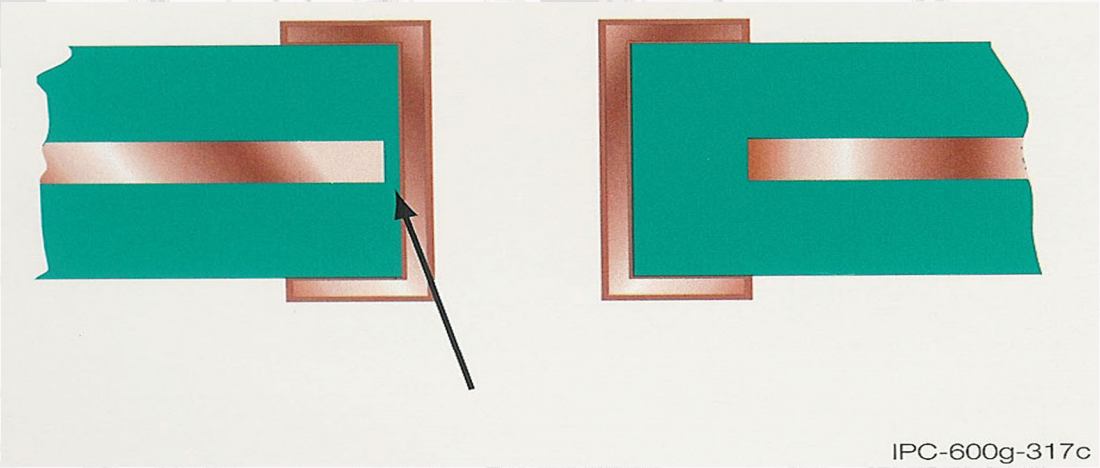
- Cost Drivers: < .8mm Device Pitch
  - Yields! The customer eventually pays for the cost of the yield loss.
    - Higher Board Costs.
    - Manufacturer goes out of business.
    - Tester time is lost waiting for PCB's.

Automated Test Design

- Cost Drivers: Yield Loss
  - Minimum Drilled Hole to Copper Feature: *the minimum spacing from the drilled hole wall to any internal copper feature; circuit or plane.*
    - This is not the same as Air Gap or Minimum Spacing!
    - Yield loss is electrical shorts or electrical leakage.
  - Z-Axis Expansion: *the movement that occurs in the Z-axis direction after the PCB material is exposed to thermal excursion.*
    - Assembly operation.
    - Yield loss is due to intermittent electrical connection due to copper barrel cracking.

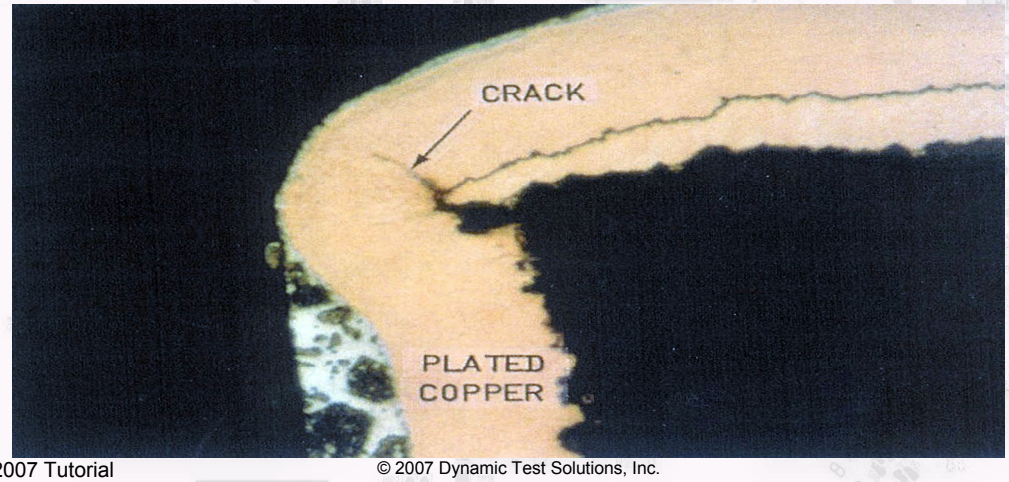
Automated Test Design

Minimum Drilled Hole to Internal Copper Feature



Automated Test Design

Poor Plated Thru Hole Integrity as a Result of Excessive Z-axis Expansion



Automated Test Design

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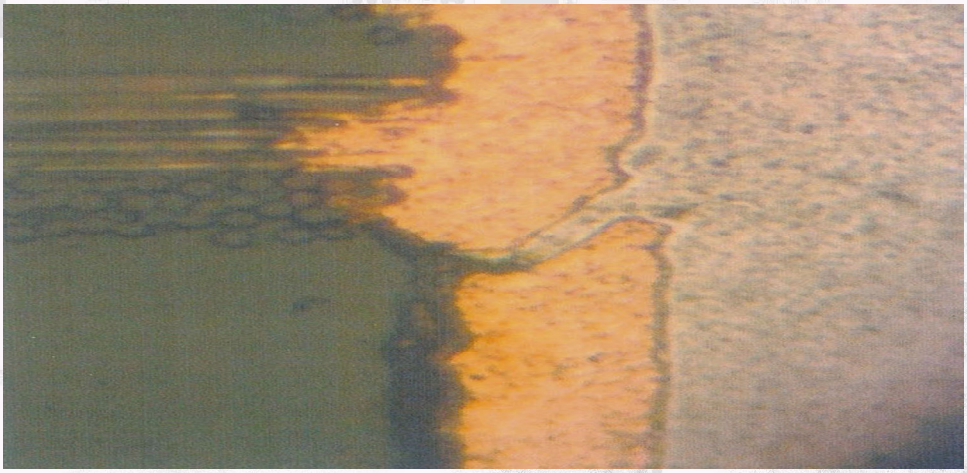

Automated Test Design

- Cost Drivers: Yield Loss
  - Cosmetics
    - Nodules, Scratches, Soldermask Adhesion
    - Gold Finish
    - Outer Layer Planes
  - Flatness < .005” per inch
    - Probe Card Designs Pushing .001”- .002” per Inch

DESIGN FOR MANUFACTURING

- Design Parameters that Drive Manufacturing
  - Device Pitch
    - Blind, Buried, Micro-vias
      - Multiple laminations
      - High aspect ratios
  - Component Volumes
    - Routing strategy as it relates to layer count
      - Real Estate
      - Traces and Spaces

DESIGN FOR MANUFACTURING

- Design Parameters that Drive Manufacturing
  - Frequency / High Temperature
    - PCB Board Material
    - Mixed Dielectrics
    - Stock vs. Build to Order
      - Price
  - Decoupling
    - Manufacturing vs. Assembly
      - Size of capacitors
      - Power distribution
      - Stacking of caps

SUB-OPTIMIZATION

- Design vs. Manufacturing: *the Trade-offs*
  - Wrong Component Selection
    - Selected a .4mm thru hole socket requiring an .008” finished hole size.
      - Design requirements
        - » .0038” Drilled Hole to Copper
        - » .002” Trace / .003” Space
        - » .0005” to .0007” Minimum Copper Plating
      - Unpredictable Outcome

SUB-OPTIMIZATION (cont.)

- Design vs. Manufacturing: *the Trade-offs*
  - Component Requirement: Quantity
    - Quantity of components required vs. physical board size and available space for the routing of traces.
      - » Will not fit in available space due to component spec driving board thickness which then drives layers available.
      - » Could use component finger cards but customer would not allow it.
    - Customer was forced to remove hundreds of parts

SUB-OPTIMIZATION (cont.)

- Design vs. Manufacturing: *the Trade-offs*
  - Maintain Existing Test Program
    - Design Required to go from a 4-site to an 8-site
      - Design Requirements
        - » Increase layer count by 21 layers!
        - » Board thickness becomes a challenge.
        - » Maintaining existing trace width is not possible.
      - The costly solution was to increase the board thickness to .250", allow best fit routing to keep trace width requirements for analog and digital signals.

SUB-OPTIMIZATION (cont.)

- Design vs. Manufacturing: *the Trade-offs*
  - Trace Width Requirement
    - Design Required .010” trace width routing into the DUT foot print and a dedicated pin list, affecting 4000 signals.
      - Design Requirements
        - » Hole to copper violations.
        - » Trace width gets set based on layer count and core thickness available to support the manufacturing.
        - » Repeated late deliveries due to poor manufacturing yields.
      - The solution was to minimize .010” trace routing, using “best fit” on four signal layers only, and reduce trace width routing on all other routs.

DTS, Inc.

- **Dynamic Test Solutions, Inc.**
  - **Founded in 2003 by a few individuals with a vast experience in the semiconductor ATE design business.**
  - **DTS supports design, fabrication and assembly of custom and generic PCB's for wafer and package test applications.**
  - **DTSA**
    - **Started in 2005**
    - **Headquarters in Singapore**
    - **Satellite offices in China, Taiwan, Thailand, Philippines, Malaysia**
  - **DTSE**
    - **Started in 2006**
    - **Headquarters in Paris, France**
    - **Satellite offices in Germany, UK, Italy**