# 2007 HOT TOPICS

## ARCHIVE 2007

## ADVANCEMENTS IN CONTACTING LEADING EDGE PACKAGES

### "Novel Low Cost Test and Burn-in of Wafer Level Packaging"

**Belgacem Haba, Ph.D., David Ovrutsky, Guilian Gao, Ph.D., Vage Oganesian**
Tessera, Inc.

### "A New Probe Card Approach for Wafer Level Chip Scale Package Testing"

**Norman J. Armendariz, Ph.D.**
Texas Instruments, Inc.

### "POP Rocks: Approaches to Socketing Package-on-Package Devices"

**Jon Diller, Kiley Beard, Jamie Andes**
Interconnect Devices, Inc.

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# Novel Low Cost Test and Burn-in Wafer Level Packaging

**2007 Burn-in and Test Socket Workshop**
**March 11 - 14, 2007**

Belgacem Haba, Ph.D., David Ovrutsky
Guilian Gao, Ph.D. and Vage Oganesian
Tessera, Inc.

## Agenda

- Background
- Wafer Level Packaging and why?
- What needs to be done?
- Results
- Conclusion

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## Agenda

- Background
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- Conclusion

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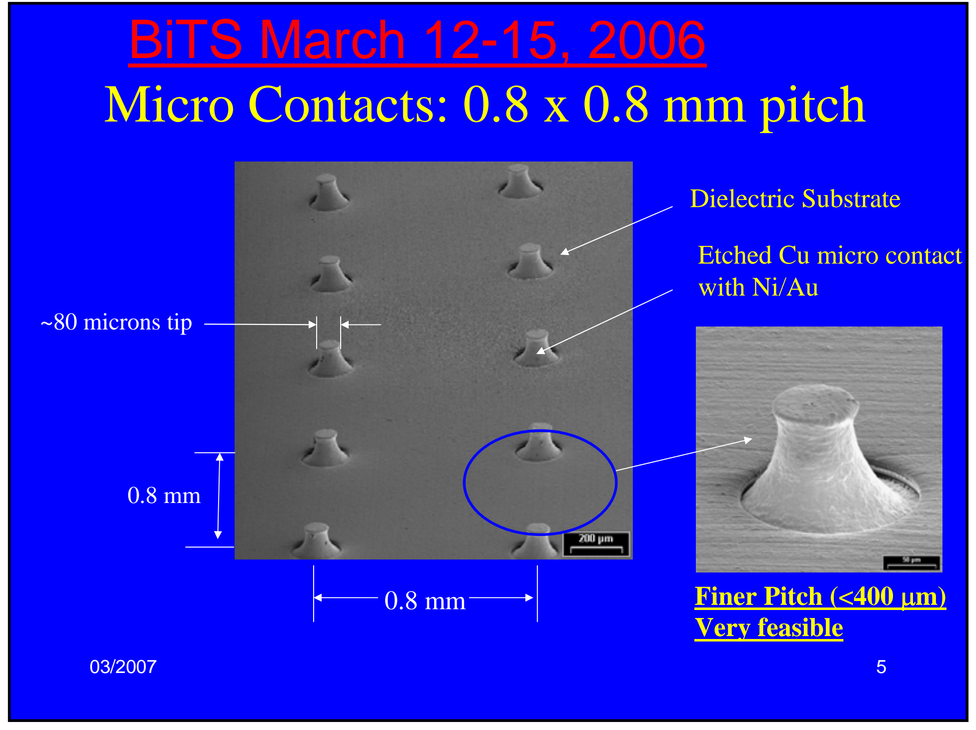
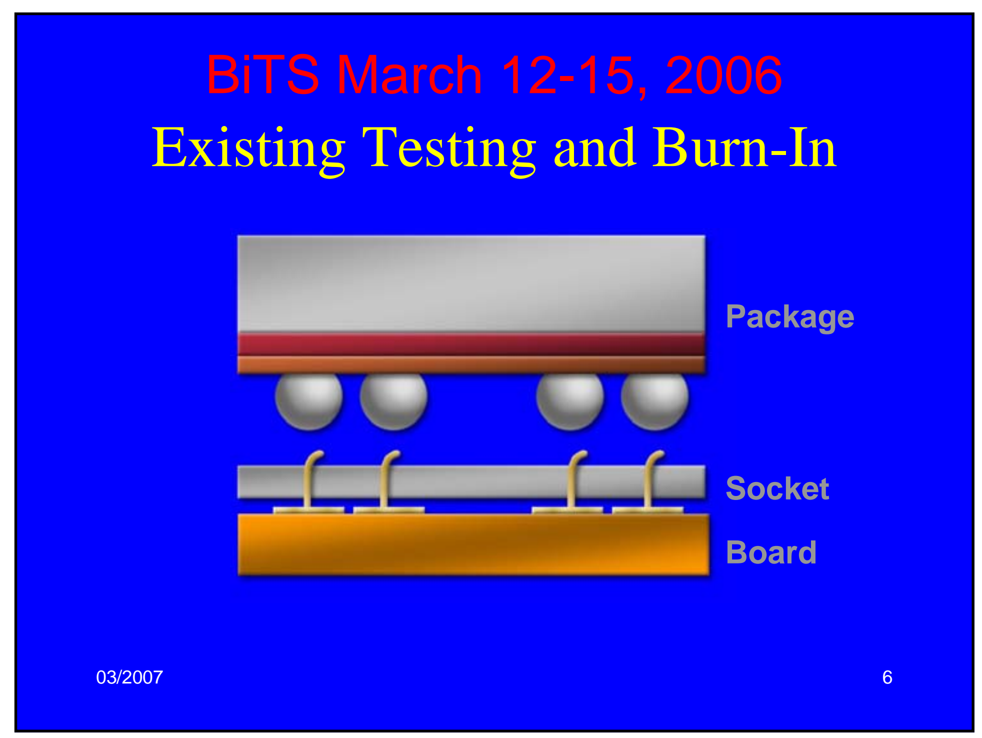
BITS MARCH 12 – 15, 2006

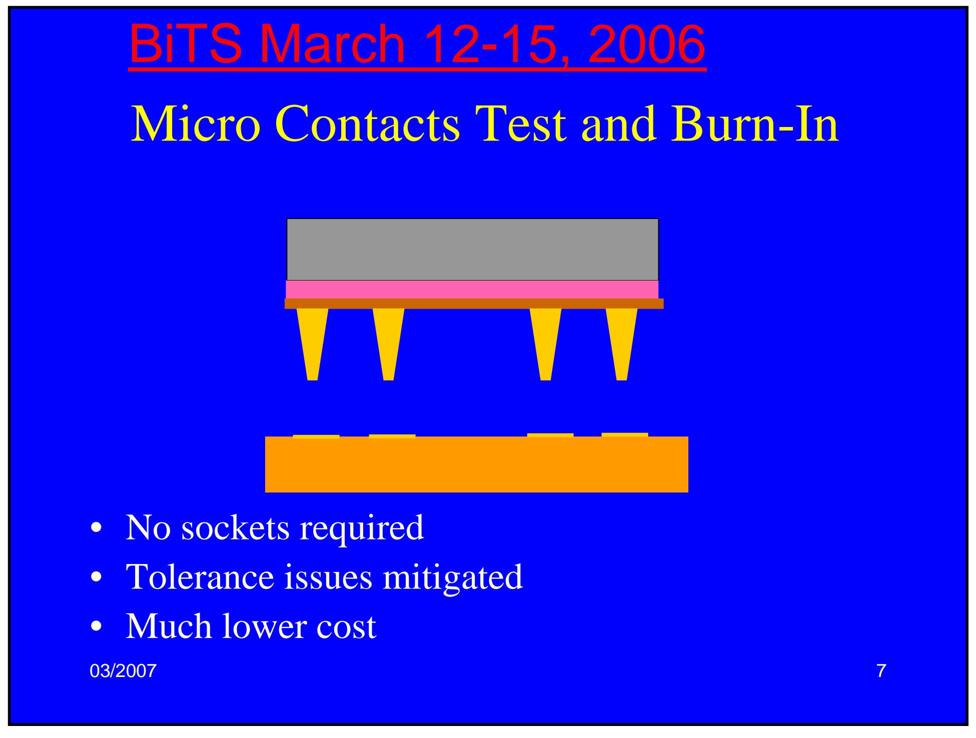
# Are Sockets Required for Test and Burn-in ?

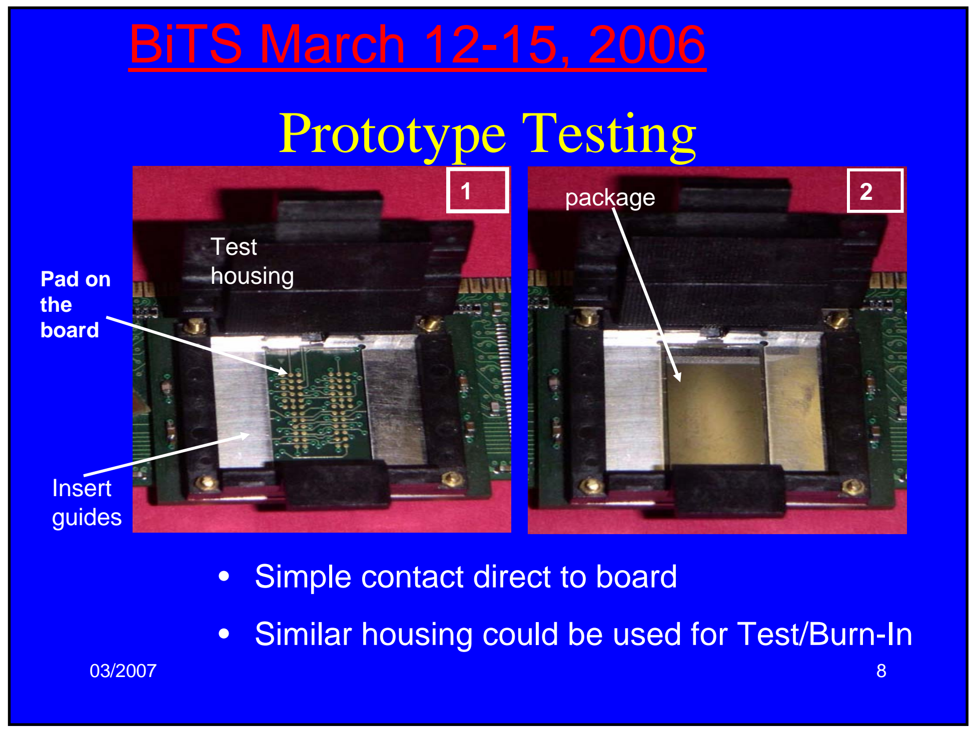
2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Belgacem Haba, Ph.D.
Tessera, Inc.


BiTS March 12-15, 2006
Micro Contacts: 0.8 x 0.8 mm pitch
Dielectric Substrate
Etched Cu micro contact
with Ni/Au
~80 microns tip
0.8 mm
0.8 mm
Finer Pitch (<400 µm)
Very feasible
03/2007
5


BiTS March 12-15, 2006
Existing Testing and Burn-In
Package
Socket
Board
03/2007
6


BiTS March 12-15, 2006
Micro Contacts Test and Burn-In
No sockets required
Tolerance issues mitigated
Much lower cost
03/2007
7


BiTS March 12-15, 2006
Prototype Testing
1
Test housing
Pad on the board
Insert guides
package
2
Simple contact direct to board
Similar housing could be used for Test/Burn-In
03/2007
8

BiTS March 12-15, 2006

## Summary

- Introduction of micro contact technology
- Scalability to fine pitch and high I/O
- Cost reduction path for test & burn-in
- Versatile approach can be leveraged in many applications
- Stay tuned……….

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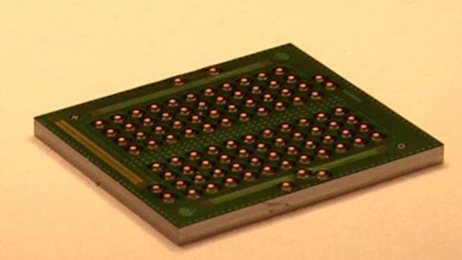
## We are proposing a socket-less Wafer Level Test and Burn-in



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## Agenda

- Background
- **Wafer Level Packaging (WLP) and why?**
- What needs to be done?
- Results
- Conclusion

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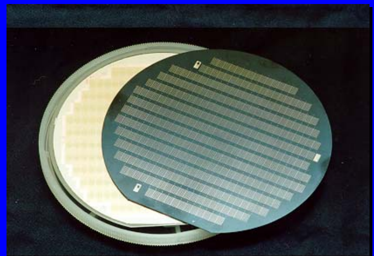
## WLP Promise

- Low Cost
- High parallelism
- Merge front end and back end
- Minimize component handling
- Test and burn-in in a wafer form



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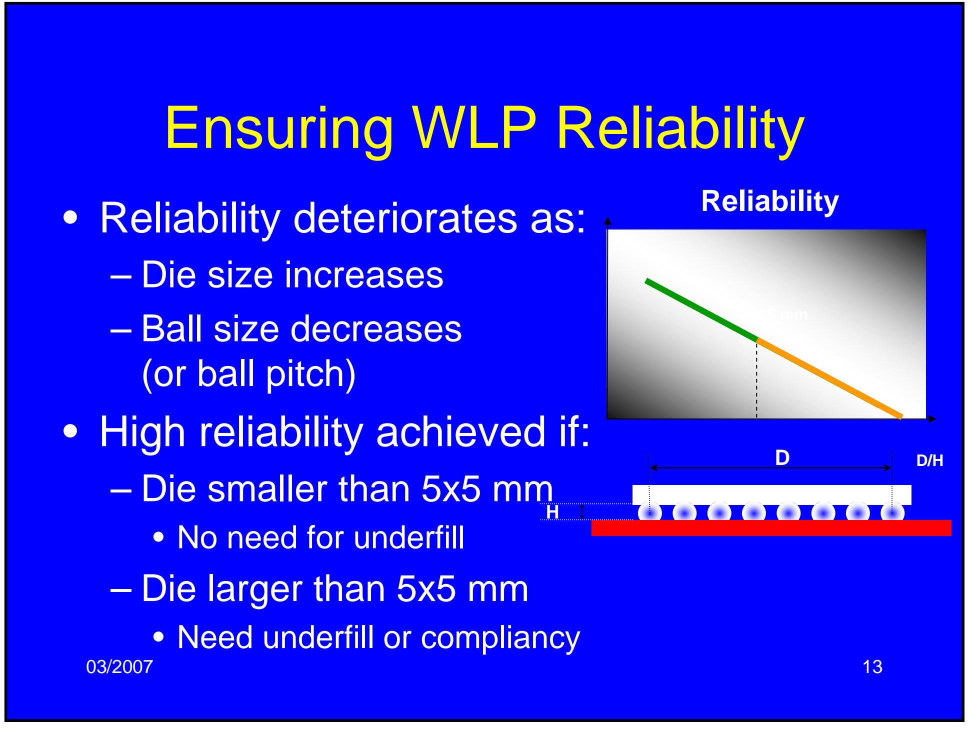
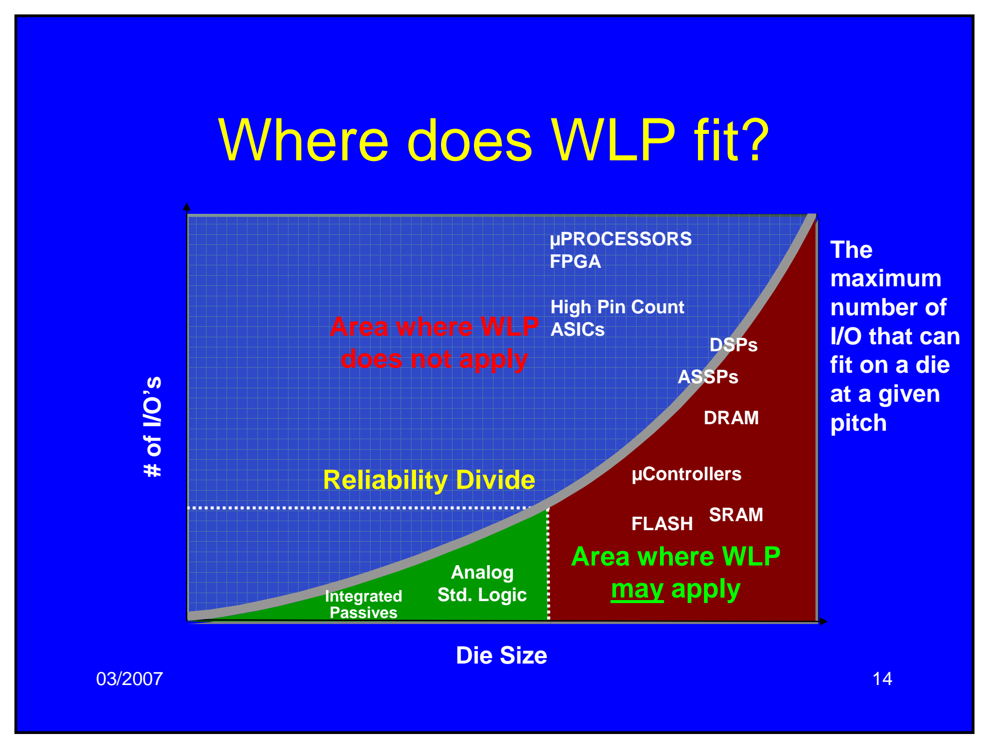

Ensuring WLP Reliability
• Reliability deteriorates as:
– Die size increases
– Ball size decreases
(or ball pitch)
• High reliability achieved if:
– Die smaller than 5x5 mm
• No need for underfill
– Die larger than 5x5 mm
• Need underfill or compliancy
Reliability
D
D/H
H
03/2007
13


Where does WLP fit?
µPROCESSORS
FPGA
High Pin Count
ASICs
Area where WLP
does not apply
DSPs
ASSPs
DRAM
Reliability Divide
µControllers
FLASH
SRAM
Area where WLP
may apply
Analog
Std. Logic
Integrated
Passives
# of I/O's
The maximum number of I/O that can fit on a die at a given pitch
Die Size
03/2007
14

# High Volume WLP Today

- Simple redistribution layer with solder bump
- Mainly used for very small die, low I/O (analog, integrated passives, power MOSFETS)
  - Very low cost; 1000s die per wafer
- Limited because of reliability issues above 5x5 mm die size

Flip Chip Technologies UltraCSP

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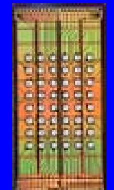
# WLP Challenges

Established wire bonding infrastructure

- Assembly Infrastructure
- Reliable larger die
- Test infrastructure

10,000's per wafer

100's per wafer



- RDL, bumping capacity increasing
- 300 mm WLP more cost effective
- Compliant WLP is reliable
- Oxide-free, compliant contact enables test
- Die shrink remains an issue

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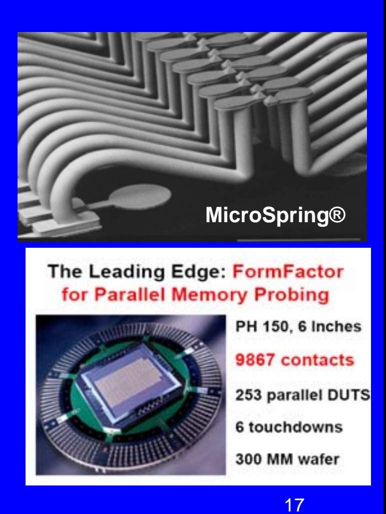
## Form Factor Wafer Probe

- Wafer Probe Cards
- 6” and 8” wafers
  - DRAM
  - Flash
  - Microprocessors
- Technology based on MicroSpring®

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## Aehr Test--Test/ BI Partner

- Aehr Systems have available test and burn-in systems
  - Based on wafer cassettes
  - Use contactors interposer between wafer and board
  - Up to14 wafers per load

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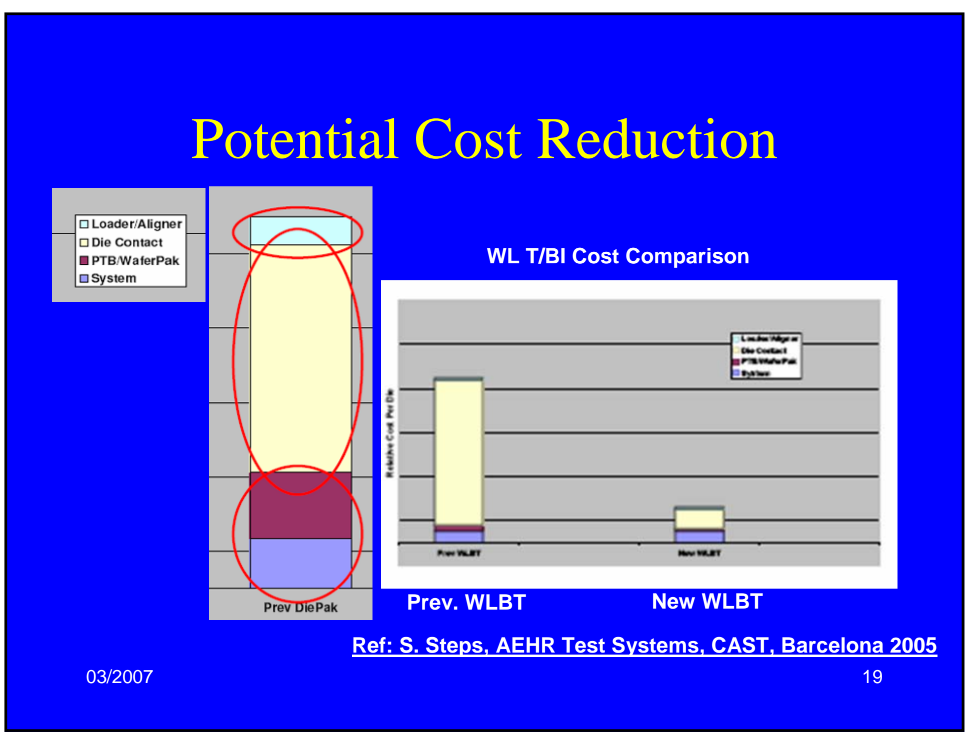


## Agenda

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- Wafer Level Packaging and why?
- **What needs to be done?**
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- Conclusion

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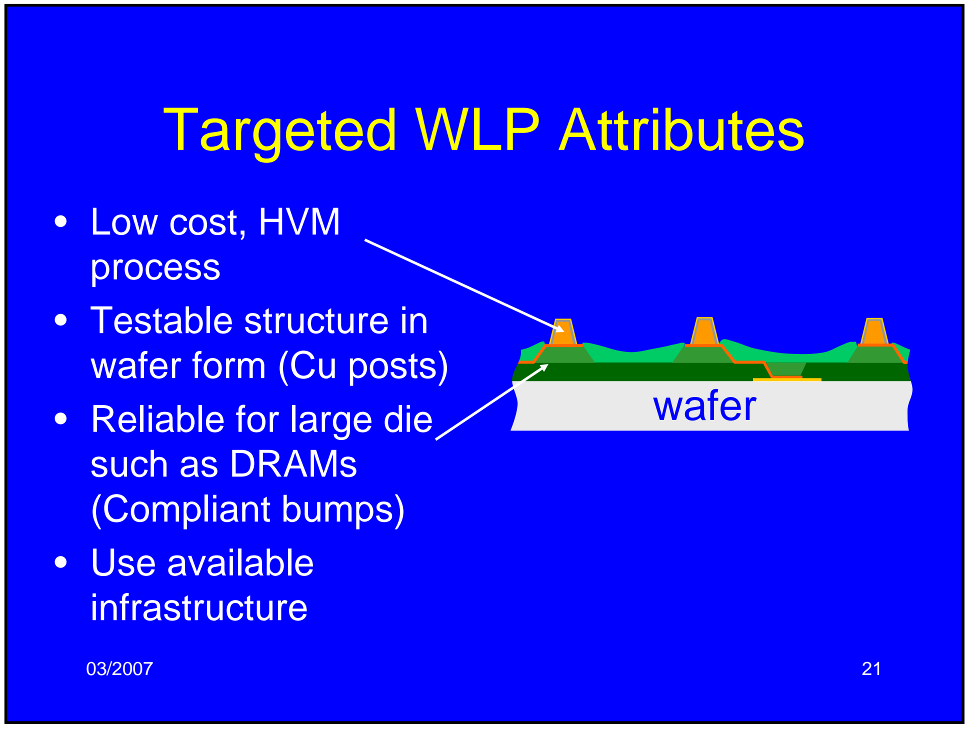
Targeted WLP Attributes
Low cost, HVM process
Testable structure in wafer form (Cu posts)
Reliable for large die such as DRAMs (Compliant bumps)
Use available infrastructure
wafer
03/2007
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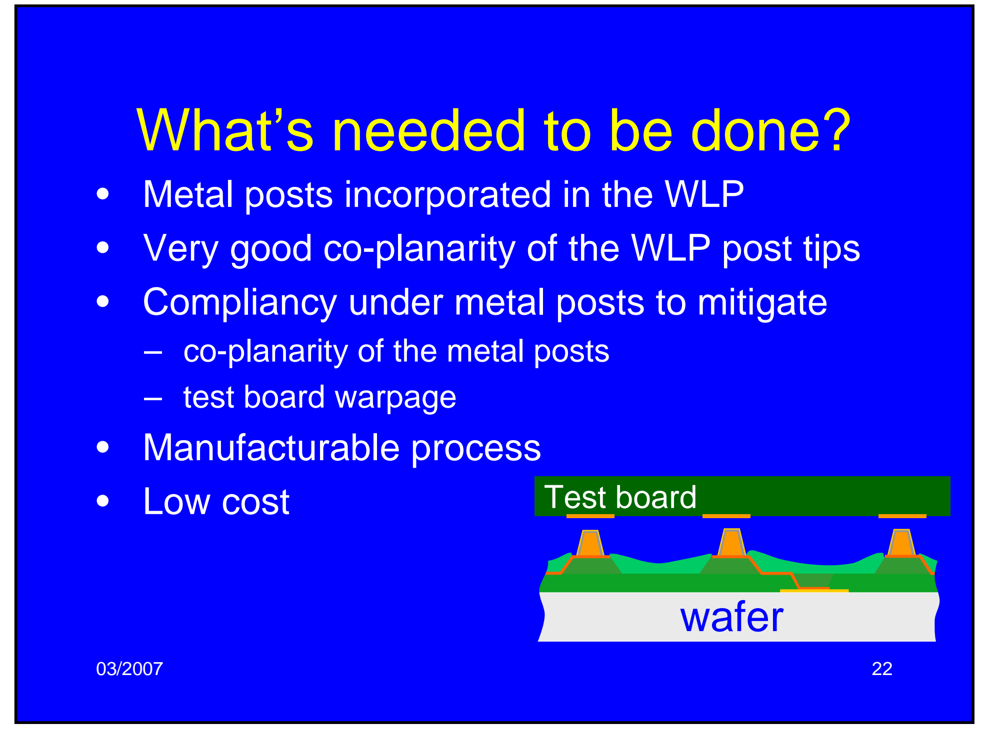
What's needed to be done?
Metal posts incorporated in the WLP
Very good co-planarity of the WLP post tips
Compliancy under metal posts to mitigate
co-planarity of the metal posts
test board warpage
Manufacturable process
Low coast
Test board
wafer
03/2007
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## Agenda

- Background
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- What needs to be done?
- **Results**
- Conclusion

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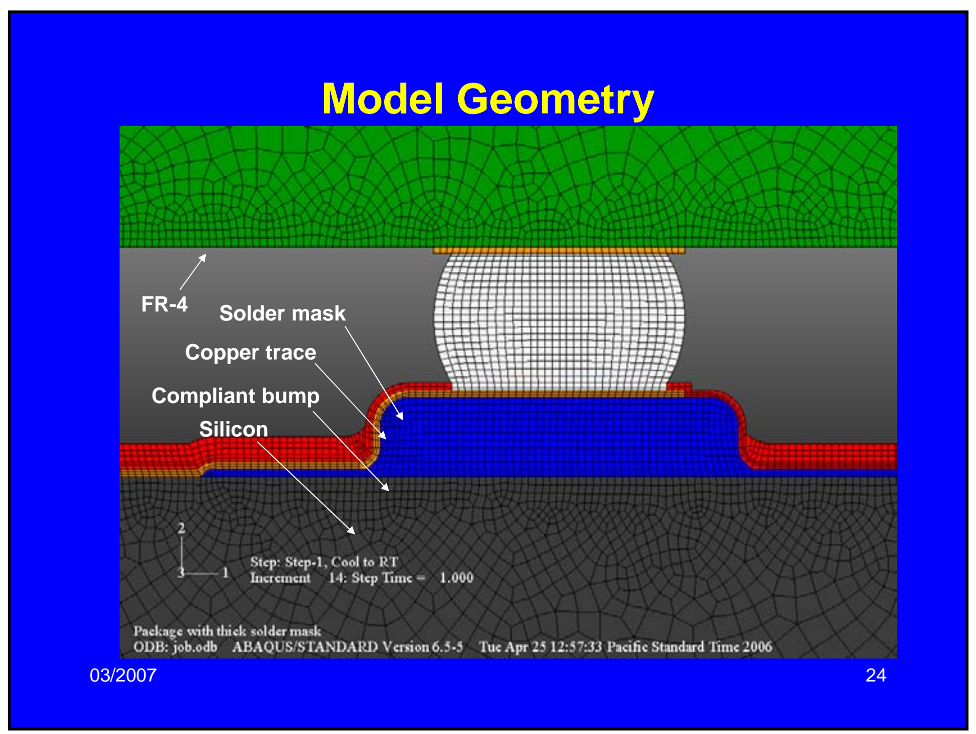
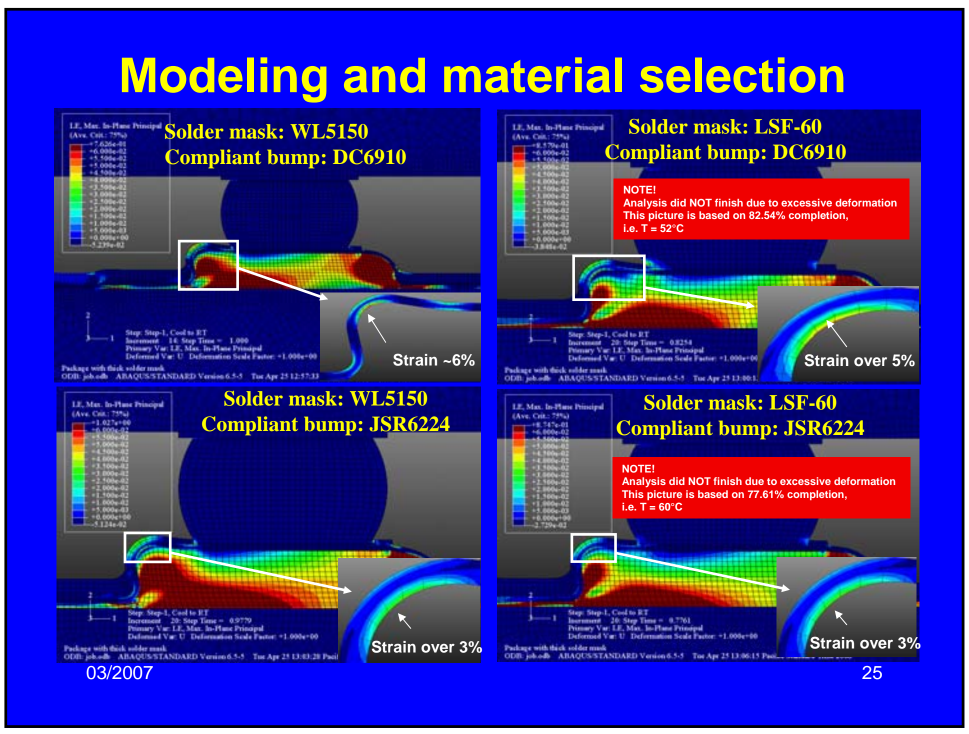
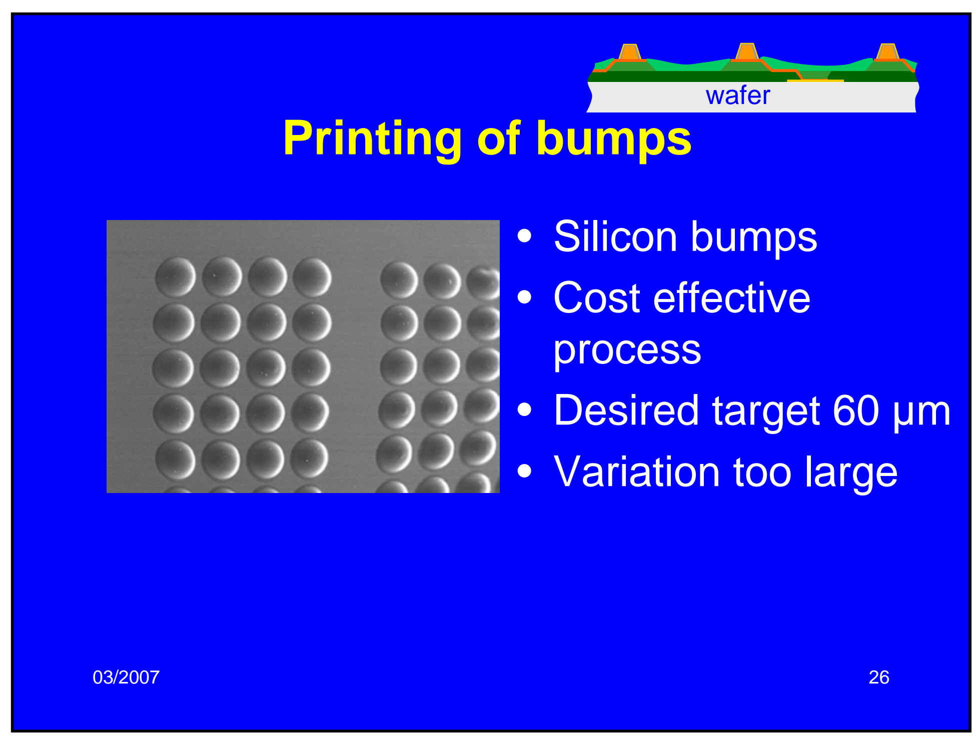



Modeling and material selection
Solder mask: WL5150
Compliant bump: DC6910
Strain ~6%
Solder mask: LSF-60
Compliant bump: DC6910
NOTE!
Analysis did NOT finish due to excessive deformation
This picture is based on 82.54% completion,
i.e. T = 52°C
Strain over 5%
Solder mask: WL5150
Compliant bump: JSR6224
Strain over 3%
Solder mask: LSF-60
Compliant bump: JSR6224
NOTE!
Analysis did NOT finish due to excessive deformation
This picture is based on 77.61% completion,
i.e. T = 60°C
Strain over 3%
03/2007
25


wafer
Printing of bumps
• Silicon bumps
• Cost effective process
• Desired target 60 µm
• Variation too large
03/2007
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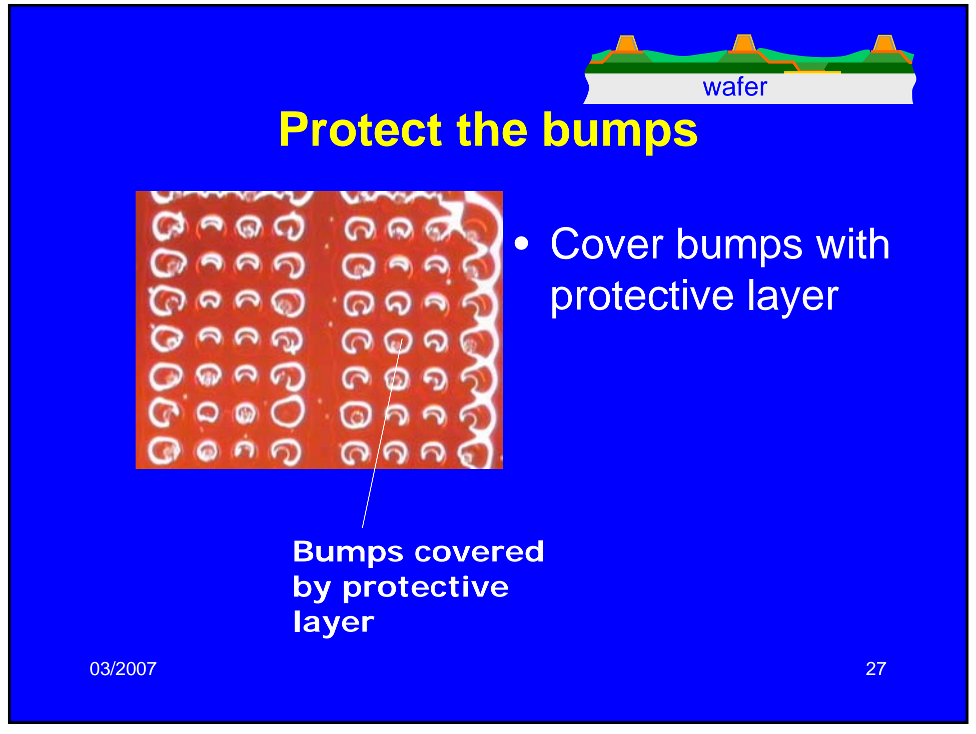
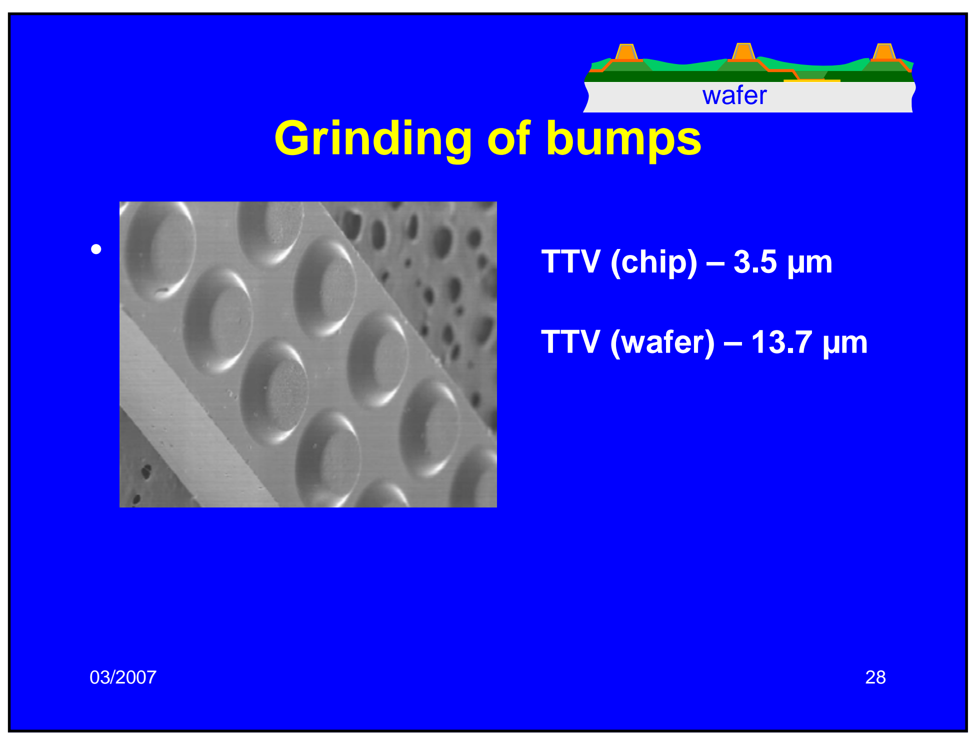

wafer
Protect the bumps
• Cover bumps with protective layer
Bumps covered by protective layer
03/2007
27


wafer
Grinding of bumps
TTV (chip) – 3.5 µm
TTV (wafer) – 13.7 µm
03/2007
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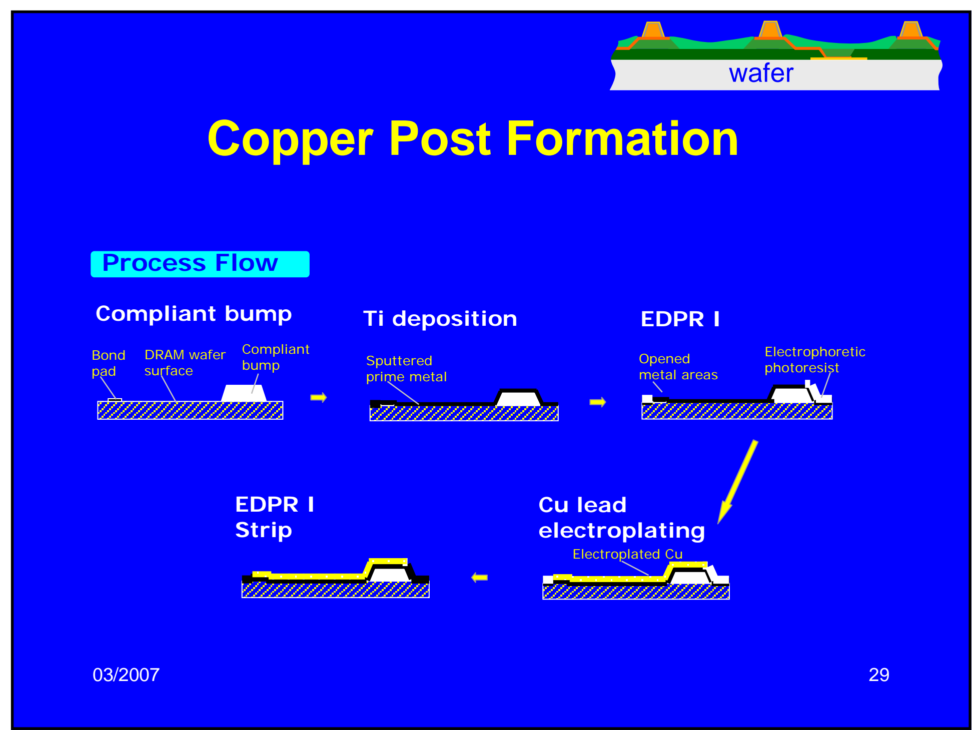
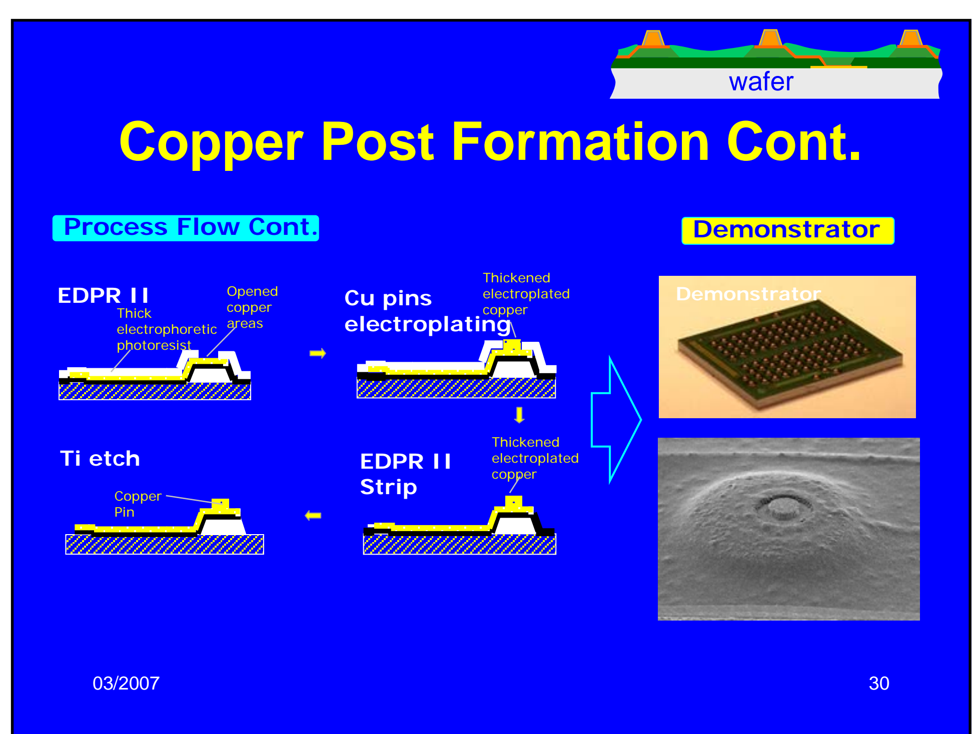


wafer
Copper Post Formation
Process Flow
Compliant bump
Bond pad
DRAM wafer surface
Compliant bump
Ti deposition
Sputtered prime metal
EDPR I
Opened metal areas
Electrophoretic photoresist
EDPR I Strip
Cu lead electroplating
Electroplated Cu
03/2007
29

wafer
Copper Post Formation Cont.
Process Flow Cont.
Demonstrator
EDPR II
Thick electrophoretic photoresist
Opened copper areas
Cu pins electroplating
Thickened electroplated copper
Demonstrator
Ti etch
Copper Pin
EDPR II Strip
Thickened electroplated copper
03/2007
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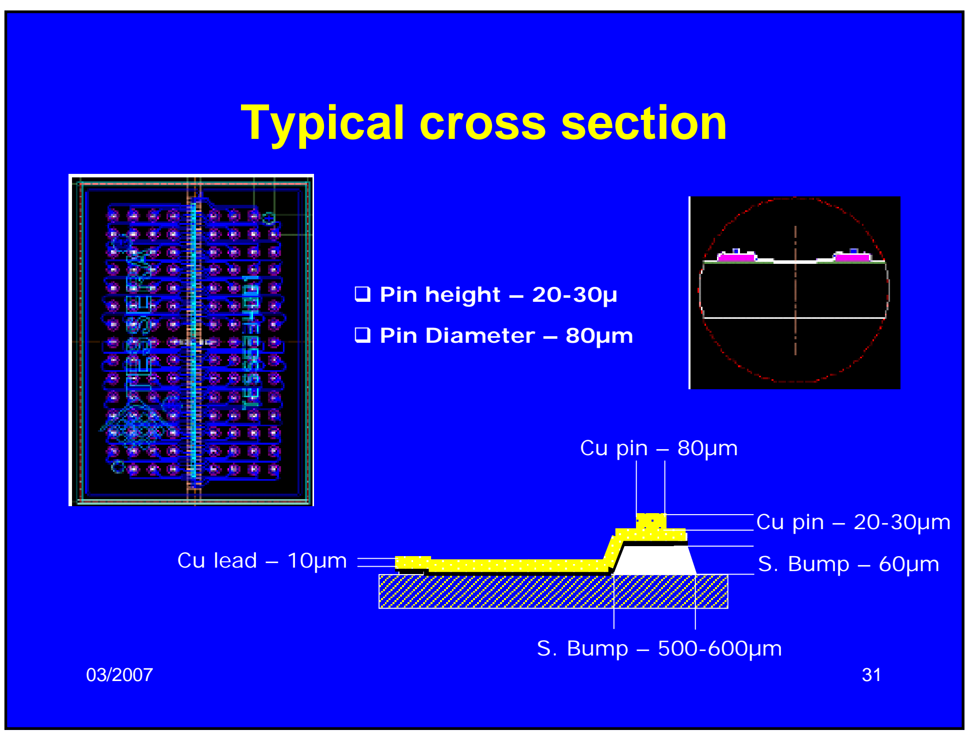
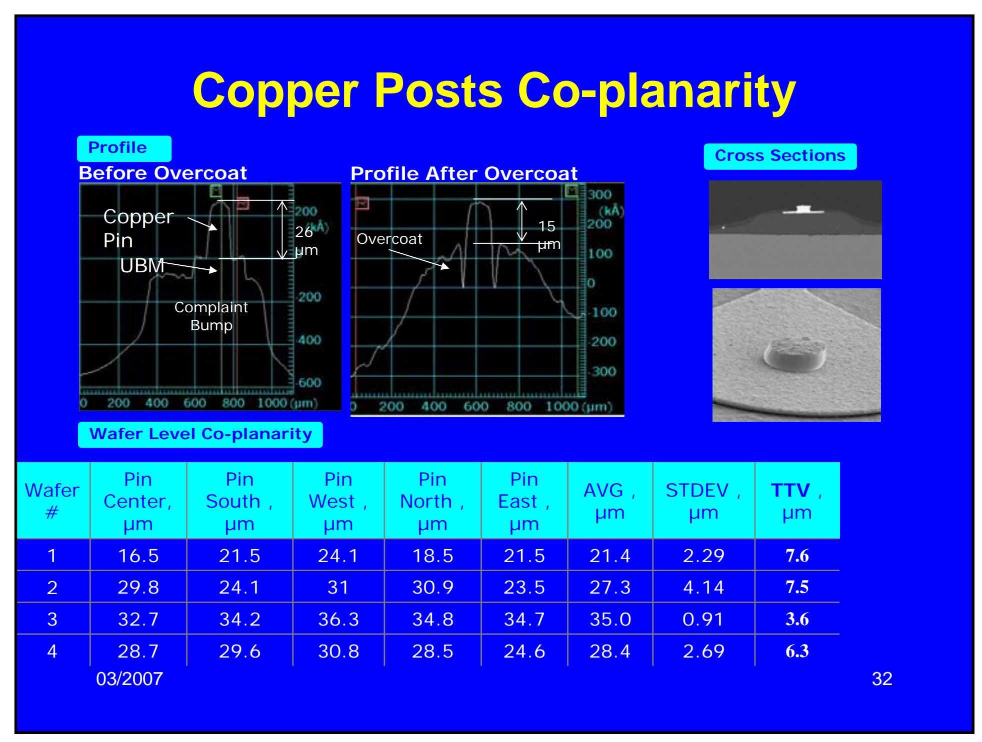
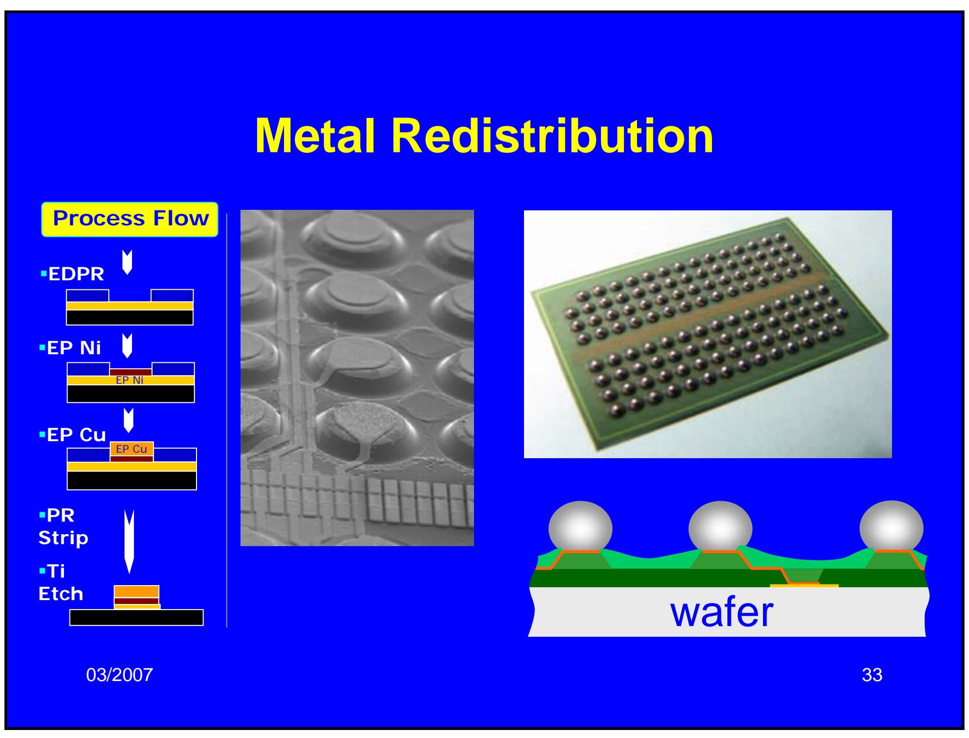



| Wafer # | Pin Center, µm | Pin South , µm | Pin West , µm | Pin North , µm | Pin East , µm | AVG , µm | STDEV , µm | TTV , µm |
|---|---|---|---|---|---|---|---|---|
| 1 | 16.5 | 21.5 | 24.1 | 18.5 | 21.5 | 21.4 | 2.29 | 7.6 |
| 2 | 29.8 | 24.1 | 31 | 30.9 | 23.5 | 27.3 | 4.14 | 7.5 |
| 3 | 32.7 | 34.2 | 36.3 | 34.8 | 34.7 | 35.0 | 0.91 | 3.6 |
| 4 | 28.7 | 29.6 | 30.8 | 28.5 | 24.6 | 28.4 | 2.69 | 6.3 |


Metal Redistribution
Process Flow
▪EDPR
▪EP Ni
EP Ni
▪EP Cu
EP Cu
▪PR
Strip
▪Ti
Etch
wafer
03/2007
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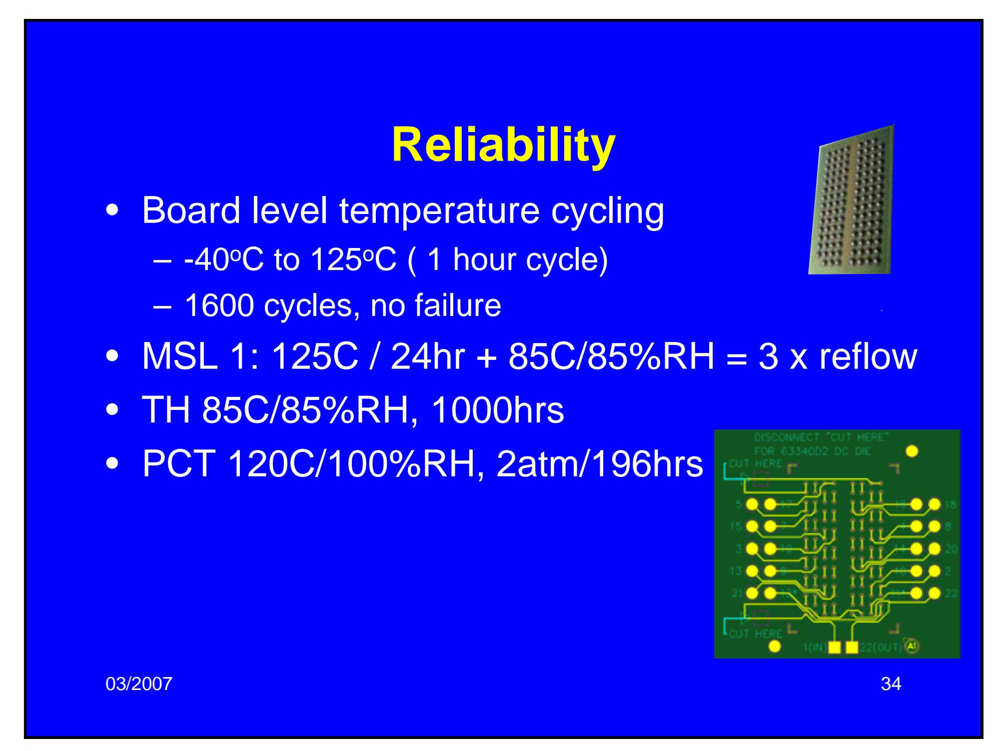
Reliability
• Board level temperature cycling
– -40oC to 125oC ( 1 hour cycle)
– 1600 cycles, no failure
• MSL 1: 125C / 24hr + 85C/85%RH = 3 x reflow
• TH 85C/85%RH, 1000hrs
• PCT 120C/100%RH, 2atm/196hrs
03/2007
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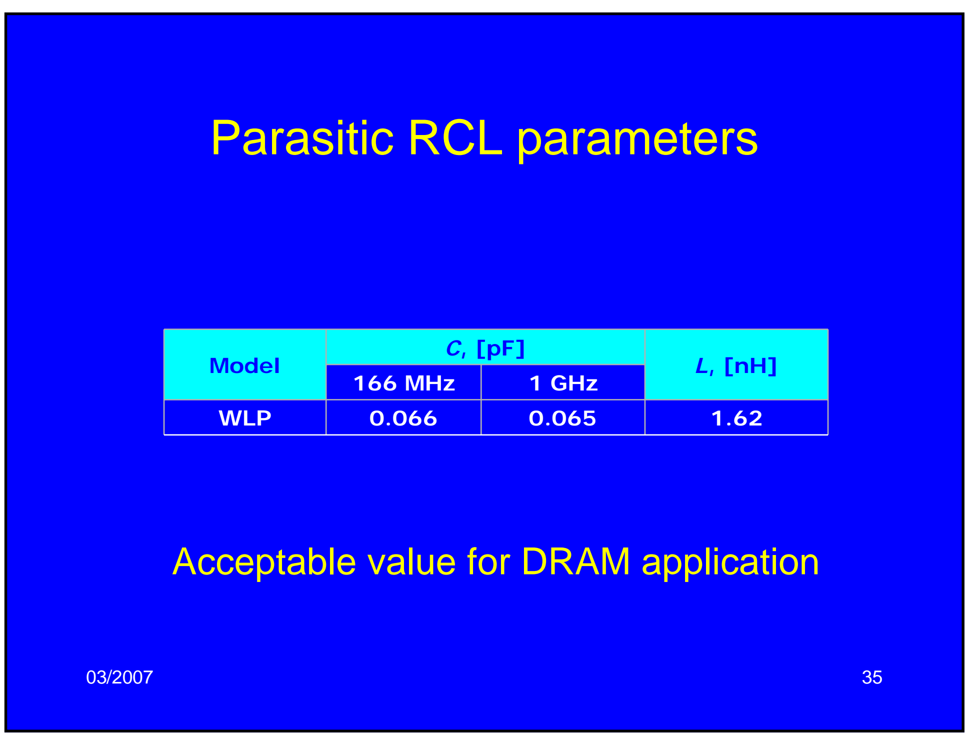
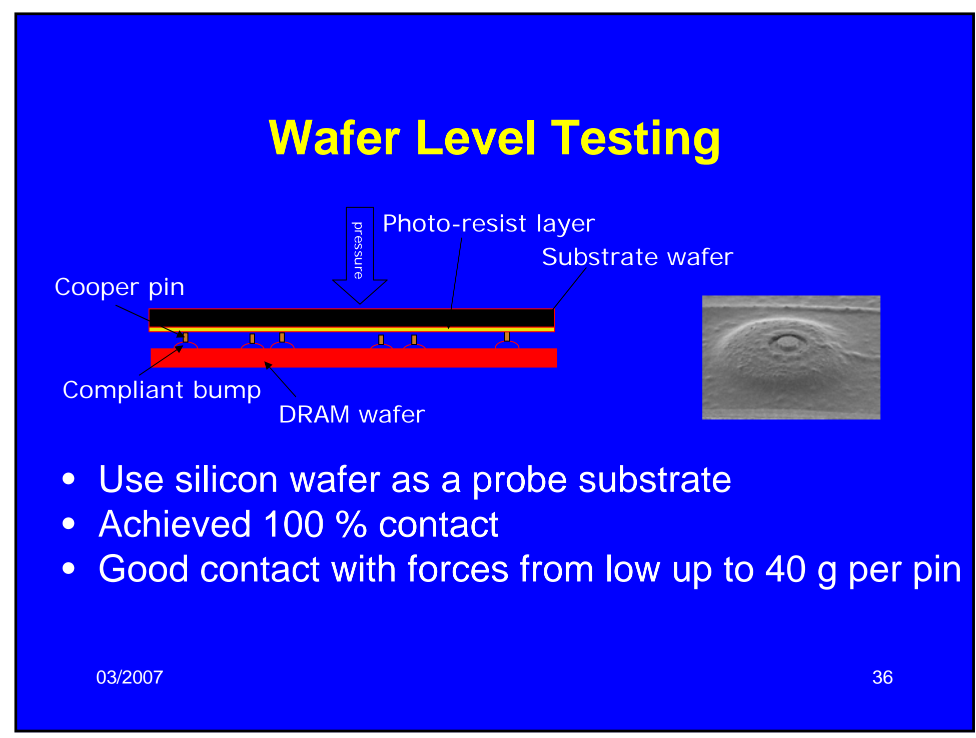

Parasitic RCL parameters
Model
C, [pF]
166 MHz
1 GHz
L, [nH]
WLP
0.066
0.065
1.62
Acceptable value for DRAM application
03/2007
35


Wafer Level Testing
pressure
Photo-resist layer
Substrate wafer
Cooper pin
Compliant bump
DRAM wafer
• Use silicon wafer as a probe substrate
• Achieved 100 % contact
• Good contact with forces from low up to 40 g per pin
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## Agenda

- Background
- Wafer Level Packaging and why?
- What needs to be done?
- Results
- **Conclusion**

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## Summary

- Demonstrated a complaint wafer level packaging (WLP) for large die
- Demonstrated a WLP structure testable without socket interposer
- Demonstrated a reliable WLP structure mounted on board
- Stay tuned for more data to come

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THANK YOU
03/2007
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# A New Probe Card Approach for Wafer Level Chip Scale Package Testing

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Norman J. Armendariz, PhD

## AGENDA

- The Need
- WSP-Wafer Scale Packages
- WSP- Manufacturing Test Flow
- Current WSP Probe Card Technologies
- New WSP- Probe Card Concept
- Challenges
- WSP Comparative Summary
- Discussion

03/2007 Wafer Level Probing of WLCSP 2

## THE NEED

TI has been testing packages at final test after singulation for some time. However, the increasing use of WLCSP- wafer level chip scale package formats require cost-effective RF testing at the wafer-level or before singulation to further reduce test costs and be globally competitive.

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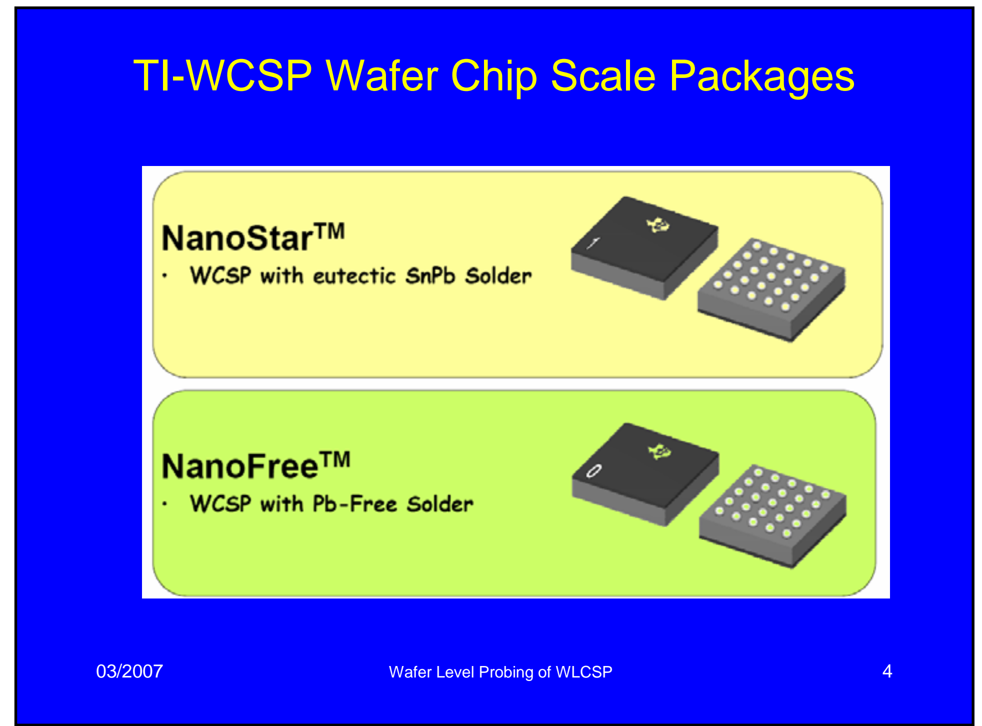
## TI-WCSP Wafer Chip Scale Packages

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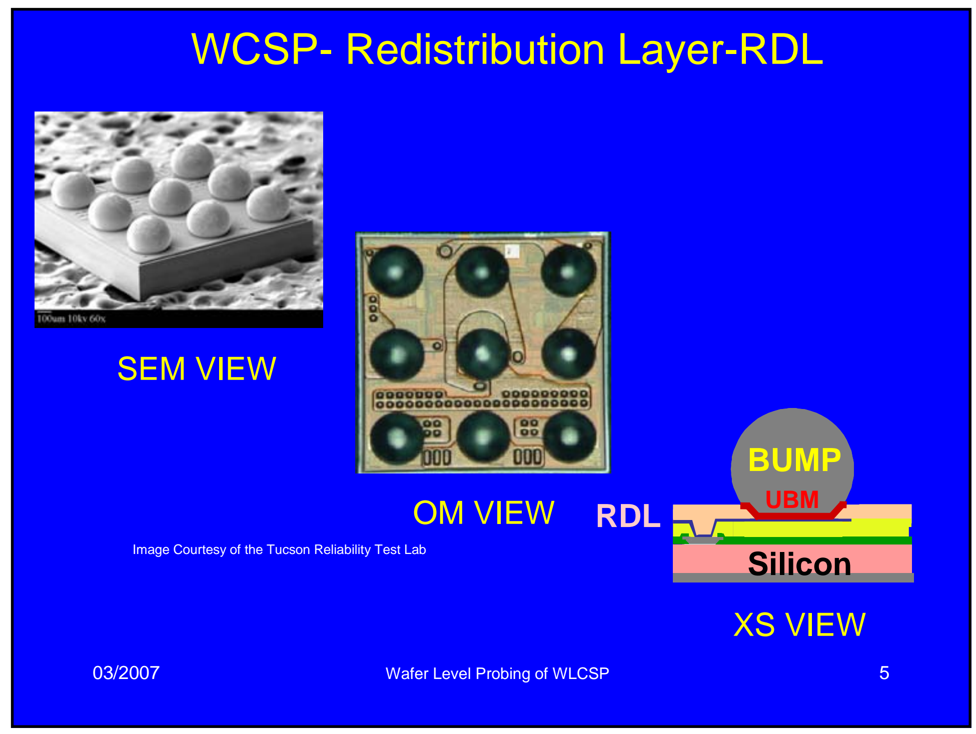
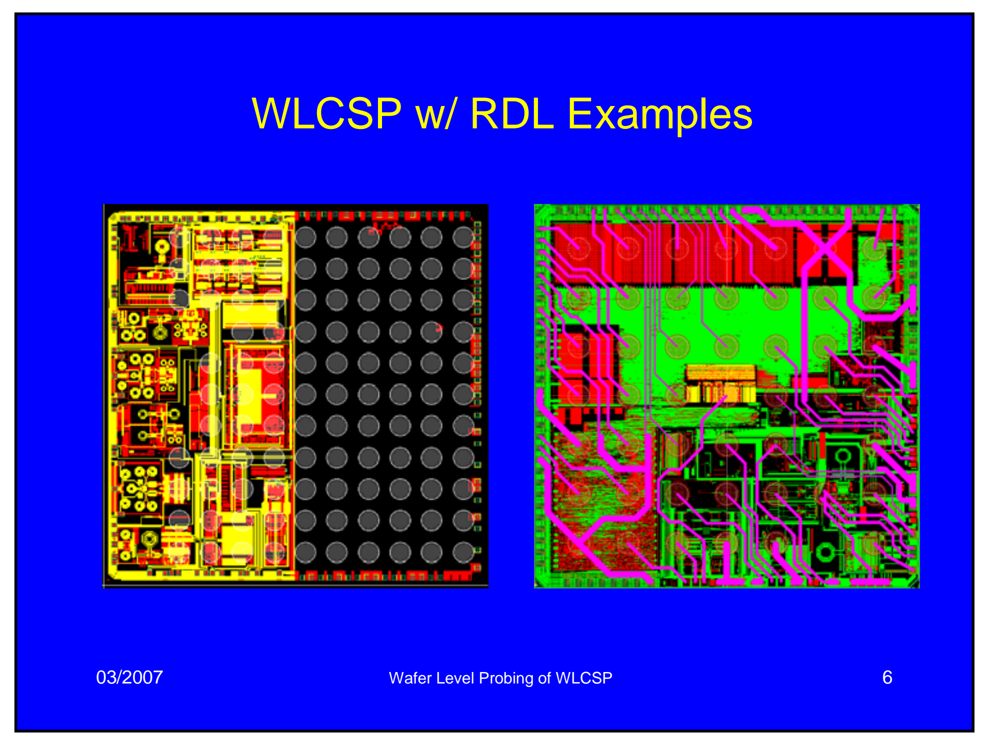

WCSP- Redistribution Layer-RDL
SEM VIEW
OM VIEW
BUMP
UBM
RDL
Silicon
XS VIEW
Image Courtesy of the Tucson Reliability Test Lab
03/2007
Wafer Level Probing of WLCSP
5


WLCSP w/ RDL Examples
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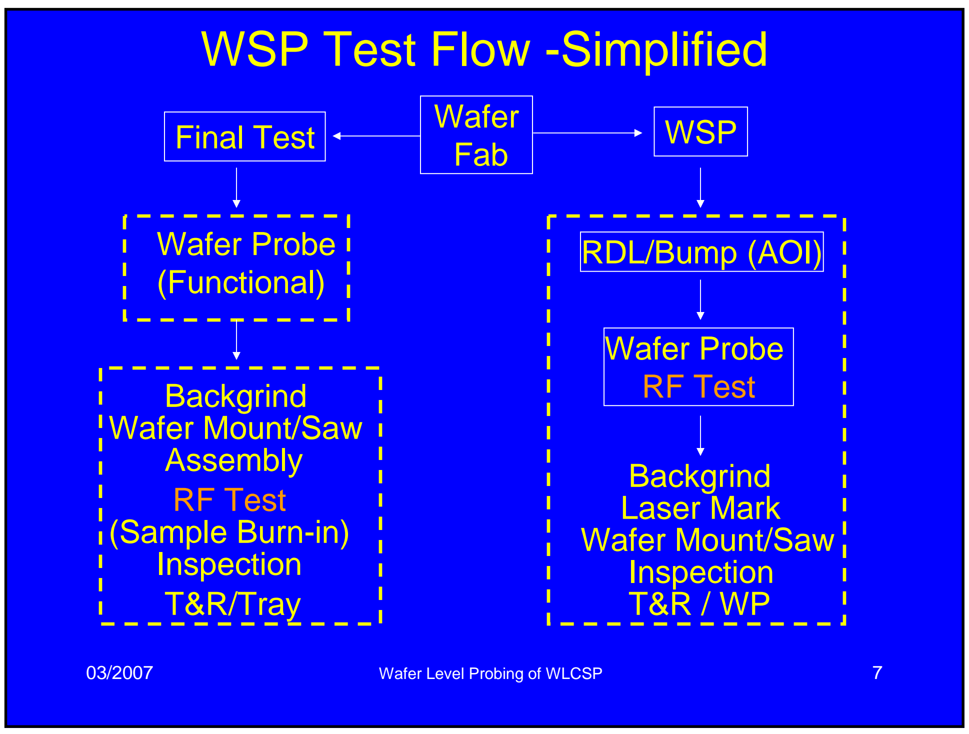
Wafer Level Probing of WLCSP
6




## Current Wafer Level Probe Card Technologies

- Cantilever- (Needle Probes)
- Vertical- (Buckling Beam)
- Membrane (Beam Probes) RF

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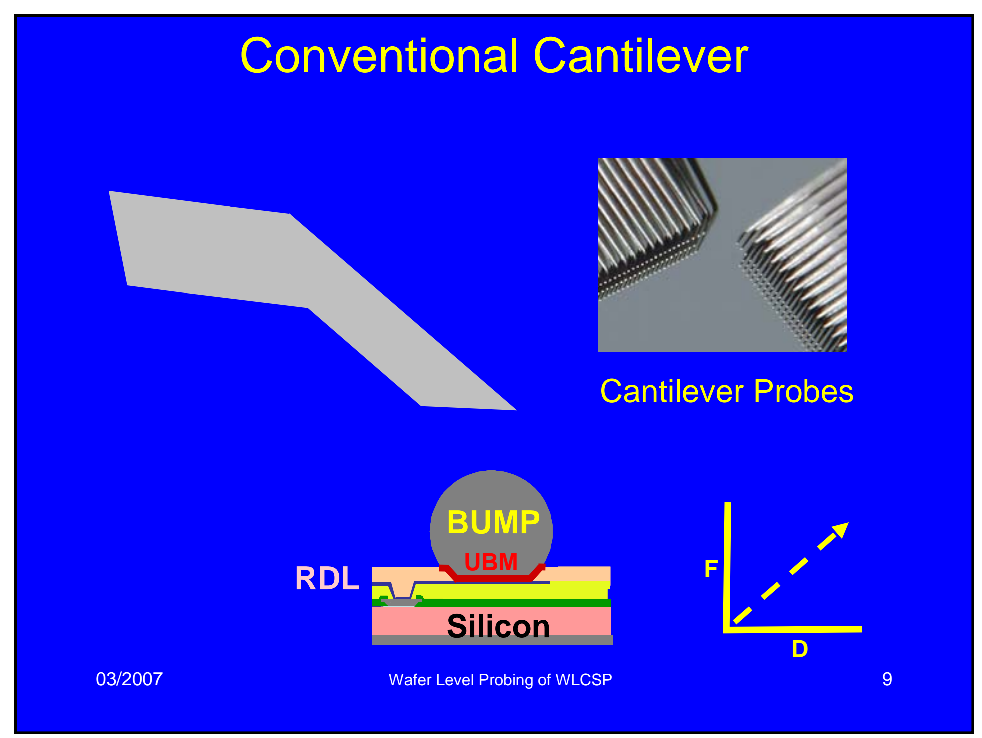
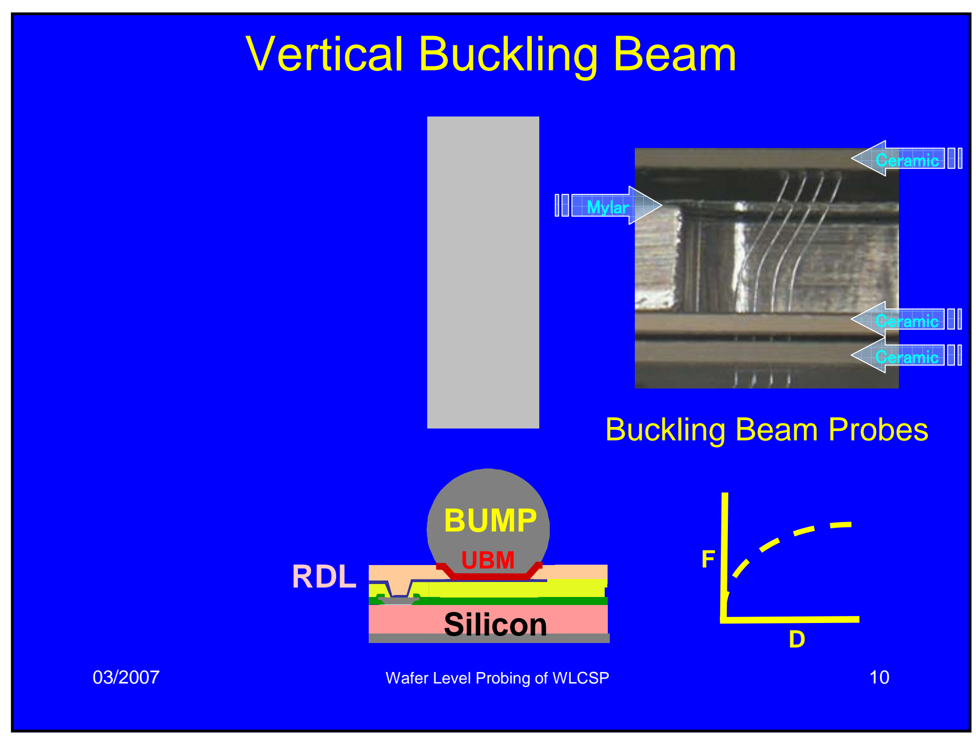
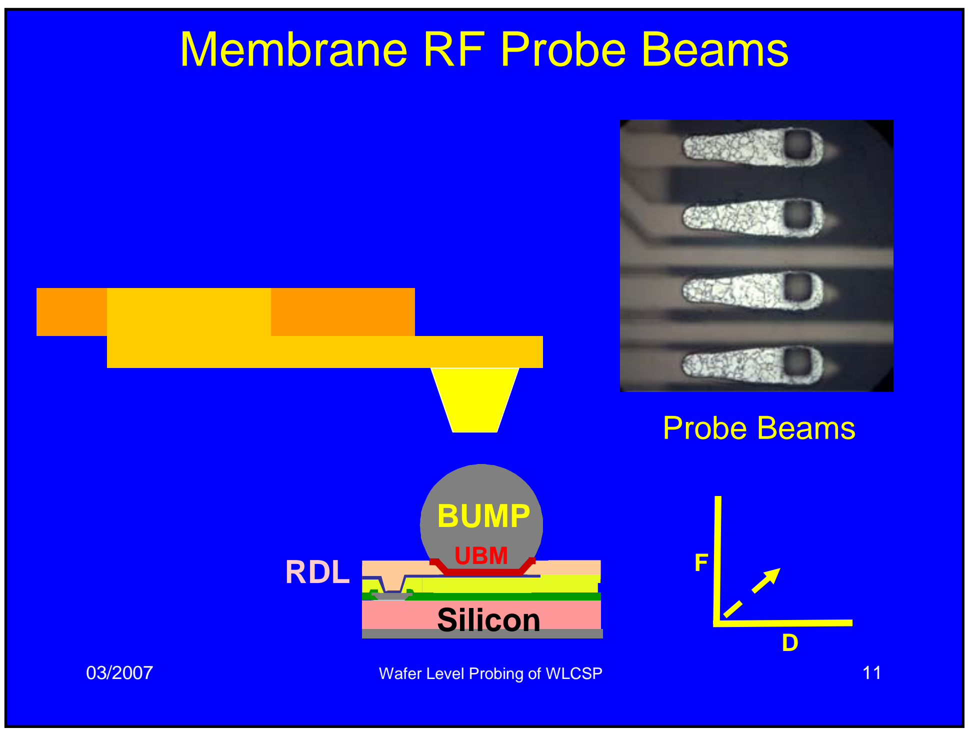

Conventional Cantilever
Cantilever Probes
BUMP
UBM
RDL
Silicon
F
D
03/2007
Wafer Level Probing of WLCSP
9


Vertical Buckling Beam
Mylar
Ceramic
Ceramic
Ceramic
Buckling Beam Probes
BUMP
UBM
RDL
Silicon
F
D
03/2007
Wafer Level Probing of WLCSP
10




## Current WSP Probe Card Status

Both cantilever and VPC probe cards exhibited limited electrical properties as well as other physical & operational limitations.

Membrane probe cards have been employed for those applications that need controlled impedance for RF (radio frequency) testing, but at some cost and also with similar physical and operational limitations.

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## Thus, WSP Probe Card Concept

**Convert or modify FT-final test boards, which already use similar sockets and RF pogo pins into a wafer level probe card for WLCSP- wafer level chip scale packages requiring RF testing and avoid an expensive probe card to skip the RF FT step!!!.**

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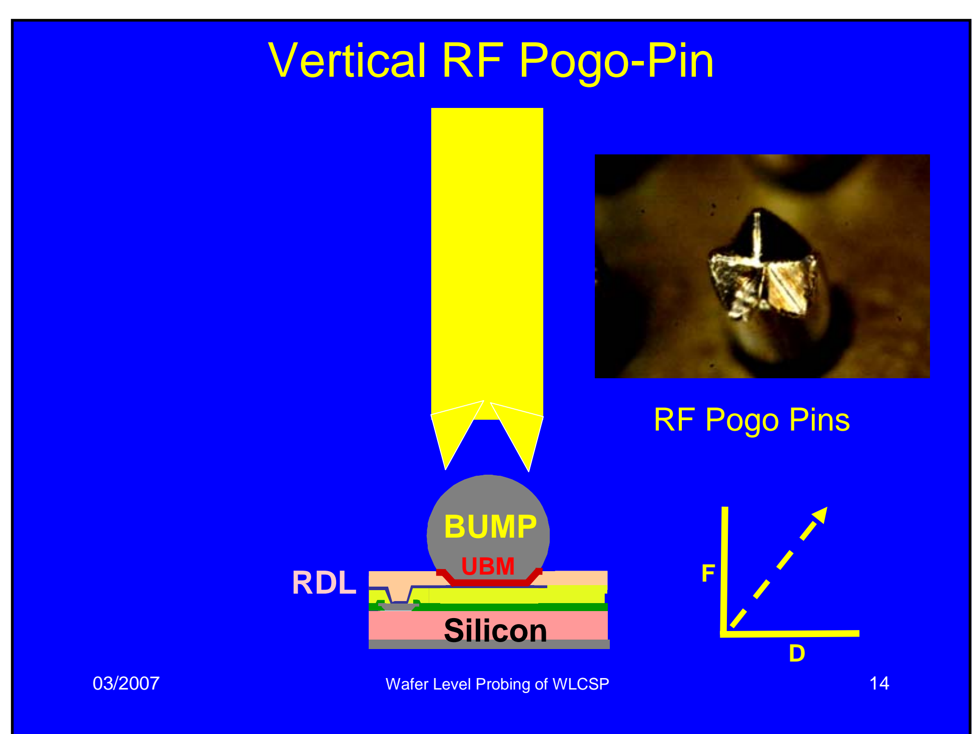

## WSP Probe Card Integration Challenges

**Initial probe cards were found to have a number of design / fabrication violations which made it difficult to mechanically and/or operational integrate for wafer-level testing on TI probers and test floors. Major issues :**

- **Socket/ Pogo-Pin Design**
- **Prober/tester Interface**
- **Alignment Algorithm**
- **Cleaning**

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## WSP Probe Card Design/ Fabrication

**Wafer Side (L) and insulator (R) overlaid as a template showing the exposed areas that are allowed between probe card and probe card support plate (PCSP). A number of components or protruding features were found in "blue" areas or "keep-out" areas (R).**

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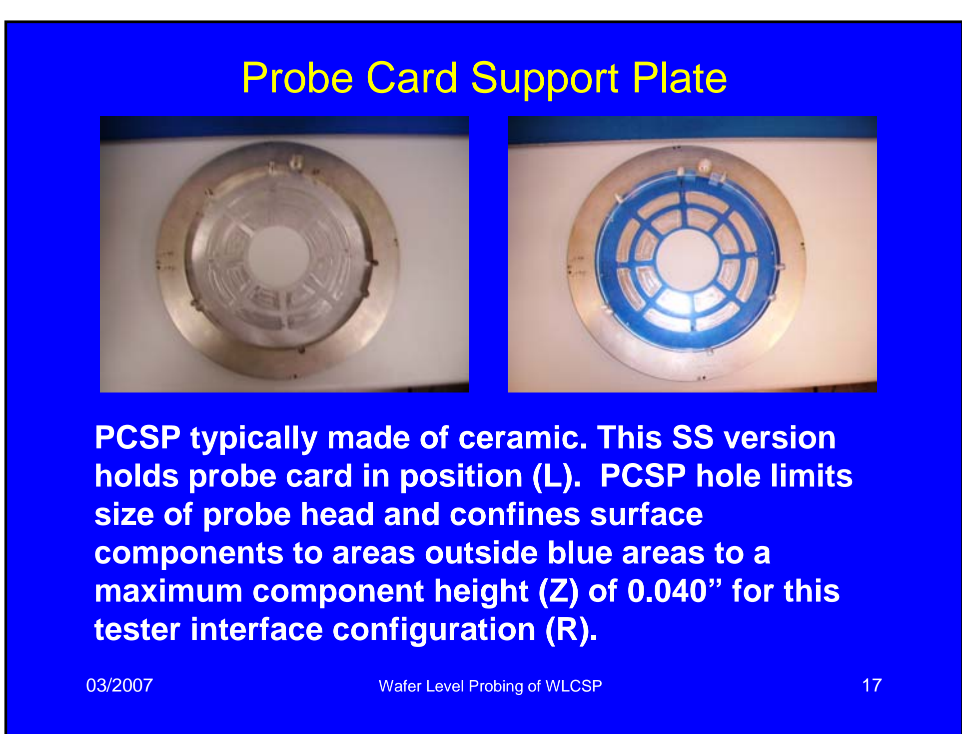
Probe Card Support Plate
PCSP typically made of ceramic. This SS version holds probe card in position (L). PCSP hole limits size of probe head and confines surface components to areas outside blue areas to a maximum component height (Z) of 0.040” for this tester interface configuration (R).
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Wafer Level Probing of WLCSP
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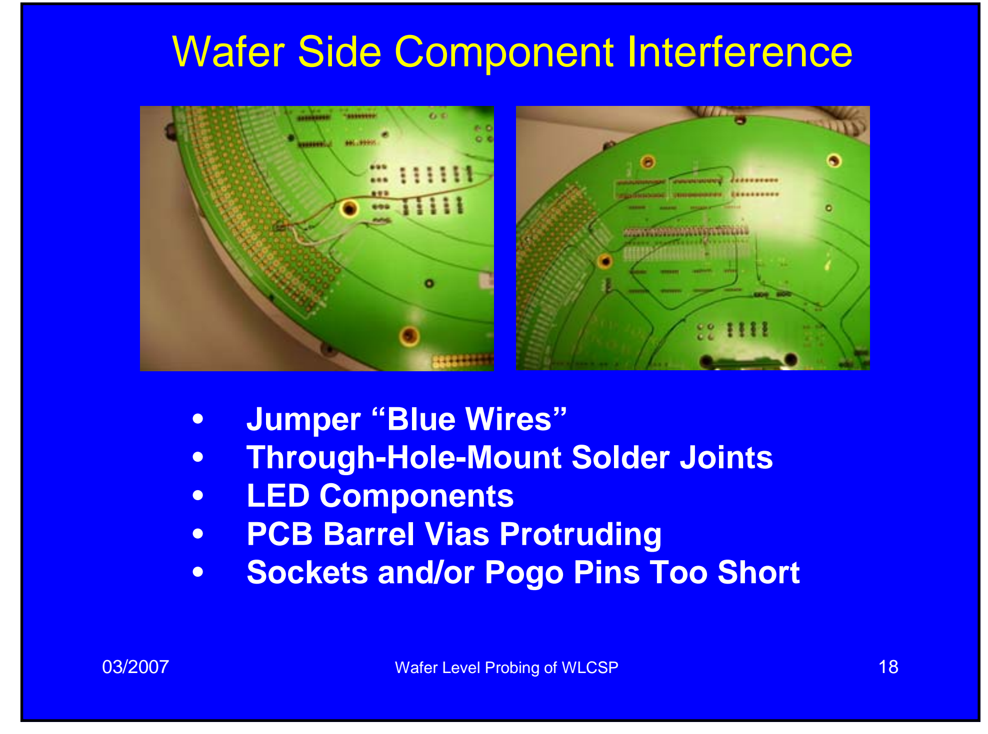
Wafer Side Component Interference
Jumper “Blue Wires”
Through-Hole-Mount Solder Joints
LED Components
PCB Barrel Vias Protruding
Sockets and/or Pogo Pins Too Short
03/2007
Wafer Level Probing of WLCSP
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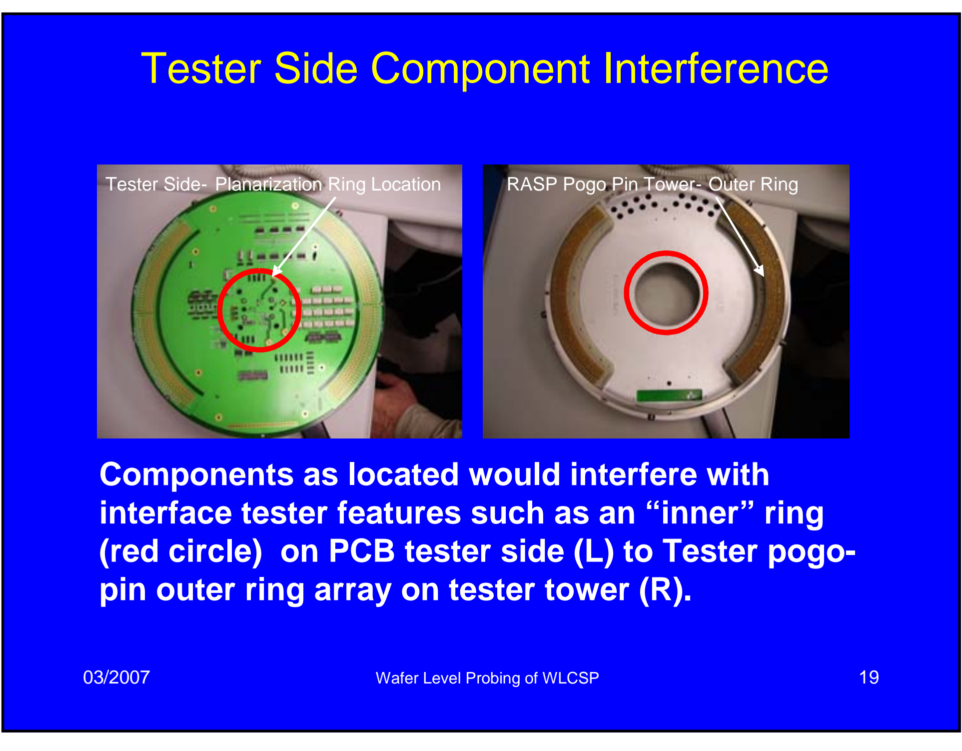
Tester Side Component Interference
Tester Side- Planarization Ring Location
RASP Pogo Pin Tower- Outer Ring
Components as located would interfere with interface tester features such as an "inner" ring (red circle) on PCB tester side (L) to Tester pogo-pin outer ring array on tester tower (R).
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Wafer Level Probing of WLCSP
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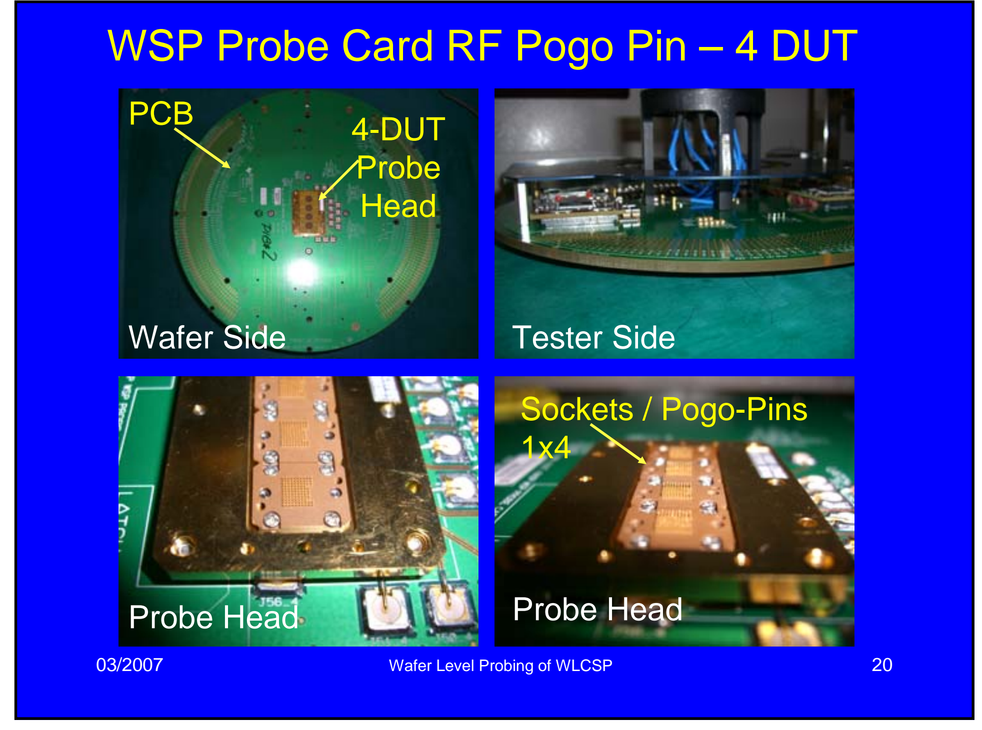
WSP Probe Card RF Pogo Pin – 4 DUT
PCB
4-DUT
Probe
Head
Wafer Side
Tester Side
Sockets / Pogo-Pins
1x4
Probe Head
Probe Head
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Wafer Level Probing of WLCSP
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## WSP PROBE CARD SUMMARY

| Technology | PROs | CONs |
|---|---|---|
| **Cantilever Needles** | Low price<br>Short Lead-time for New Designs.<br>Repairable Contacts<br>Many Qualified Suppliers | Electrically Limited<br>Periphery limited<br>F / D Linear<br>Bump-Top Damage/ Reflow |
| **VPC Buckling Wires** | Multi-site 4-16x<br>F / D Profile<br>Hi-Temp Stability<br>Many Qualified Suppliers | Electrically Limited<br>Initial Price and Lead Time<br>Bump-Top Damage/ Reflow<br>Probe binding |
| **Membrane Probe Beams** | Electrical Properties<br>Small scrub marks<br>Alignment | Production Reliability<br>Initial Price & Lead Time<br>Die Size/ Routing Limits<br>Few Qualified Suppliers |
| **WSP Pogo-Pins** | Electrical Properties<br>Low Price<br>Small Marks on Sides of Bump<br>Multi-site x4-x16 | Current Pitch Limited to 300 um<br>Lead-Time<br>Supplier base<br>Linear F / D |

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## WSP Probe Card Future Work

- Optimize Prober to Wafer Chuck Settings
  - •Auto Vertical Chuck Adjustment
  - •Alignment Method/Algorithm
- Optimize Cleaning Settings
  - •Cleaning Material/ Tip Design
  - •Particle Size
- Minimize Probe Card Deflection
  - •Tester PCSP Design
  - •Mechanical Stiffeners
- Define Probe Card Design and User Specifications
  - • Multi-Site x8 to x16
  - • Inspection

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## DISCUSSION

03/2007 Wafer Level Probing of WLCSP 24

## Acknowledgements

- Doyce Ramey
- Kelly Daughtry
- Byron Gibbs
- Dave Reed

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# PoP Rocks

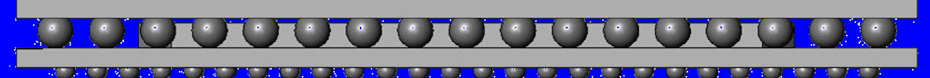
## Approaches to Socketing Package-on-Package Devices

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Jon Diller, Kiley Beard, Jamie Andes
Interconnect Devices, Inc.

## Device Description

- Logic + Memory
- Typically BGA-on-BGA
- Enables greater density & SIP solutions



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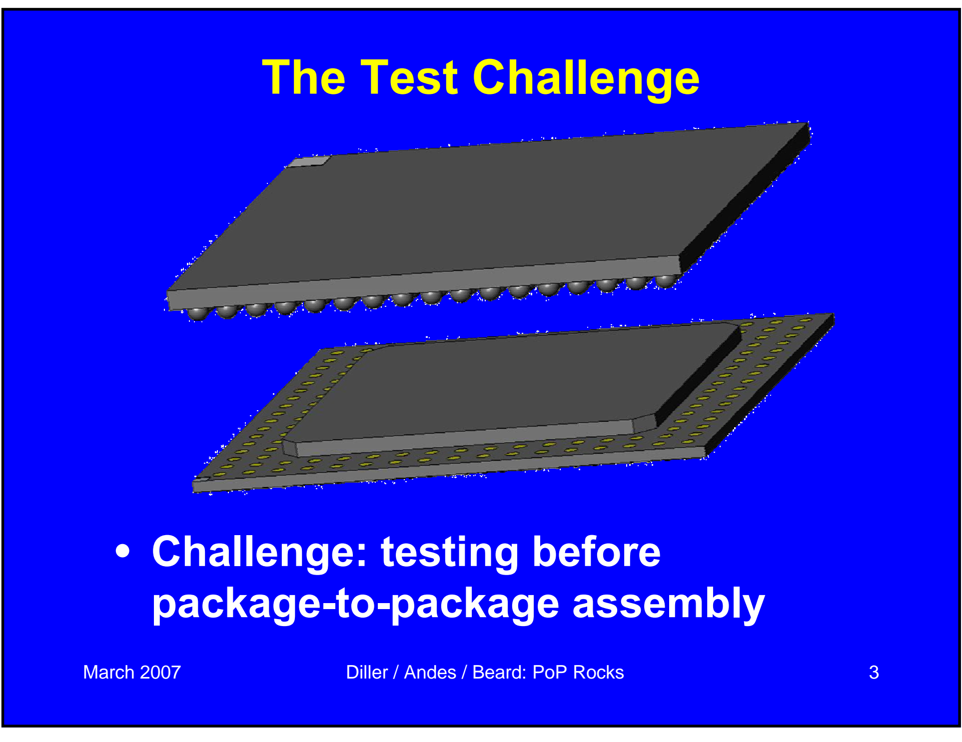


## The Ante

- If only tested after assembly, dollars lost on the parent (processor)
- Parent cannot be tested without memory function
- Test of unassembled devices requires contact to memory side – on the top!

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## Platform Considerations

- Top-side contact integrated with handler chuck
- Must be completely free-floating
- Must mate / de-mate per cycle
- Cycle life should be ≥ socket contacts
- Should be noiseless to memory test standards

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## The Basis: Load Board Design

- Normal array of DUT pads
- Extra array of interface pads

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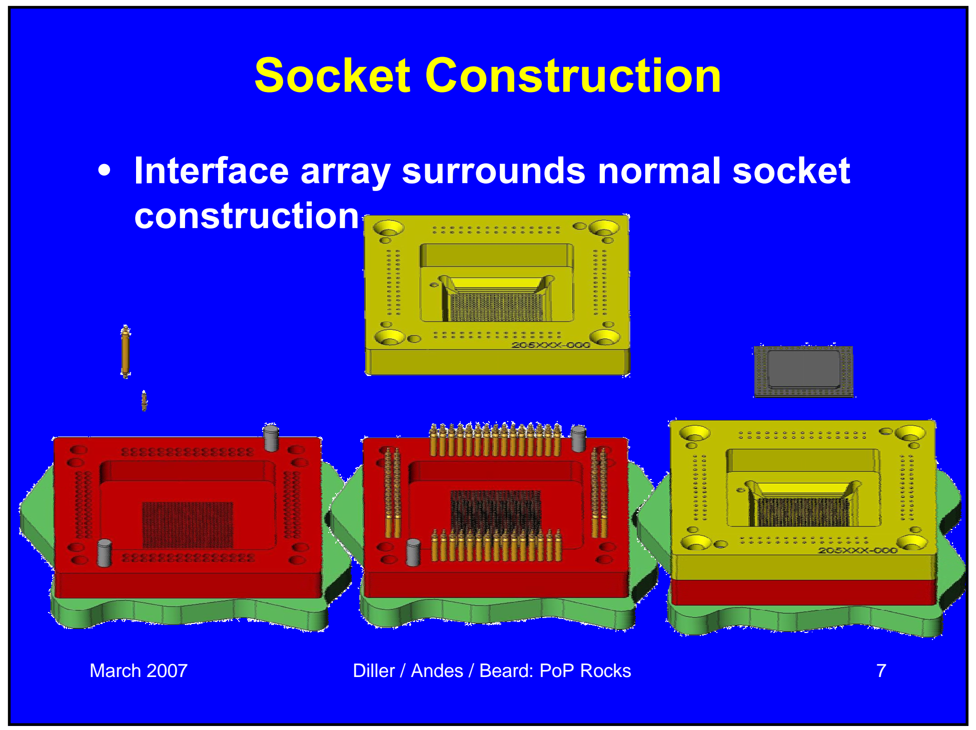
Socket Construction
• Interface array surrounds normal socket construction
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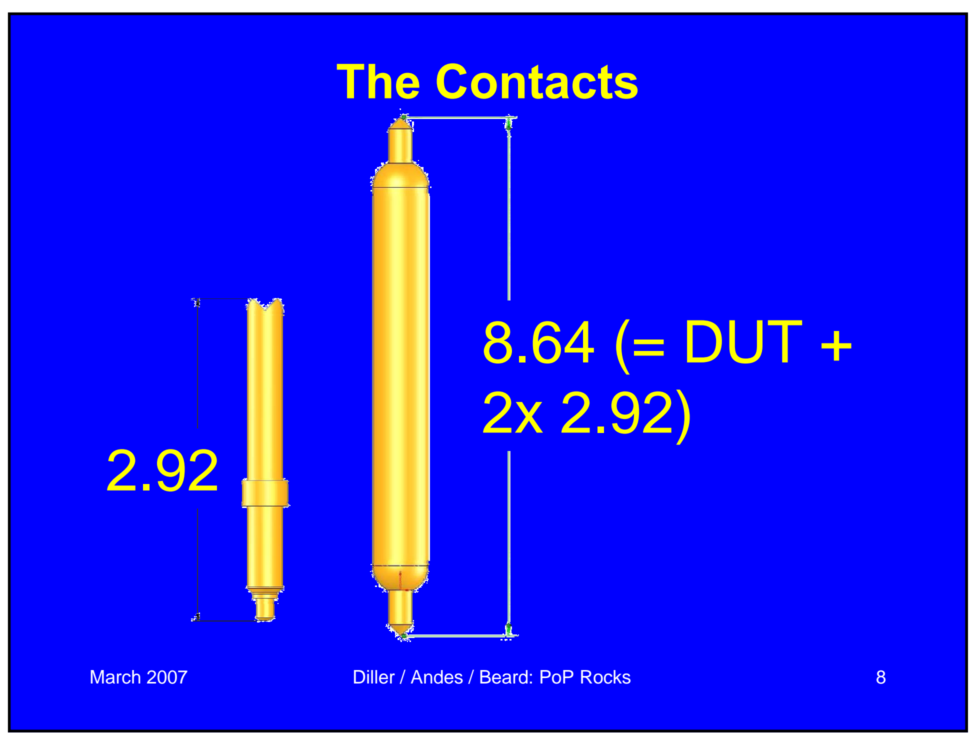
The Contacts
2.92
8.64 (= DUT + 2x 2.92)
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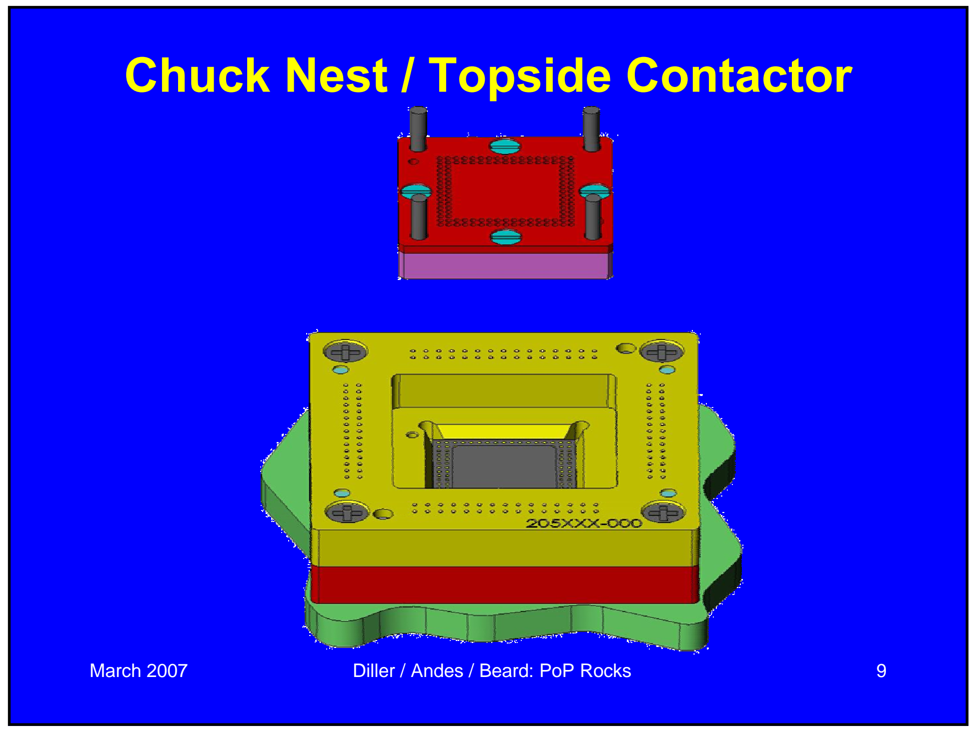
Chuck Nest / Topside Contactor
205XXX-000
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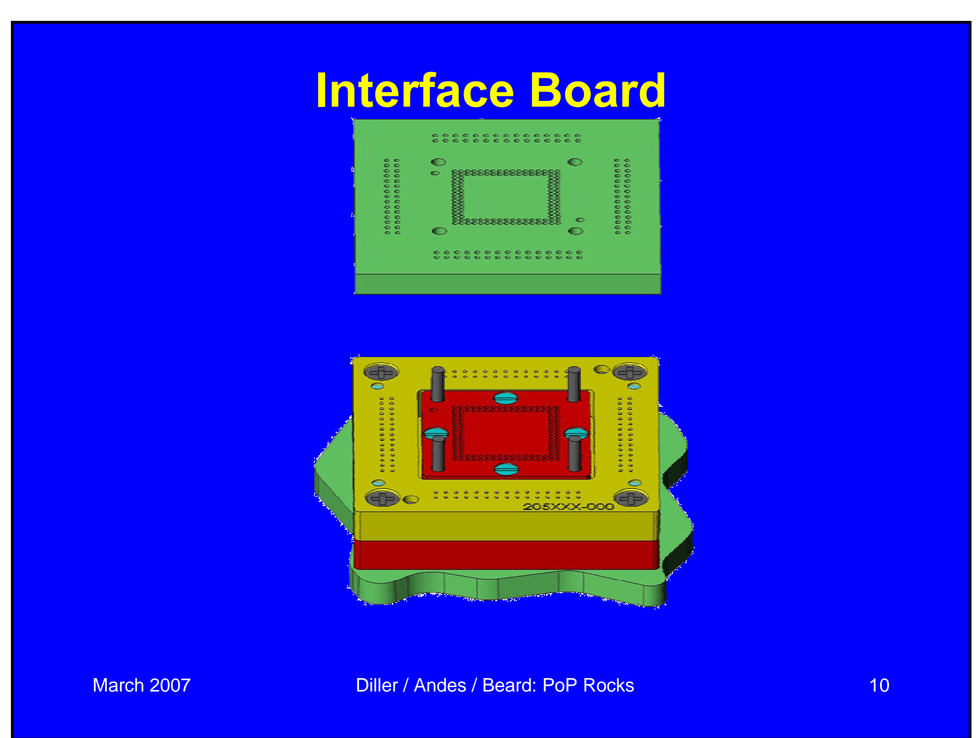
Interface Board
205XXX-000
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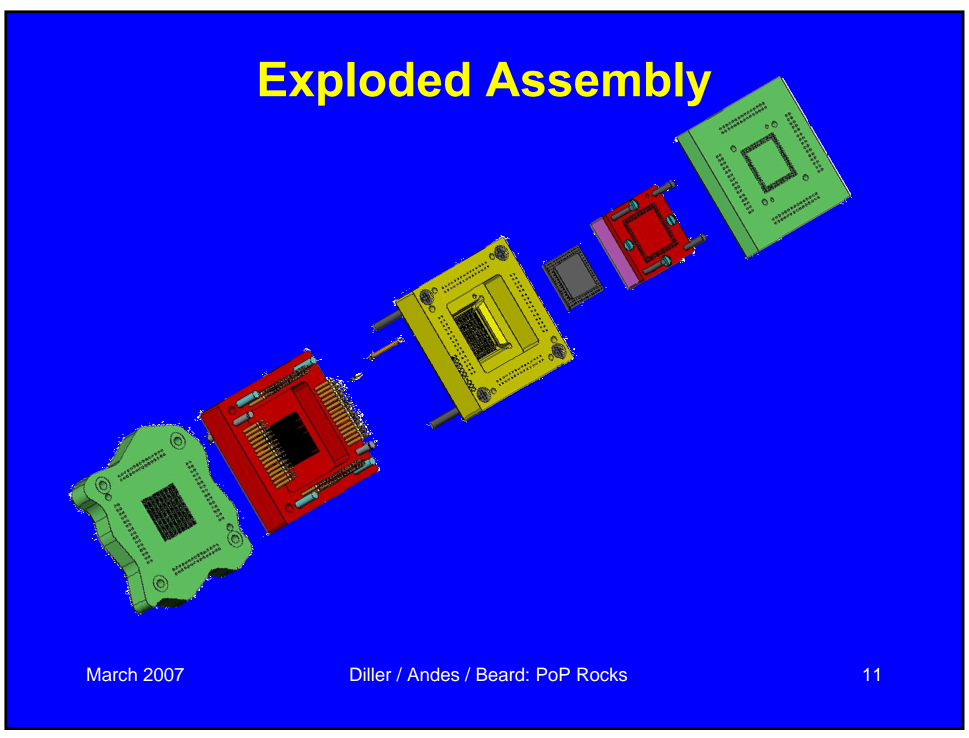
Exploded Assembly
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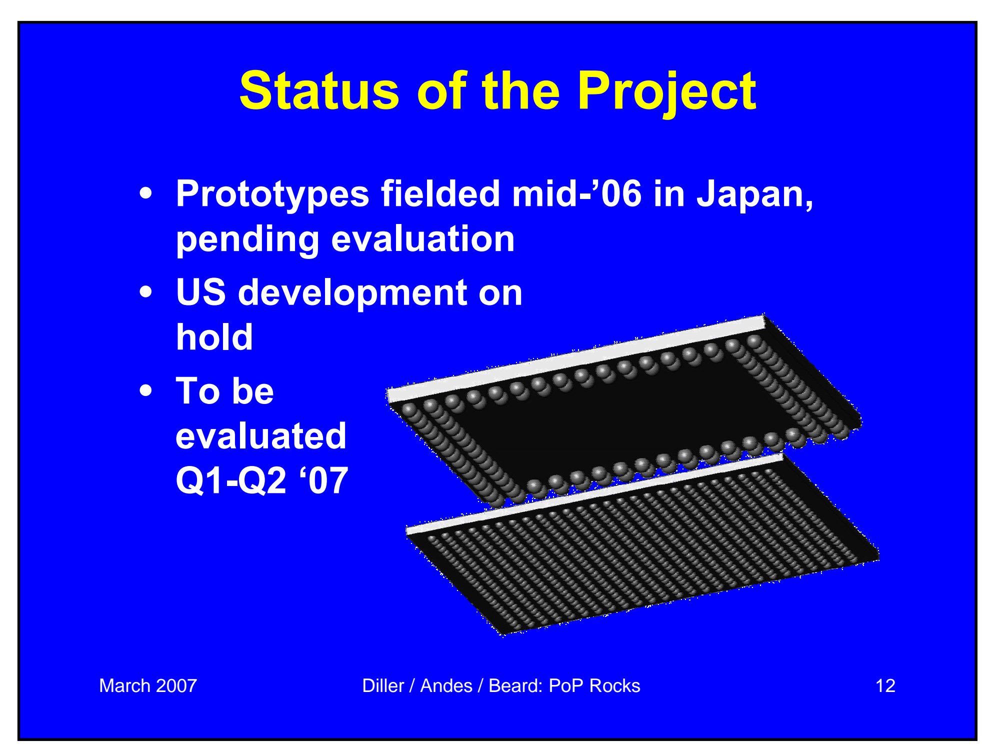
Status of the Project
• Prototypes fielded mid-'06 in Japan, pending evaluation
• US development on hold
• To be evaluated Q1-Q2 '07
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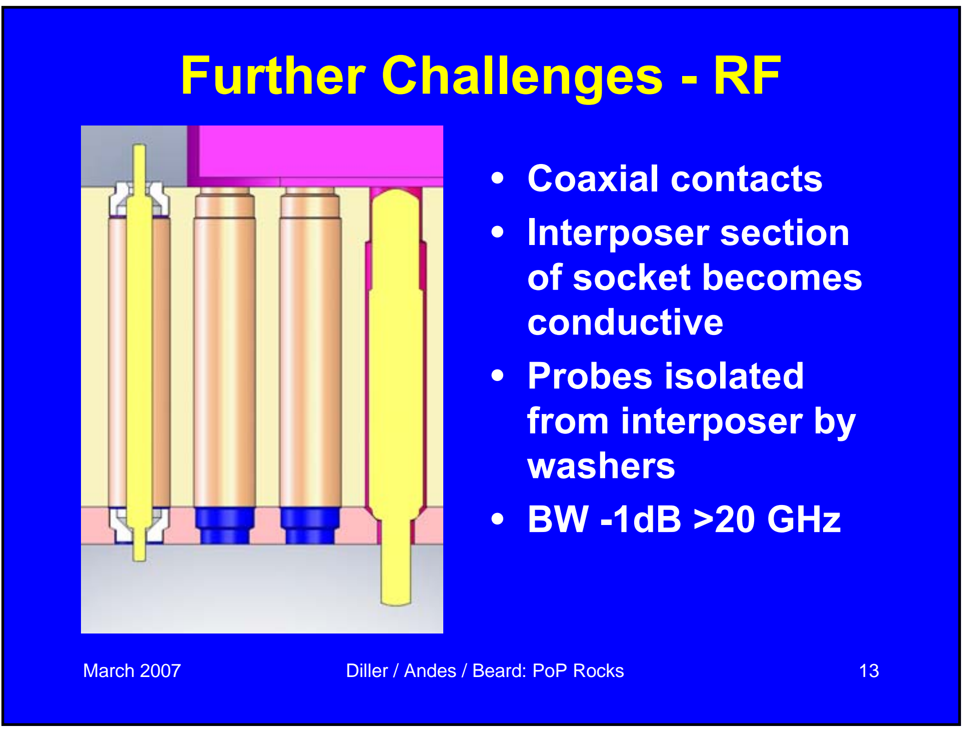


## Conclusions

- Radical contact challenges solved through interfacing experience
- Any broad, solutions-focused supplier can develop
- Consider the versatility and responsiveness of your partners