
# Burn-in & Test Socket Workshop

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Hilton Phoenix East/Mesa Hotel
Mesa, Arizona

IEEE

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Burn-in & Test Socket Workshop

# Technical Program

## Session 7
## Wednesday 3/06/02 8:00AM

## Burn-in Board Design

**"Burn-in Board Over-current Protection – What Are The Options?"**

**KW Low** - Intel Corporation
**Zamel Jaafar** - Intel Corporation

**"Protecting Conductor Pads On Burn-in Boards From Oxidation And Corrosion"**

**Alfred Sugarman** - Loranger International Corporation
**Al Loranger** - Loranger International Corporation

**"Power Decoupling Optimizer – A Systematic Frequency Domain Approach To BiB Noise Decoupling Simulation"**

**Isaac Chang -** Intel Corporation

# Burn-in Board Over-current Circuit Protection - What Are The Options?

KW Low/Zamel Jaafar
Intel Malaysia


2002 Burn-in and Test Socket Workshop
March 3 - 6, 2002

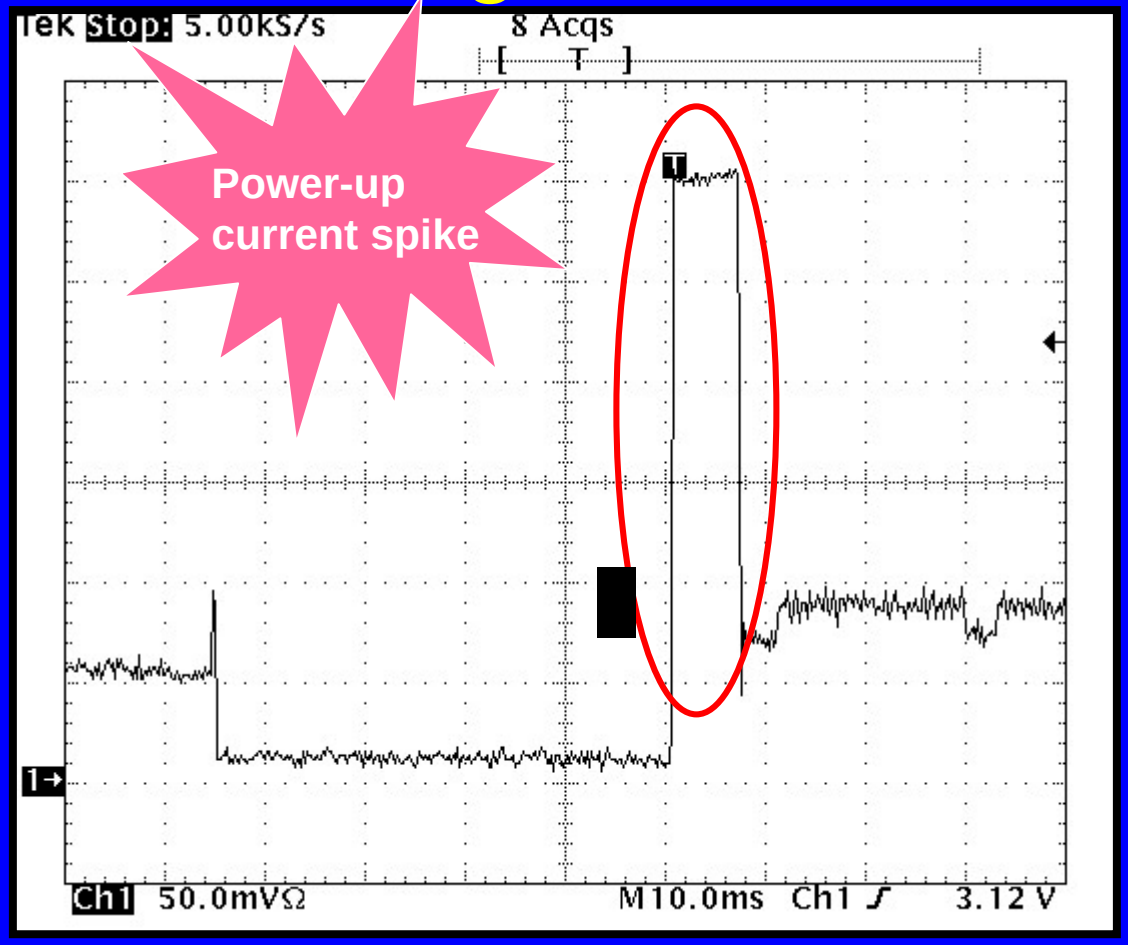
# Agenda

- Introduction
- UUT Switching Characteristics
- BIB Over-current Circuit Protective Devices
- Manufacturing Issues & Concerns
- Solutions Investigated
- Technology Challenges
- Conclusion
- Acknowledgement

# Introduction

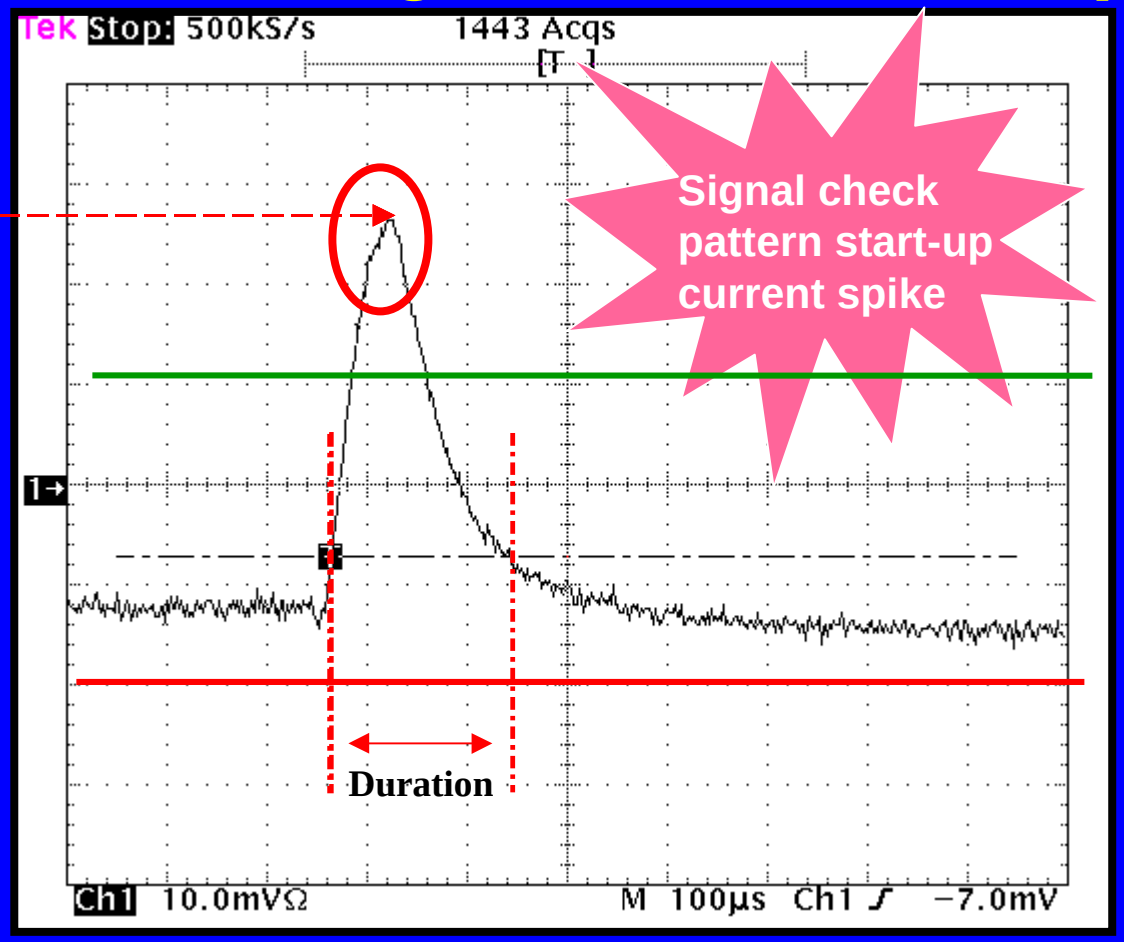
- BIB over-current protection prevents premature component failures, short circuits and fire hazards.
- In dynamic burn-in, current spikes occur at oven power supplies sequencing and auto signal checks.
- Common phenomenon for high current, high speed units under test.
- Fuses are effectively being utilized for overload or short-circuit protection.
- Incidences of nuisance fuse blowing is disruptive to production.
- Fuse replacement is an expensive & inconvenient task.
- Number of fuses on a burn-in board vary with each design.
- Other better alternatives (technology) are being reviewed.

# UUT Switching Characteristics(1)



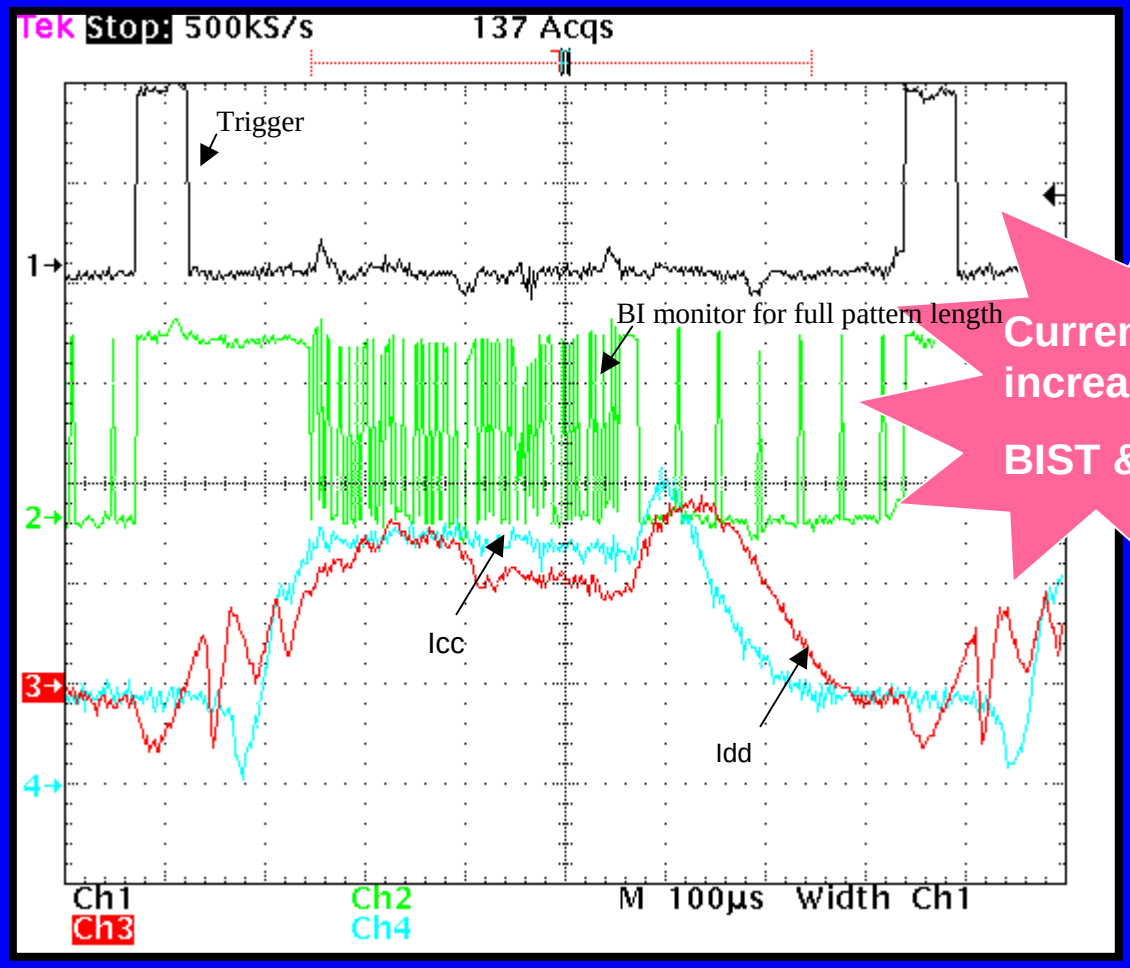

- During oven power sequencing there are current spikes on the BIB.
- These transients are harmful to the electronic circuit on the BIB and UUT.
- They last for tens of milliseconds and can reach hundreds of millivolts.

# UUT Switching Characteristics(.2)




- During signal check pattern testing current spikes are observed.
- Repetitive high current in amperes; hundreds of microseconds in duration.
- These current spikes can breach limit of the fuse rating.

# UUT Switching Characteristics(.3)

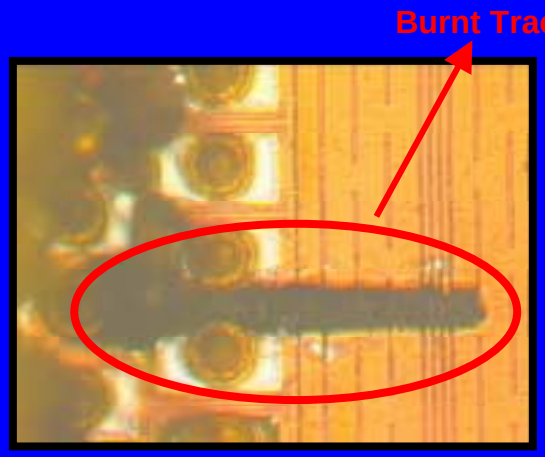



Current spikes increase during BIST & Reset

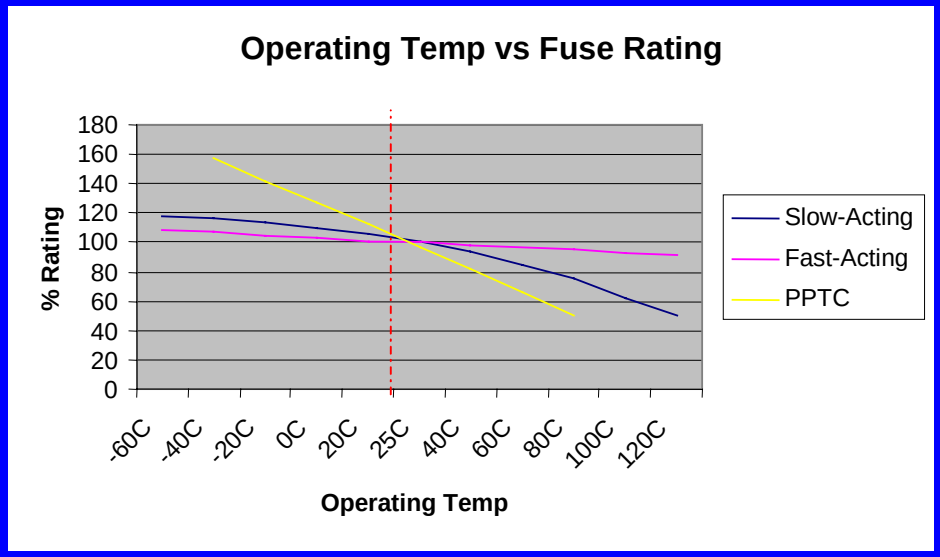
- During logic switching more current spikes are further evident.
- The magnitude and occurrence depends on number of power supplies & complexity of the stress pattern.

# BIB Over-current Protective Device (1)

- Fuses are commonly used to isolate and protect the UUT on BIB.
- Using correct fuse current rating, type (fast or slow-acting) and derating factor is important to avoid circuit electrical over-stress.
  - Fuse rating = Normal Operating Current/0.75 x % rating




Lack of protection causes die EOS

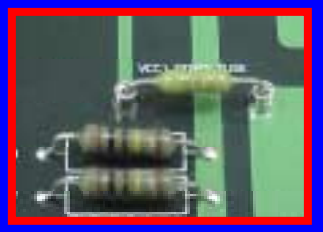



Fuse value is derated with elevated operating temperature

- They are current sensitive devices serving as a weak link in BIB circuit.
- Fuse characteristic is determined by respond to various current overload.
- Slow-acting fuse has more thermal inertia that tolerates initial overload current.
- Fast-acting or very fast-acting fuse is good for sensitive, critical circuits.

# BIB Over-current Protective Device (.2)

- Selection of circuit protective devices depends on
  - matching circuit characteristic to device specification
  - operating current, voltage and temperature
  - required protection device response time
  - interrupt rating
  - fault current and
  - circuit resistance
- Burn-in board circuit protection choice.
  - Wire Fuse
    - ✓ low power consumption
    - ✓ no leakage current
    - ✓ suitable for high voltage & high current circuits
      - × one time use only
      - × consumable item
      - × high maintenance cost



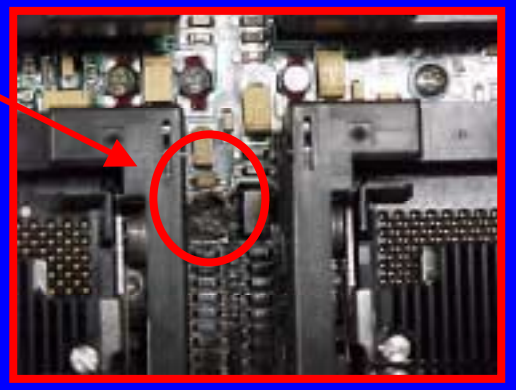
Subminiature fuse mounted into turrets

Subminiature fuse soldered onto fork connectors


Subminiature SMD fuses in receptacles

# Manufacturing Issues & Concern

- Resources are needed to detect, identify and repair burn-in boards with blown fuses.
  - Finance (money)
  - Headcount (labour)
  - Facility (equipment set-up)
- Burn-in board maintenance cost has escalated.
  - Labour and component increase
  - Need to manage component inventory
- Extra capacity baked into build plan to offset burn-in boards temporarily taken out of service.
  - More burn-in board inventory (spares buffer)
  - Long through-put-time for product builds (bottleneck)
  - Output yields are affected (need to build more in advance)
- Good UUTs could be scrapped when they are processed on a burn-in board with blown fuses.



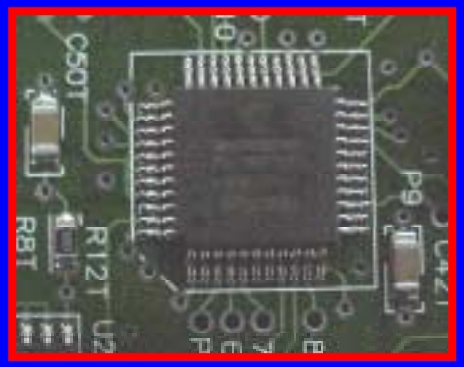
Components & BIB Burnt

# Solutions Investigated

- **Polymer-based Positive Temperature Coefficient (PPTC) fuse.**
  - ✓ resettable
  - ✓ low power consumption
  - ✓ small footprint
    - × resistance is higher than wire fuse
    - × max operating temperature ~85 deg C
    - × max operating current ~11A

PPTC Resettable fuse

- **Current-limiting IC.**
  - ✓ resettable
  - ✓ feedback signal for closed loop control
  - ✓ fast response
    - × high cost
    - × sensitive to voltage fluctuation
    - × susceptible to program interference




Custom Current-limiting IC

# Technology Challenges

- BIB application of resettable fuse depends on:
  - Ability to operate at 125 deg C; 45 to 95 deg C typical range
  - Little or no leakage current
  - Voltage rating < 5 volts; current rating 5A, 10A, 15A & 20A
  - Small footprint, preferably SMD
  - Low cold resistance
  - Improved time-current characteristic (speed of response) better than for slow blow fuse
- Other solution of using ICs are still being reviewed.
  - Requires additional circuit to sense and switch
  - Software has to be developed to complement circuit function
  - Takes up space and reduces socket density on BIB
  - More trace routing makes BIB design complex
  - Initial cost is higher

# Conclusion

- Burn-in board is designed with different fuse configuration.
  - Fuse per burn-in board
  - Fuse per socket
  - Fuse per socket cluster
  - Fuse per socket row
- Need for more user friendly circuit protective devices.
  - A better option to wire fuse
  - Something simple with minimum board re-design
  - It has to be a cost effective solution
  - Ideally maintenance free
- As burn-in ambient temperature is decreasing, resettable fuse provides an attractive alternative.
- Burn-in board is a multimillion $$$ business, any viable option has a ready market.

# Acknowledgement

**The authors would like to acknowledge the support provided by colleagues for their comments & suggestions in the preparation of this presentation:**

Anthony Wong, CS Low, HL Kon, KH Lee, KS Yeoh

&

P Schubring

**Thank You**

# PROTECTING CONDUCTOR PADS ON BURN-IN BOARDS FROM OXIDATION AND CORROSION

by Alfred Sugarman, Al Loranger

Presented at
BiTS Burn-In & Test Socket Workshop
March 3-6, 2002
Mesa, AZ

## PURPOSE

Evaluate different conductor pad coatings on burn-in boards for contact stability and resistance.

# PROCEDURE

- Printed circuit assemblies (PCAs) for testing a Loranger LGA 375SQ312L6617 socket were fabricated with the following conductor pad coatings.

  COATING THICKNESSES ON TESTED BOARDS
  - 20 µin Electroplated Gold
  - 50 µin Electroplated Gold
  - 300 µin Solder
  - bare copper
  - 100 µin Electroplated Nickel

- Coating thicknesses on conductor pads of the PCAs were independently measured to confirm the nominal values above.

- Electrical resistances and average contact deflections were measured in the sockets at 0 hours and at increments of time throughout the burn-in process. Resistances were measured by using a gold plated mock device. The mock device nulled any effect of plating and/or coatings on the package to isolate the data to the burn-in board conductor pad plating only.

# Procedure Continued

- PCAs were assembled with sockets and heated to 125ºC for increments of time up to 1,000 hours to simulate burn-in process.
- Periodically the PCAs were removed from the oven to measure contact resistances and examine the conductor pads.
- Gold coated boards were cleaned after 1,000 hours burn-in by first swabbing conducting pads with isopropyl alcohol and then cleaning them in a dishwasher with ordinarily dishwasher detergent.
- Contact resistance with contact deflection was evaluated by stacking.0038” paper shims on top of the mock device and closing the cover.

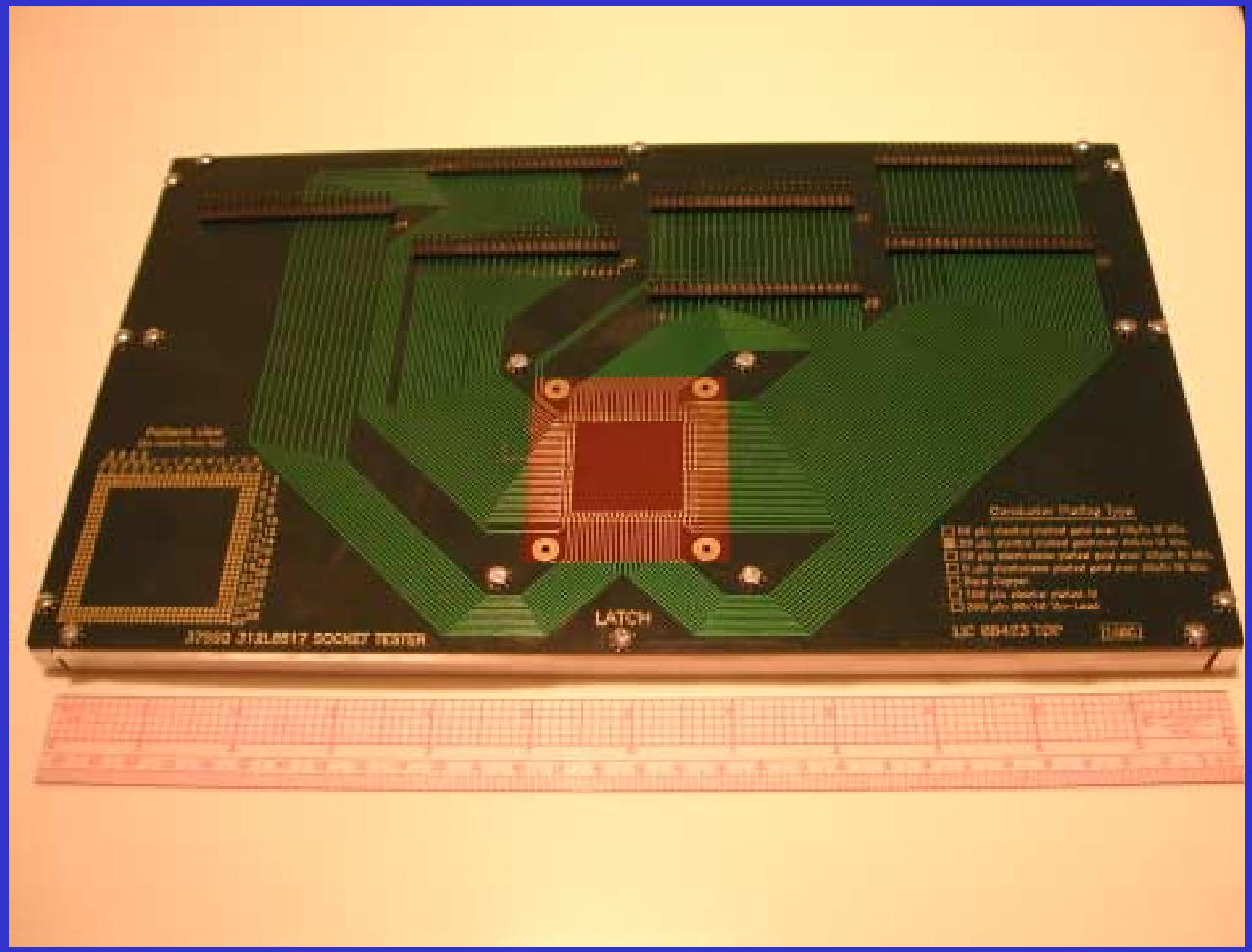
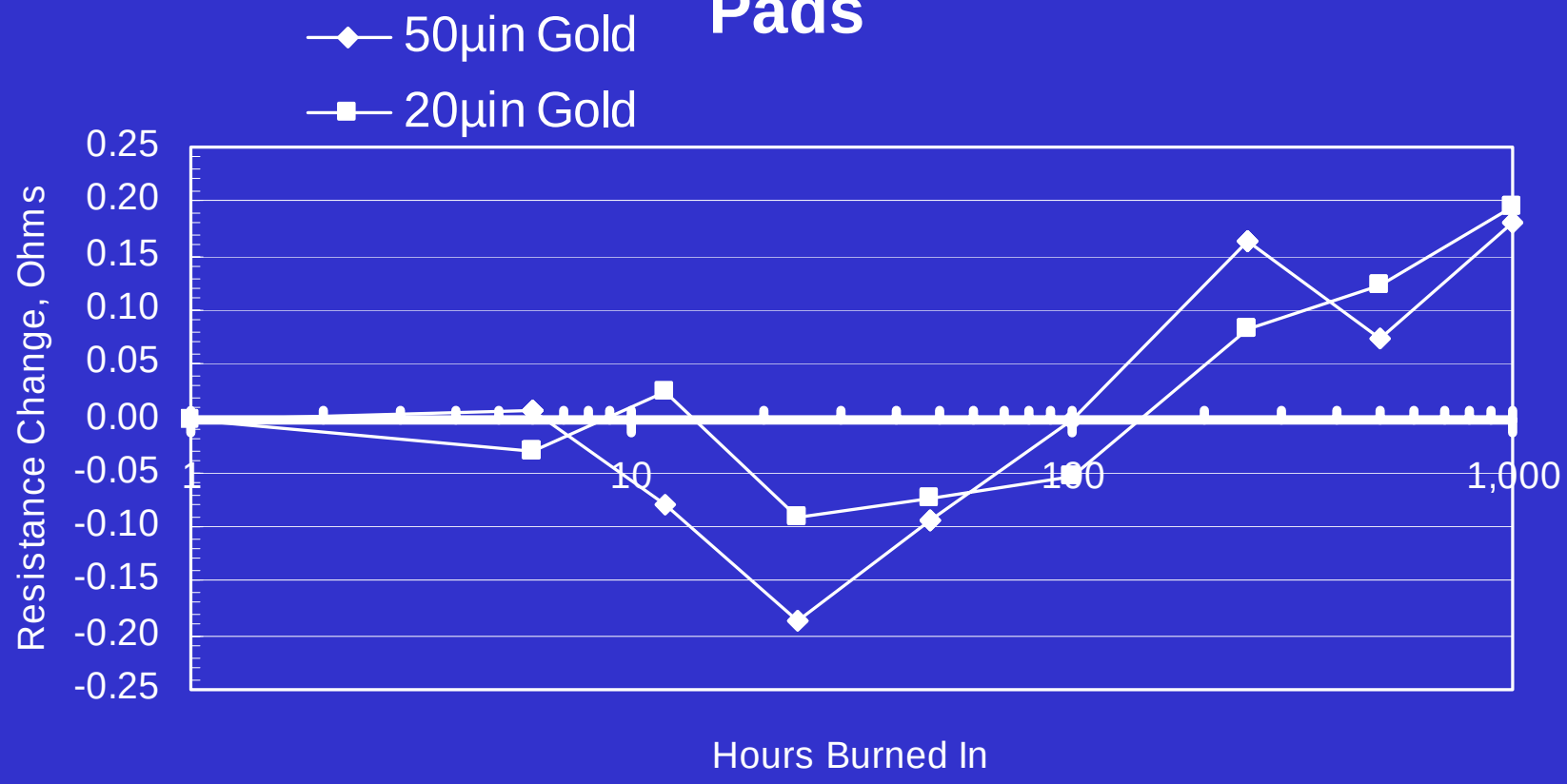
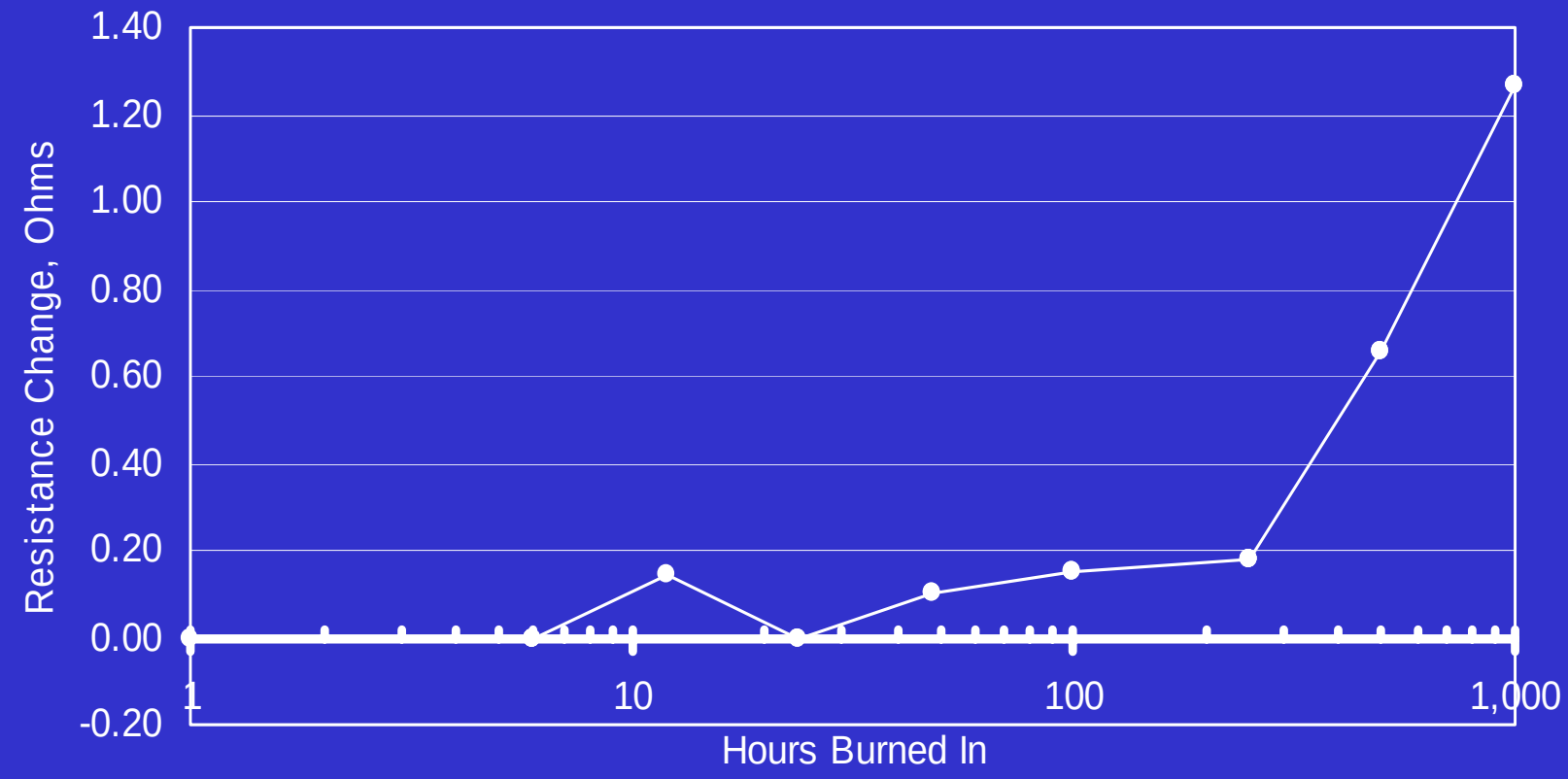


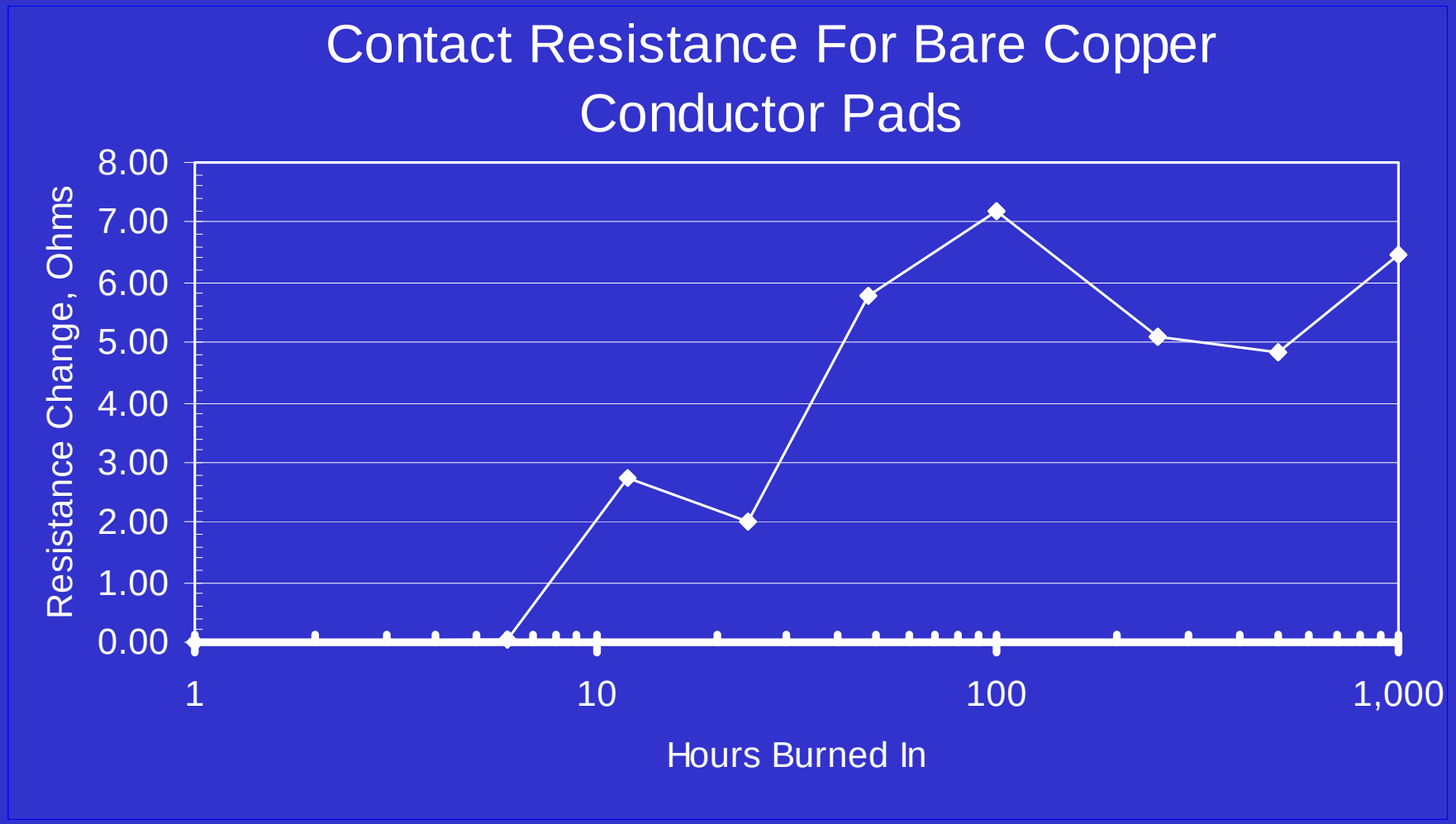

Figure 1. Typical MAP6 board on which sockets were burned in and resistances measured.

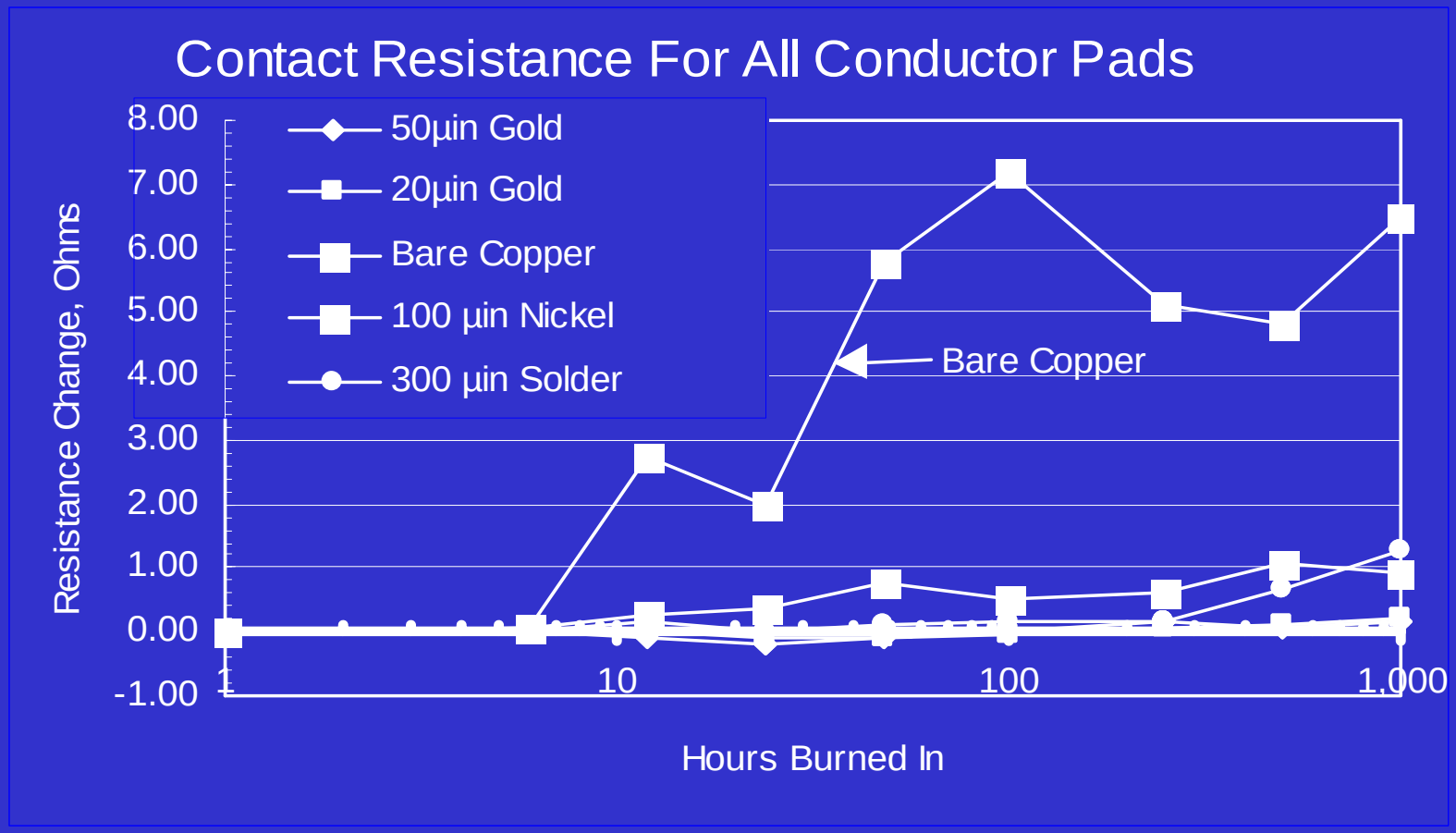
# Contact Resistance For Gold Plated Conductor Pads



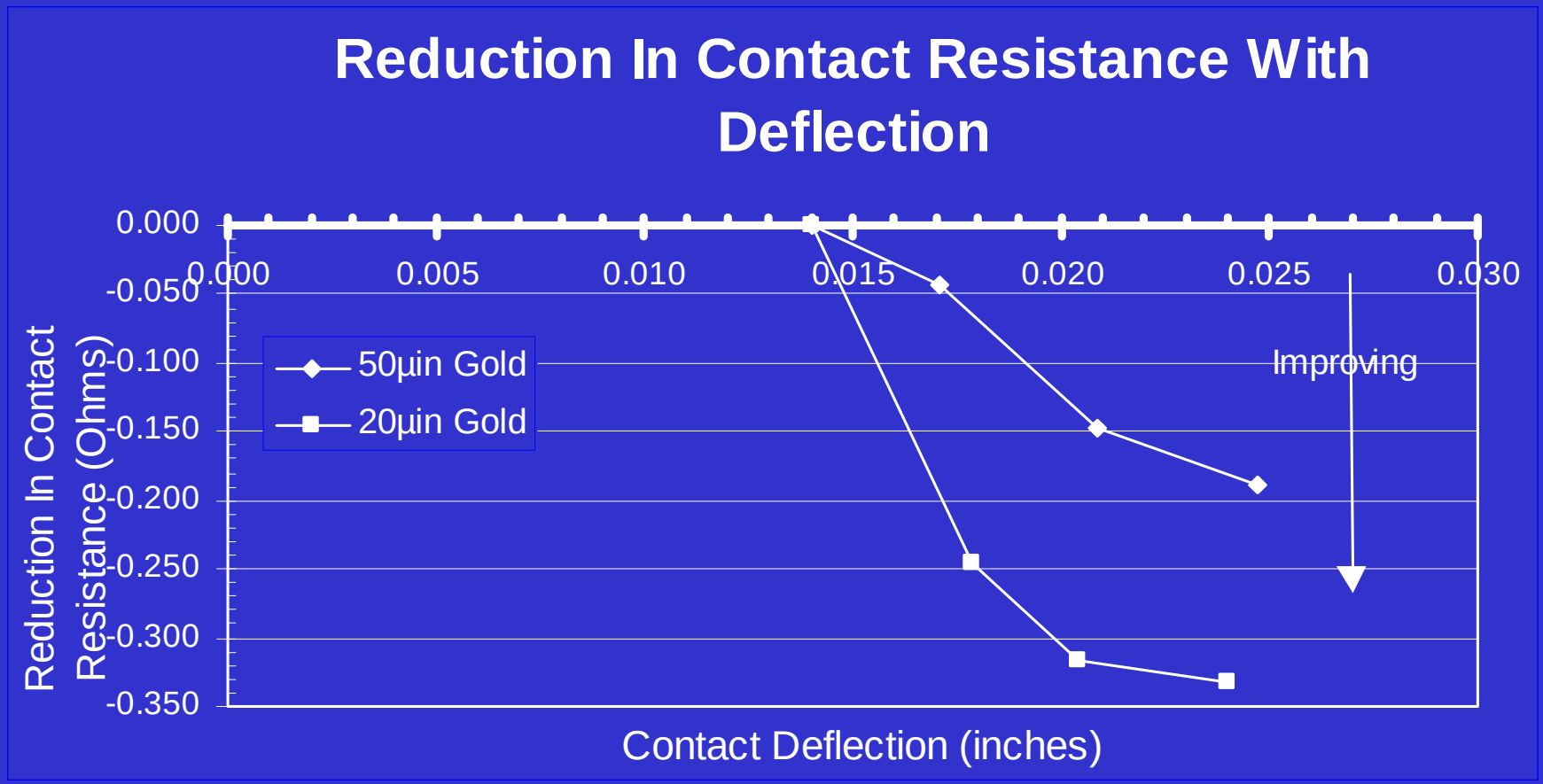
# Contact Resistance For Solder Coated Conductor Pads




Contact Resistance For Bare Copper Conductor Pads
Resistance Change, Ohms
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
1
10
100
1,000
Hours Burned In


Contact Resistance For All Conductor Pads
50µin Gold
20µin Gold
Bare Copper
100 µin Nickel
300 µin Solder
Bare Copper
Resistance Change, Ohms
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
-1.00
1
10
100
1,000
Hours Burned In

# Reduction In Contact Resistance With Deflection



## TABLE 1. NUMBER OF OPEN CONTACTS AFTER BURN-IN AT 125ºC

| Hours Burn-In | 1 | 6 | 12 | 24 | 48 | 100 | 250 | 500 | 1,000 |
|---|---|---|---|---|---|---|---|---|---|
| 50µin Gold | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20µin Gold | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 300 µin Solder | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 24 |
| 100 µin Nickel | 0 | 1 | 2 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bare Copper | 0 | 2 | 0 | 0 | 6 | 3 | 15 | 27 | 65 |

Figure 2. 50 µin thick gold plated conductor pads after 500 hrs at 125 ºC. This is typical of appearance of similar conductor pads.

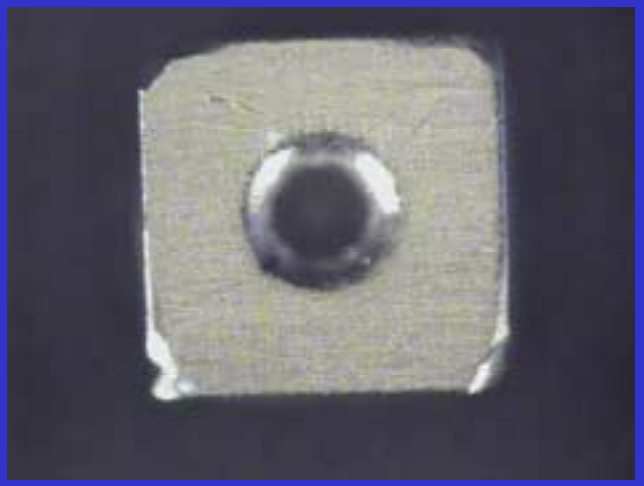


Figure 3. 50 µin thick gold plated conductor pads after 1,000 hrs at 125 ºC. Note good uniform appearance.

Figure 4. 20 µin thick electroless gold plated conductor pads after 1,000 hrs at 125 ºC. Note blistering.

Figure 5. 300 µin thick solder plated conductor pads after 1,000 hrs at 125 ºC. Note 5 mil deep witness marks left in the solder.

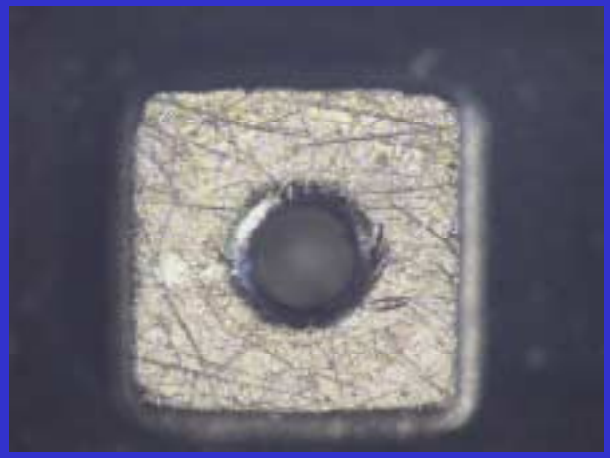


Figure 6. 100 µin nickel plated conductor pad after 1,000 hours at 125ºC.

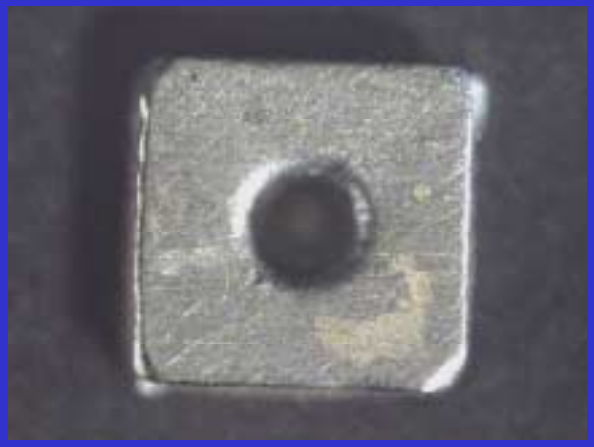


Figure 7. Bare copper conductor pad after 1,000 hours at 125 ºC.

# REVIEW OF GOLD COATING THICKNESS REQUIREMENTS

- IPC-6012A, "Qualification and Performance Specification for Rigid Printed Boards", Table 3-2

**Table 3-2 (partial) Final Finish, Surface Plating Coating Requirements**

| Finish | Class 1 (General Electronic Products) | Class 2 (Dedicated Electronic Products) | Class 3 (High Reliability Electronic Products) |
|---|---|---|---|
| **Gold (min) for edge-board connectors and area not to be soldered** | 0.8 µm (30 µin) | 0.8 µm (30 µin) | 1.25 µm (49 µin) |

- EIA – 540 GAAA, "Detail Specification for Burn-In Sockets for Chip Carrier Packages with Molded Carrier Rings for Use in Electronic Equipment", October 1993.

Paragraph 2.2.9 says .....

2.2.9 CONTACT FINISH AT TERMINATION AREA

Contact finish at the termination area shall be designated by one letter as follows:

| | |
|---|---|
| K:Gold over Nickel | 0.76 micron (30µ") min. gold over 1.27 microns (50µ") min. to 3.81 microns (150µ") max. nickel. |

# DISCUSSION

- Gold coated conductor pads particularly those with 50 µin gold had 0 opens and the conductor pads had best appearance.

- Initial resistance and resistance increase with burn-in time was smallest with gold coated conductor pads compared with pads coated with nickel, solder and bare copper conductor pads.

- Conductor pad coatings of nickel and solder had larger increases in resistance. Bare copper conductor pads had largest resistance increase with burn-in time

Discussion (continued)

- Conductor pads coated with 100 µin nickel and 300 µin solder and with bare copper had poor electrical stability compared with gold coated conductor pads.

- Increasing deflection of contacts significantly reduces contact resistance by increasing contact force and can more than compensate for increasing resistance with burn-in time.

(Discussion Continued)

- Reasons for high resistances and low stability in other than gold coated conductor pads are ...

| | |
|---|---|
| - Copper and nickel coated pads | Relatively hard oxide coating on surface of pads |
| - Solder coated pads | Creep of contact through solder until it touches parent conductor pad metal. |

# CONCLUSIONS

- Gold coated conductor pads performed better than all others to achieve lowest contact resistance and most stability
- Increasing contact deflection (equivalent to increasing force) made significant reductions in contact resistance more than compensating for the increase in resistance with burn-in time

# Power Decoupling Optimizer – A Systematic Frequency Domain Approach to BIB Noise Decoupling Simulation

**Isaac Chang**
**Intel Corporation**

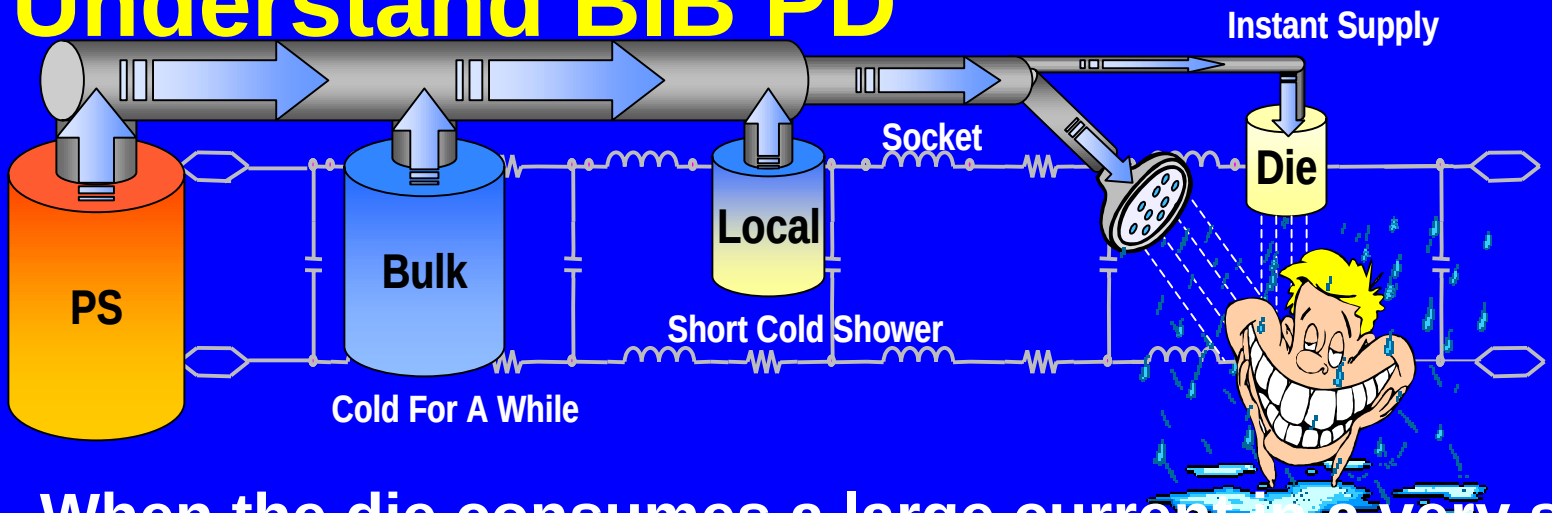

**2002 Burn-in and Test Socket Workshop**

**March 3 - 6, 2002**

# Agenda

- Understand BIB Power Decoupling(PD)
- Introduction
- Existing PD Approach & Drawbacks
- New PD Optimization(PDO) BKM(Best Known Method)
- PDO Uses Ztarget
- Cres Effect in Optimization
- PDO – Cbulk/Clocal Optimization Steps
- Capacitor Selection for Cbulk/local
- Example: BIB Capacitor Optimization
- Key Results
- Conclusion
- Acknowledgement

# Understand BIB PD

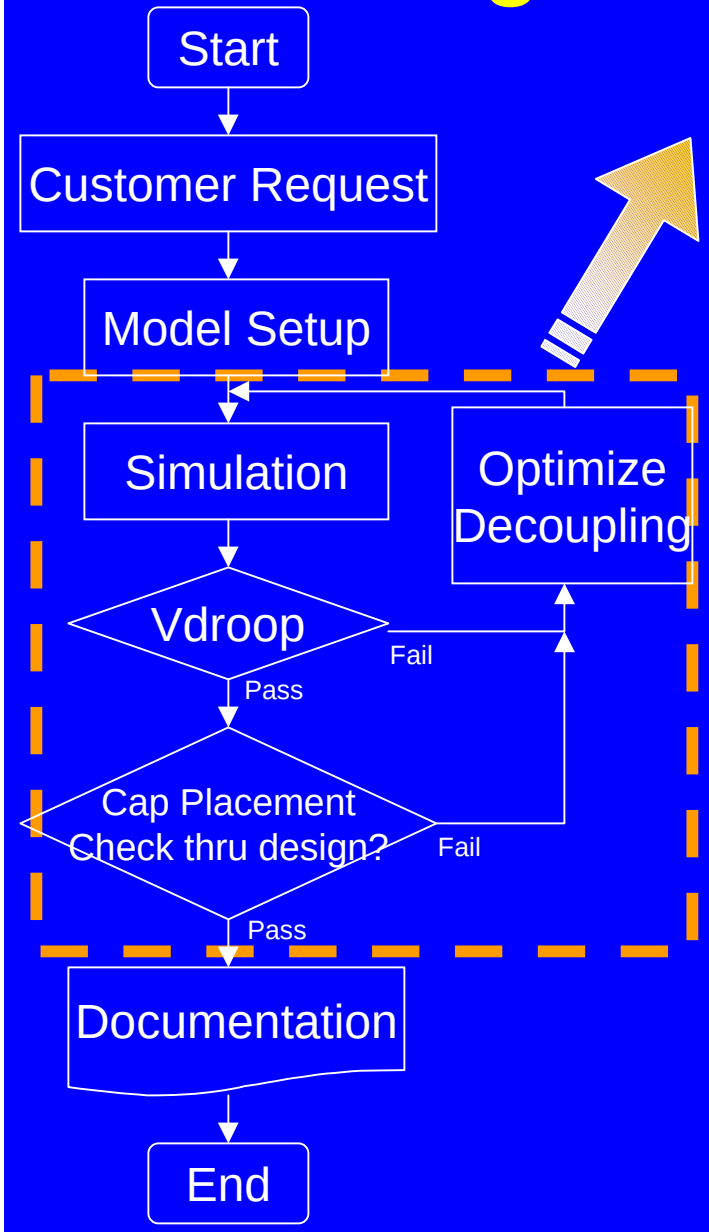



- When the die consumes a large current in a very short period during the output state transition, it will cause unwanted voltage drop(spikes/transient) along the power path.
- Thus, the decoupling capacitors(bulk/local) are placed near to the die to lower the ground bounce/transient noise on the power supply(PS) for the device.
  - They will charge up during the less stressful period and then provide additional charges during the transient instead of the PS, thus reducing the spike magnitude along the power path.

# Introduction

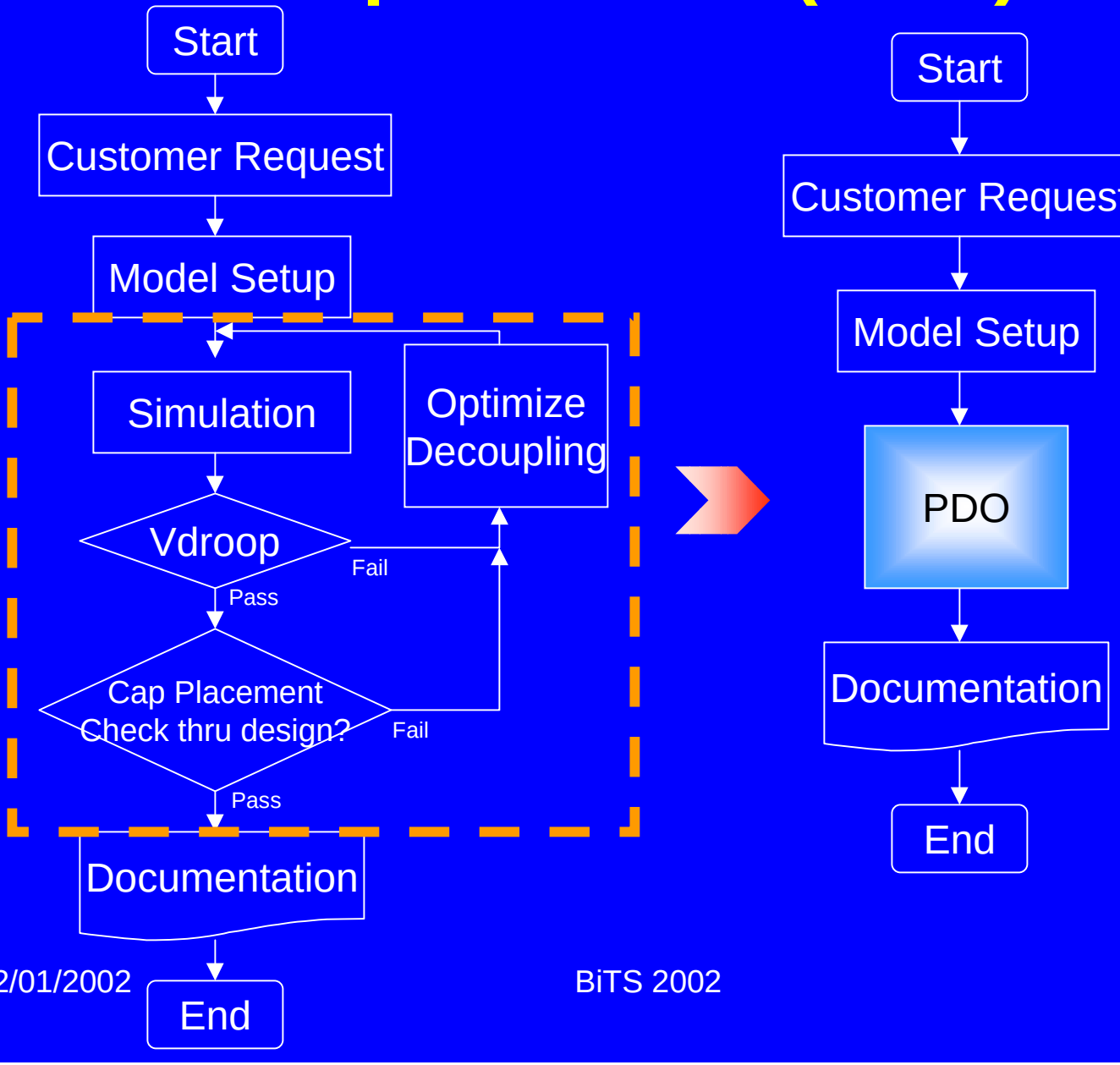
- **Existing Time Domain(TD) methodology of power noise decoupling is critical for ensuring stable/consistent power delivery for Burn-In Board(BIB) operation.**
  - **Utilizes a full system power delivery model and simulated using PSPICE software in TD using trial-&-error approach.**
  - **Requires numerous tedious iterations to determine the optimized decoupling capacitance.**
  - **Several major drawbacks in predicting the decoupling requirements with the selective/appropriate capacitors in term of types and quantities effectively/accurately.**

# Existing PD Approach & Drawbacks




- **Non systematic approach**
  - **It's merely trial-&-error TD approach decoupling optimization**
- **Time consuming**
  - **Many steps taken for optimization**
- **Unable to understand individual capacitor performance/ effectiveness**
  - **Each capacitor is only effective before its resonant frequency region**
- **Thus, it needs a systematic /effective methodology for a more comprehensive optimization solution**

# New PD Optimization(PDO) BKM

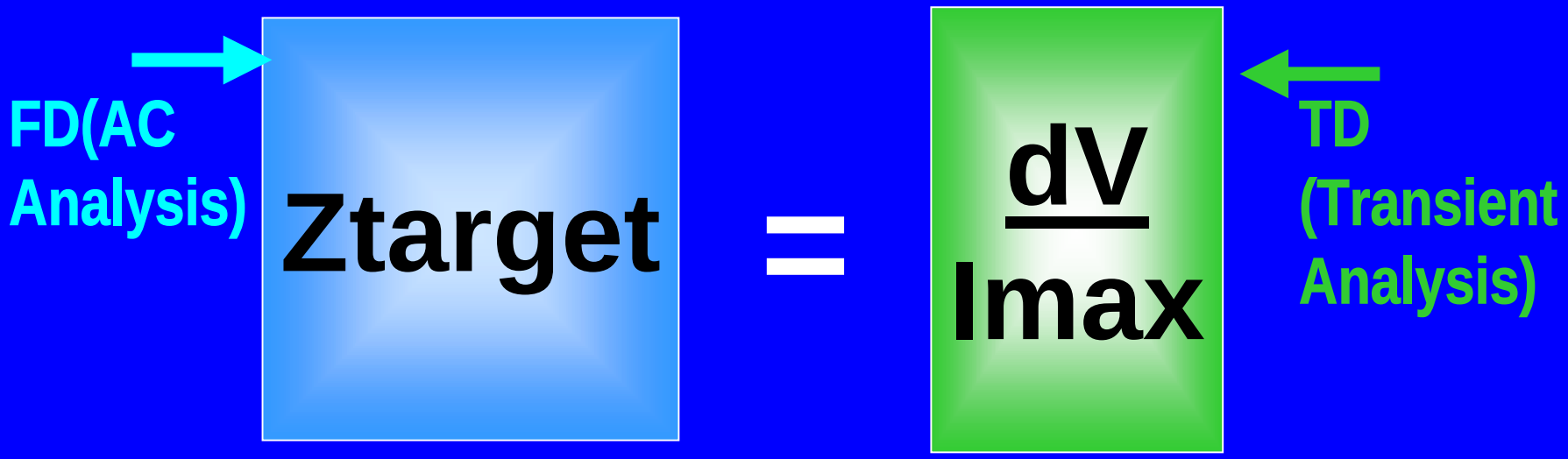


# PDO Uses Ztarget(rolling down!)

| Year | Voltage (V) | Power Dissipated (W) | Current (A) | Ztarget (mΩ) | Ripple – *noise* (mV) | Frequency (MHz) |
|---|---|---|---|---|---|---|
| 1990 | 5.0 | 5 | 1 | 250 | 250 | 16 |
| 1993 | 3.3 | 10 | 3 | 54 | 165 | 66 |
| 1996 | 2.5 | 30 | 12 | 10 | 125 | 200 |
| 1999 | 1.8 | 90 | 50 | 1.8 | 90 | 600 |
| 2002 | 1.2 | 180 | 150 | 0.4 | 60 | 1200 |

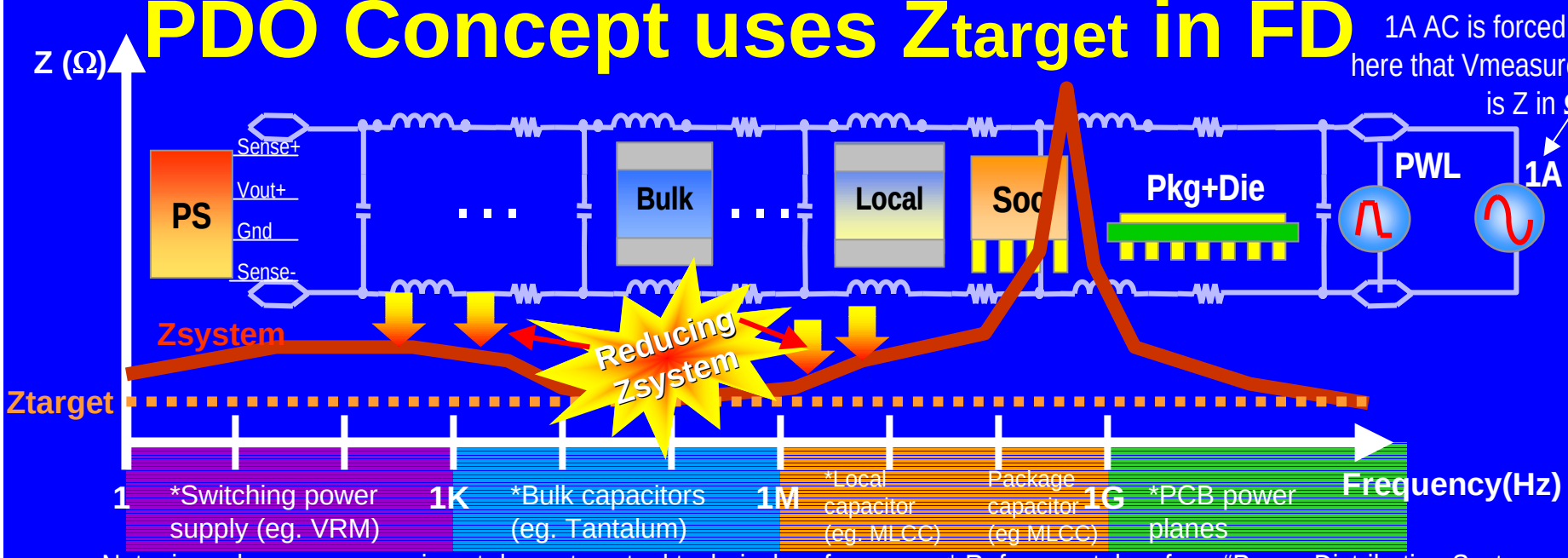
- PDO Concept is based on reducing the overall system impedance(Zsystem) to be <Ztarget in FD.
- Ztarget trend is decreasing at an alarming rate for high current future microprocessor requirement.
  - Data is extracted from “Power Distribution System Design Methodology & Capacitor Selection for Modern CMOS Technology.” by Larry Smith, except ripple is calculated.

# Ztarget Definition & Relationship With V




- Ztarget is the impedance that the test tooling system has to be optimized to which it will ensure that noise droop in the system will be able to meet the noise droop tolerance(allowed ripple) at the highest current ramp.

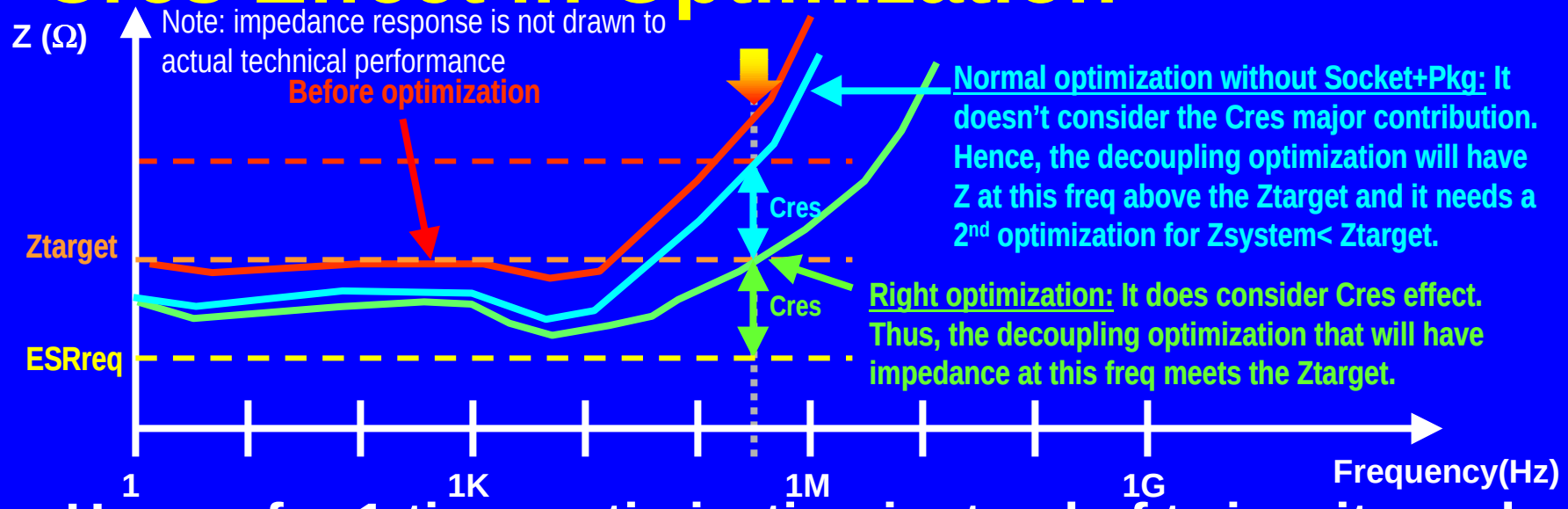
# PDO Concept uses Ztarget in FD




Note: impedance response is not drawn to actual technical performance. * Reference taken from "Power Distribution System Design Methodology & Capacitor Selection for Modern CMOS Technology." by Larry Smith

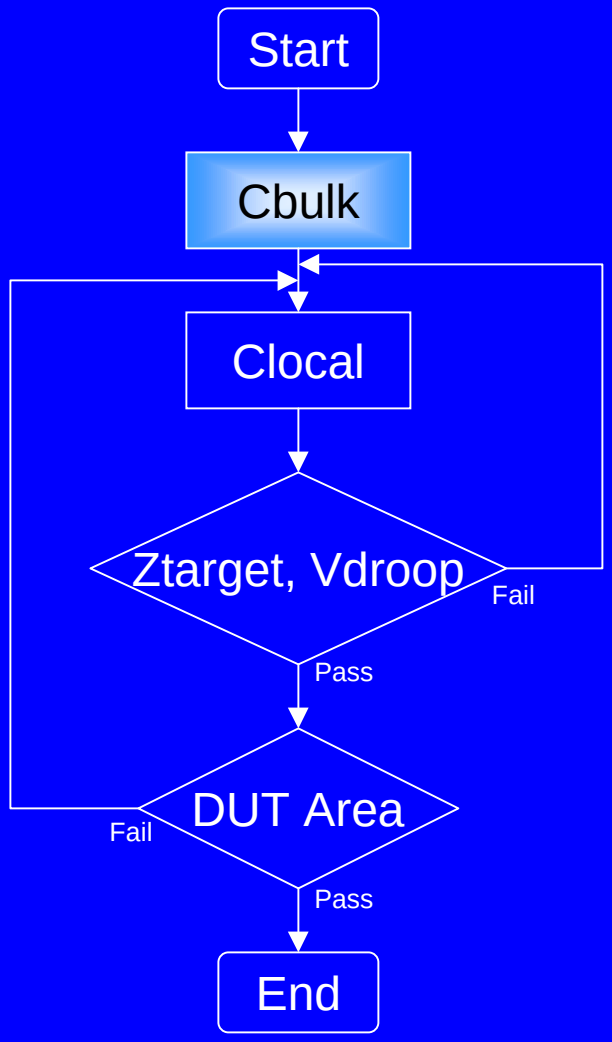
- **Zsystem can be reduced(<Ztarget) by using capacitor with the consideration of its resonance.**
- **However, not the whole Zsystem over the whole freq range can be reduced, e.g. the package & die, which the bulk/local decoupling are out of influence to decouple noises at that level.**

# Cres Effect in Optimization



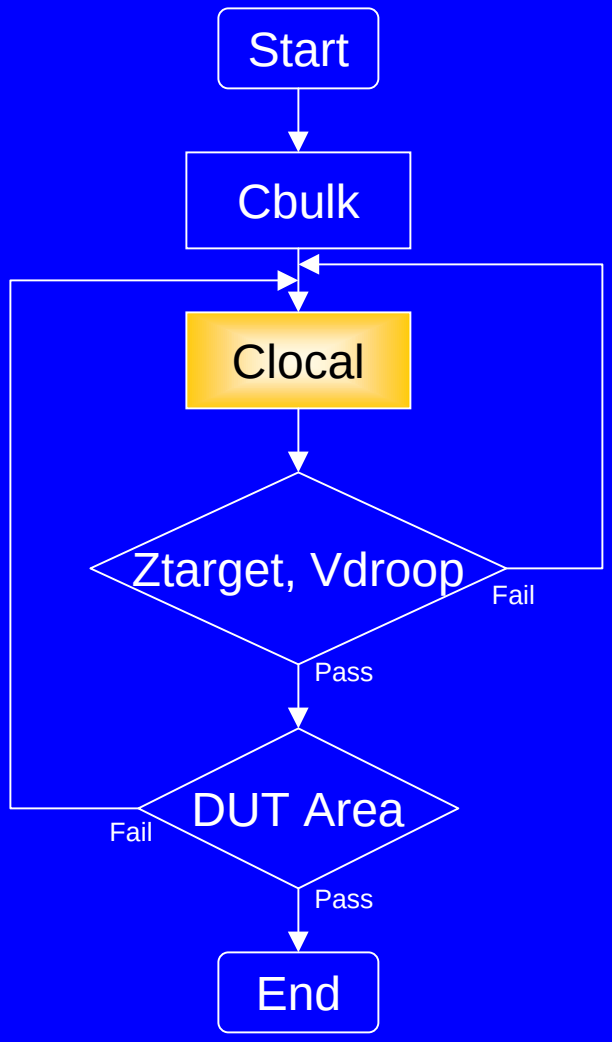

- Hence, for 1-time optimization instead of twice, it needs to consider the highest resistive element, ie the socket Cres effect since it increases the Zsystem.
- Use Cres effect as reference for estimating capacitor quantity by reducing Ztarget by Cres to give the required ESR for each cap type.
- By having total cap ESR of a cap type(all parallel) meeting ESRreq(cap optimization) will bring Zsystem to below <Ztarget(system optimization).

# PDO – Cbulk Optimization Steps



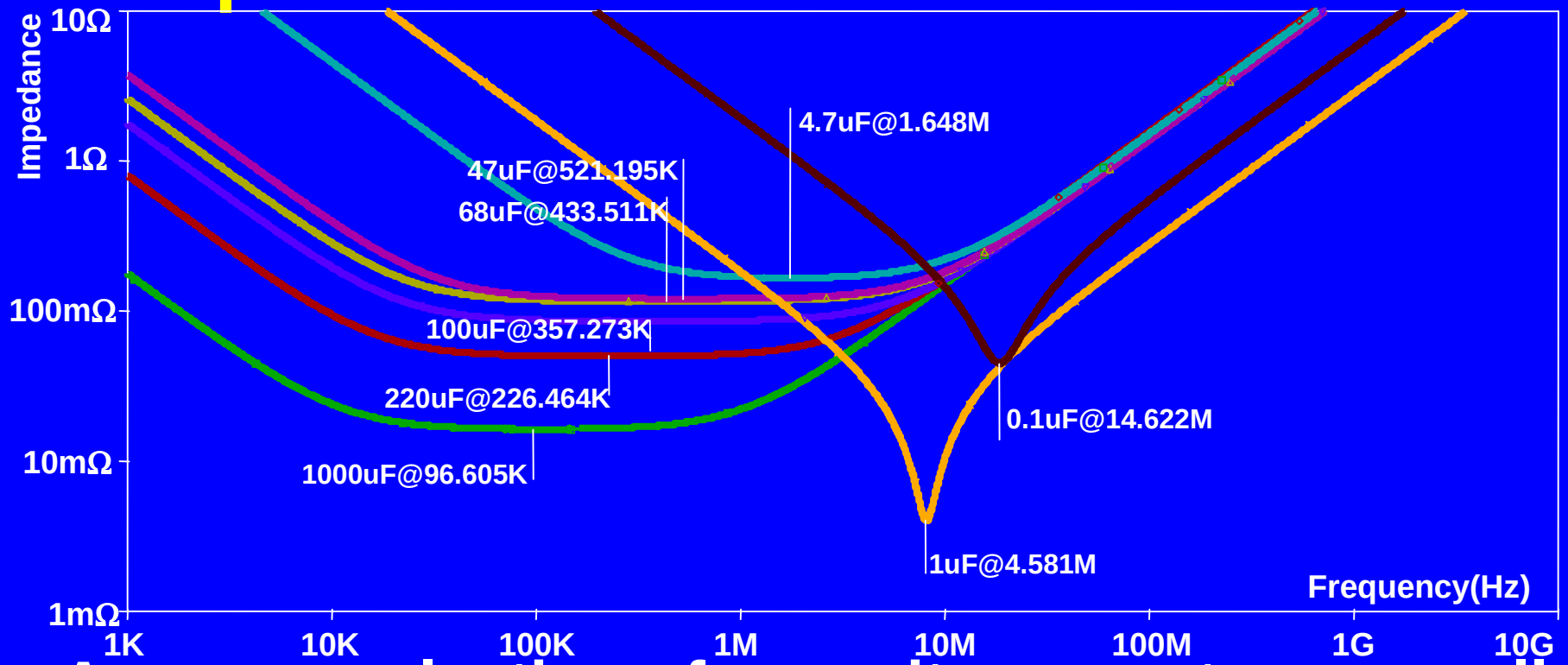

- **Calculate**
  - **Ztarget = dV/Imax**
  - **Cbulk = I.dt/dV**
- **Select caps to meet Cbulk.**
- **Check Cbulk whether meeting Ztarget.**

# PDO – Clocal Optimization Steps



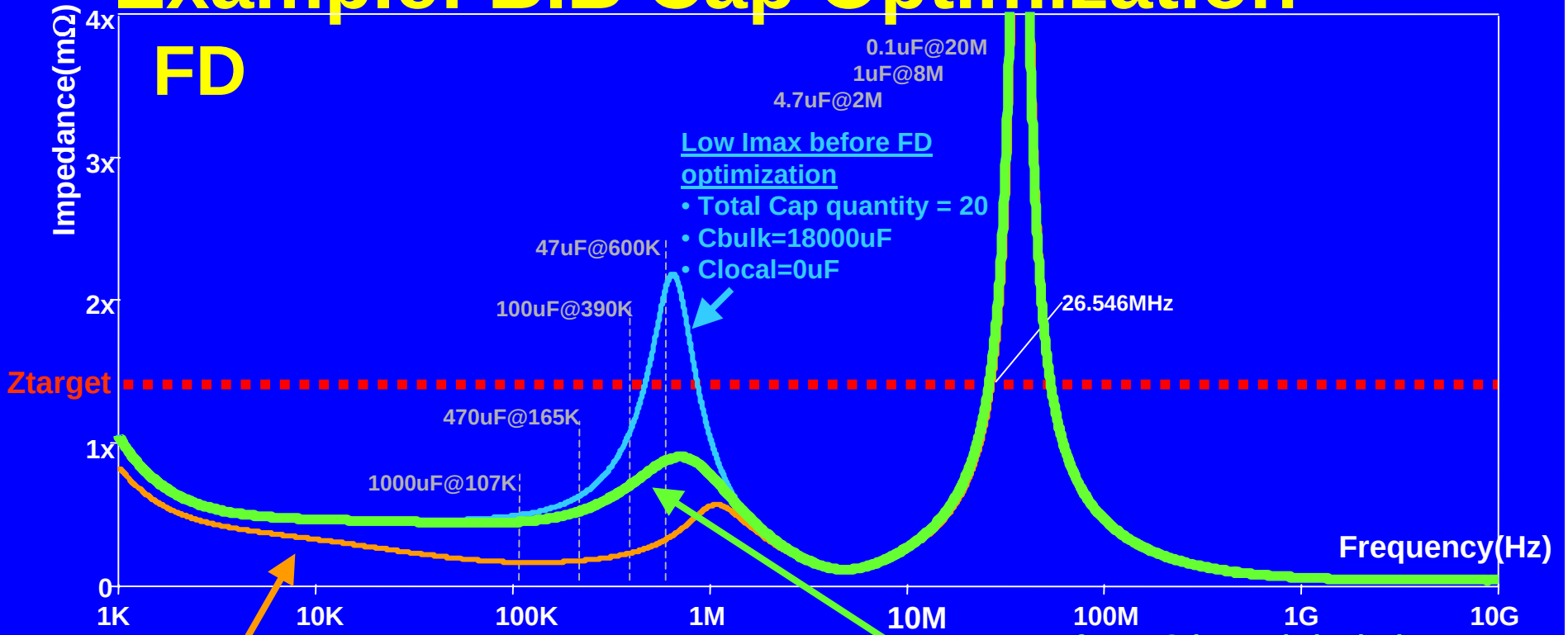

- **Calculate**
  - **Cres = Soc Cres/#Pwr pin + Soc Cres/#Gnd pin.**
  - **ESRreq=Ztarget-Cres**
    **(ESRreq:total ESR required from a combination of caps)**
- **Compute effective freq cap quantity(start with low freq cap) by ESR that meets ESRreq.**
- **Go to next higher effective freq cap(provided with a standard cap list in place)**

# Capacitor Selection for Cbulk/local

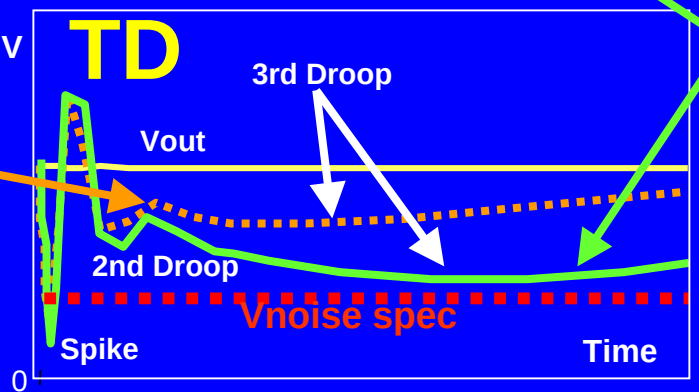



- A proper selection of capacitors must cover well the frequency spectrum for Zsystem reduction effectiveness to <Ztarget.
  - The effective frequency in this case is estimated from about 1KHz~100MHz range.

# Example: BIB Cap Optimization




**Baseline:**
- High Imax after TD optimization
- Total Cap quantity = 77
- Cbulk=18000uF
- Clocal=4734uF



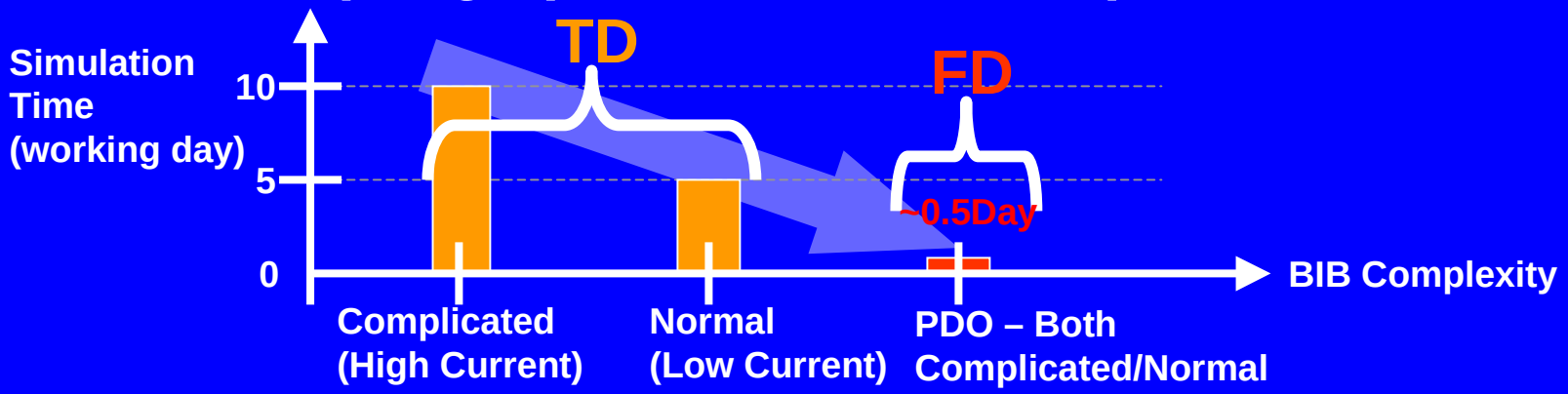

**Low Imax after PDO (FD optimization)**
- Note, the cap resonance that crosses with Zsystem is 47uF and use ESRreq to determine its quantity
- Total Cap quantity = 25
- Cbulk=18000uF, Clocal=188uF

– TD confirms PDO capacitor reduction scheme.

– PDO(FD) uses less capacitor than TD.

# Key Results

- Proven more systematic as compared to the merely trial-&-error TD approach decoupling optimization
- Better understanding of individual capacitor performance/effectiveness before placing any capacitor for decoupling.
- Shown FD effectiveness in Z reduction through proper capacitor selection.
- Less time consuming because it uses less iterations to achieve decoupling optimization as compared to TD



# Conclusion

- PDO is a more systematic and speedy BKM for noise decoupling by proper capacitor selection to reduce Zsystem to >Ztarget.
- PDO can be used in any test tooling platform.
- The capacitors used today may have a big challenge to meet Ztarget below 10mΩ. Hence, it needs to path find ultra low ESR cap to cater future low Z system.

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